FT5x06

True Multi-Touch Capacitive Touch Panel Controller

INTRODUCTION

The FT5x06 Series ICs are single-chip capacitive touch panel controller ICs with a built-in 8 bit Micro-controller unit (MCU).They adopt the mutual capacitance approach, which supports true multi-touch capability. In conjunction with a mutual capacitive touch panel, the FT5x06 have user-friendly input functions, which can be applied on many portable devices, such as cellular phones, MIDs, netbook and notebook personal computers.

The FT5x06 series ICs include FT5206/FT5306/FT5406, the difference of their specifications will be listed individually in this datasheet.

FEATURES

- Mutual Capacitive Sensing Techniques
- True Multi-touch with up to 10 Points of Absolution X and Y Coordinates
- Immune to RF Interferences
- Auto-calibration: Insensitive to Capacitance and Environmental Variations
- Supports up to 28 Transmit Lines and 16 Receive Lines
- Supports up to 8" Touch Screen
- Full Programmable Scan Sequences with Individual Adjustable Receive Lines and Transmit Lines to Support Various Applications
- High Report Rate: More than 100Hz
- Touch Resolution of 100 Dots per Inch (dpi) or above -- depending on the Panel Size
- Optional Interfaces :I2C/SPI
- 2.8V to 3.6V Operating Voltage
- Supports 1.8V/AVDD IOVCC
- Capable of Driving Single Channel (transmit/receive) Resistance: Up to15K Ω
- Capable of Supporting Single Channel (transmit/receive) Capacitance: 60 pF
- Optimal Sensing Mutual Capacitor: 1pF~4pF
- 12-Bit ADC Accuracy
- Built-in MCU with 28KB Program Memory, 6KB Data Memory and 256B Internal Data Space
- 11 Internal Interrupt Sources and 2 External Interrupt Sources
- 3 Operating Modes
  - Active
  - Monitor
  - Hibernate
- Operating Temperature Range: -20°C to +85°C

TABLE OF CONTENTS

1 OVERVIEW

1.1 Typical Applications

FT5x06 accommodate a wide range of applications with a set of buttons up to a 2D touch sensing device, their typical applications are listed below.

- Mobile phones, smart phones
- MIDs
- Netbook
- Navigation systems, GPS
- Game consoles
- Car applications
- POS (Point of Sales) devices
- Portable MP3 and MP4 media players
- Digital cameras

FT5x06 Series ICs support < 8.0" Touch Panel, users may find out their target IC from the specs listed in the following table,

Model Name	Panel		Package			Touch Panel Size	Recommended Pitch
	TX	RX	Type	Pin	Size		
FT5206GE1	15	10	QFN5*5	40	0.75-P0.4	≤3.7"	~5mm
FT5306DE4	20	12	QFN6*6	48	0.75-P0.4	≤5.0"	~5mm
FT5406DQ9	26	16	QFN6*6	56	0.55-P0.35	≤7.0"	~5mm
FT5406EE8	28	16	QFN8*8	68	0.75-P0.4	≤8.0"	~6mm

Remarks: FocalTech suggests to use pitch between 4.0mm to 6.0mm; The customer can decide the pitch based on applications.

2 FUNCTIONAL DESCRIPTION

Architectural Overview Figure2-1 shows the overall architecture for the FT5x06.

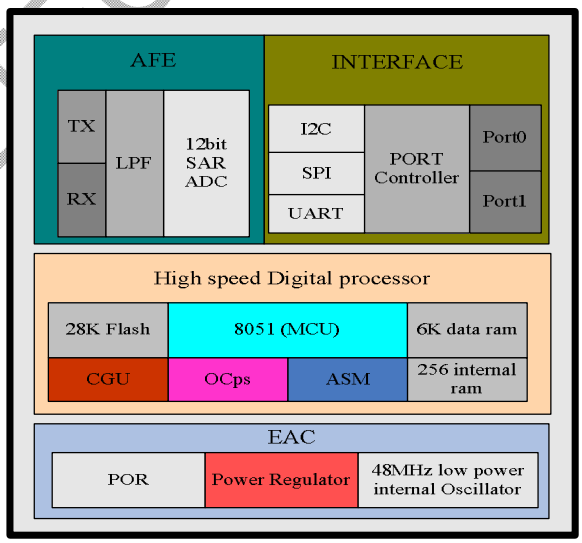


Figure 2-1 FT5x06 System Architecture Diagram

The FT5x06 is comprised of five main functional parts listed below,

- Touch Panel Interface Circuits

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the

panel and processes the received signals from the panel. So, it supports both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces, which will be explained in detail in a later section.

- 8051-based MCU

This MCU is 8051 compatible with some enhancements. For instant, larger program and data memories are supported. In addition, a Multiplication-Division unit (MDU) is implemented to speed up the touch detection algorithms. Furthermore, a Flash ROM is implemented to store programs and some key parameters.
Complex signal processing algorithms are implemented with firmware running on this MCU to process further the received signals in order to detect the touches reliably. Communication protocol software is also implemented on this MCU to exchange data and control information with the host processor.

- External Interface
  - I2C/SPI: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - WAKE: an interrupt signal for the host to change FT5x06 from Hibernate to Active mode
  - /RST: an external low signal reset the chip.
- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.8V for digital circuits from the input VDD3 supply
- Power On Reset (POR) is active until VDDD is higher than some level and hold decades of µs.

2.1 MCU

This section describes some critical features and operations supported by the 8051 compatible MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the 8051 compatible MCU core, we have added the following circuits,

- MDU: A 16x8 Multiplier and A 32/32 Divider
- Program Memory: 28KB Flash
- Data Memory: 6KB SRAM
- Real Time Clock (RTC): A 32KHz RC Oscillator
- Timer: A number of timers are available to generate different clocks
- Master Clock: 24/ 48MHz from a 48MHz RC Oscillator
- Clock Manager: To control various clocks under different operation conditions of the system

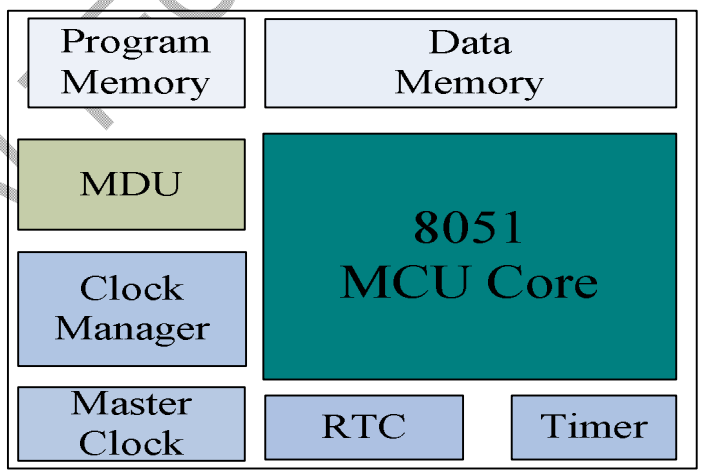


Figure 2-2 MCU Block Diagram

2.2 Operation Modes

FT5x06 operates in the following three modes:

- Active Mode

When in this mode, FT5x06 actively scans the panel. The default scan rate is 60 frames per second. The host processor can configure FT5x06 to speed up or to slow down.

- Monitor Mode

When in this mode, FT5x06 scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. When in this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT5x06 shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor.

- Hibernate Mode

In this mode, the chip is set in a power down mode. It shall only respond to the "WAKE" or "RESET" signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

2.3 Host Interface

Figure 2-3 shows the interface between a host processor and FT5x06. This interface consists of the following three sets of signals:

- Serial Interface
- Interrupt from FT5x06 to the Host
- Wake-up Signal from the Host to FT5x06

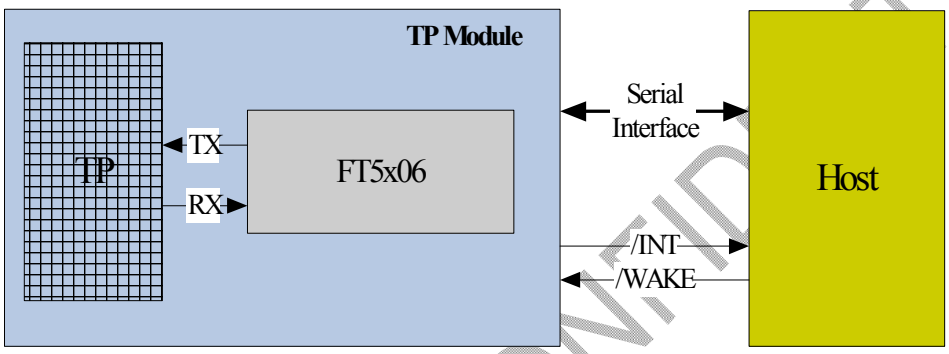


Figure 2-3 Host Interface Diagram

The serial interfaces of FT5x06 is I2C or SPI. The details of this interface are described in detail in Section 2.5. The interrupt signal (/INT) is used for FT5x06 to inform the host that data are ready for the host to receive. The /WAKE signal is used for the host to wake up FT5x06 from the Hibernate mode. After exiting the Hibernate mode, FT5x06 shall enter the Active mode.

2.4 Serial Interface

FT5x06 supports the I2C or SPI interfaces, which can be used by a host processor or other devices.

2.4.1 I2C

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure 2-4.

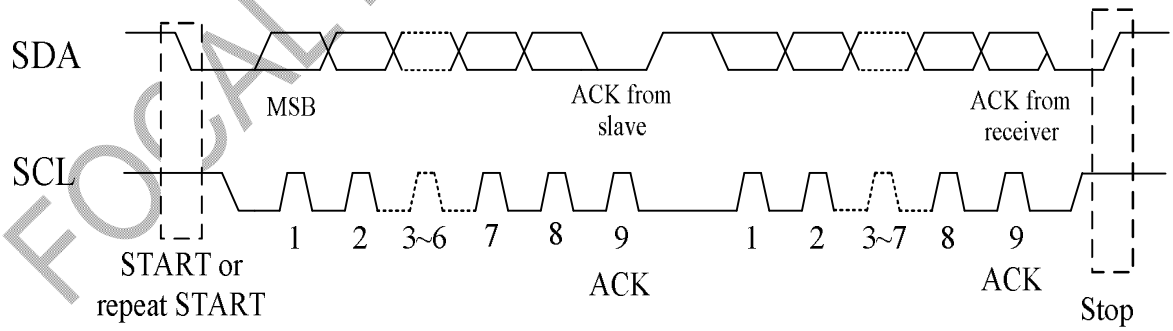


Figure 2-4 I2C Serial Data Transfer Format

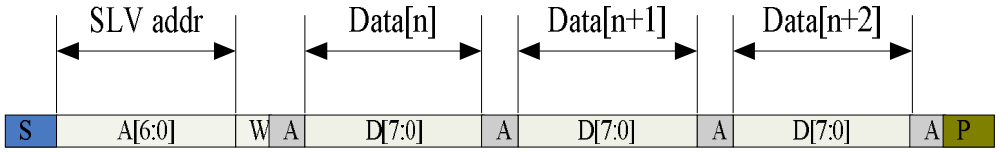


Figure 2-5 I2C master write, slave read

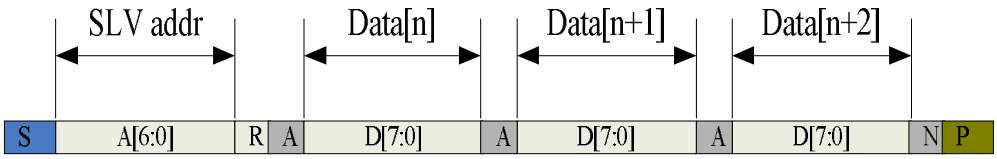


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address A[6:4]: 3'b011 A[3:0]: data bits are identical to those of I2CCON[7:4] register.
W	1'b0: Write
R	1'b1: Read
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Unit	Min	Max
SCL frequency	KHz	0	400
Bus free time between a STOP and START condition	us	4.7	\
Hold time (repeated) START condition	us	4.0	\
Data setup time	ns	250	\
Setup time for a repeated START condition	us	4.7	\
Setup Time for STOP condition	us	4.0	\

2.4.2 SPI

SPI is a 4 wire serial interface. The following is a list of the 4 wires:

- SCK: serial data clock
- MOSI: data line from master to slave
- MISO: data line from slave to master
- SLVESEL: active low select signal

SPI transfers data at 8bit packets. The phase relationship between the data and the clock can be defined by the two registers: phase and polck. Some data transfer examples can be found in Figure 2-7 to Figure 2-10.

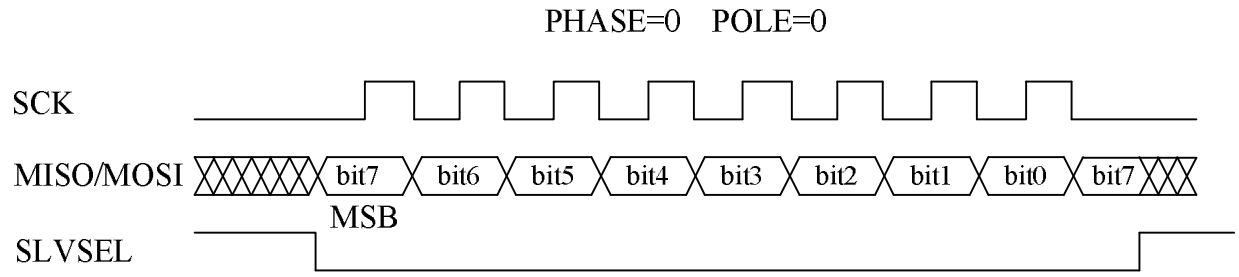


Figure 2-7 SPI Data Transfer Format (Phase=0, POLCK=0)

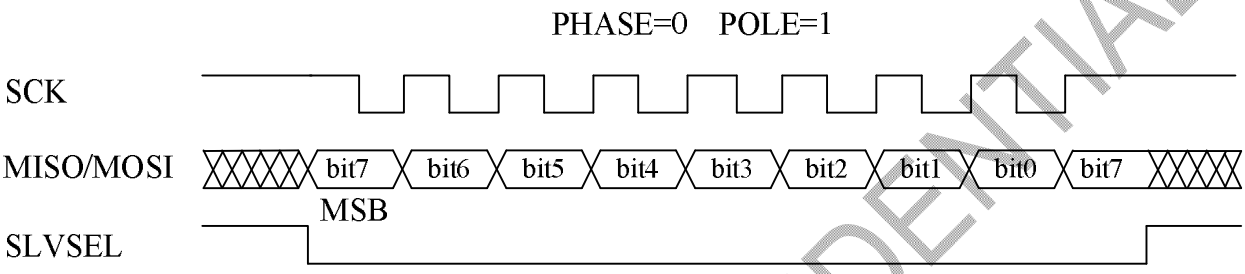


Figure 2-8 SPI Data Transfer Format (PHASE=0, POLCK=1)

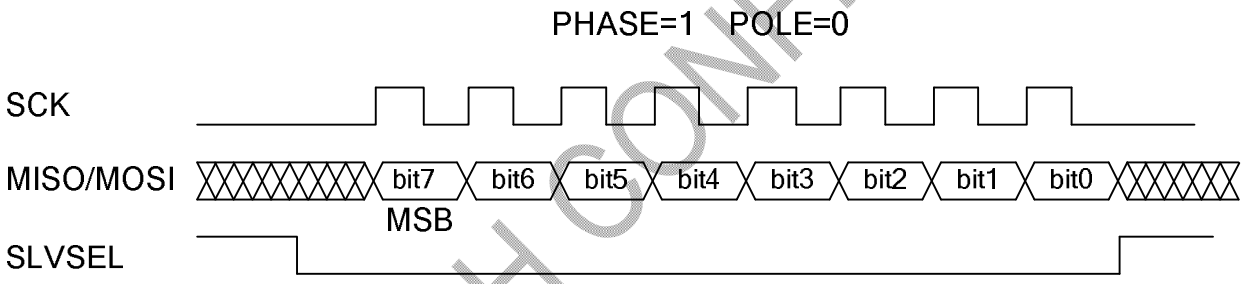


Figure 2-9 SPI Data Transfer Format (Phase=1, POLCK=0)

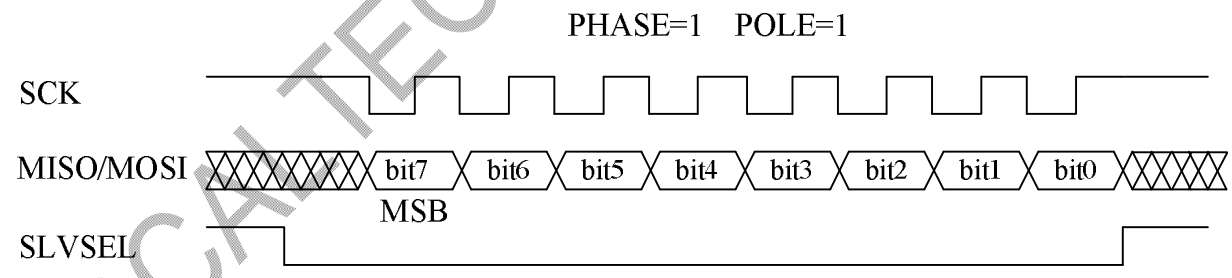


Figure 2-10 SPI Data Transfer Format (Phase=1, POLCK=1)

SPI can be configured into either Master or Slave mode via the MAS bit of the SPI0CON register. When in the Master mode, the SPI needs to supply the data clock, whose frequency relationship with the Master clock can be set by CLKDVD bits of the SPI0CON register. When it is configured in the Slave mode, the clock, SCK, is supplied by the external Master. The maximum data clock frequency must not be higher than $\frac{F_{mclk}}{8}$.

SPI Interface Timing Characteristics is shown in the following Figure2-11,Figure2-12, Figure2-13, Figure2-14 and Table 2-3.

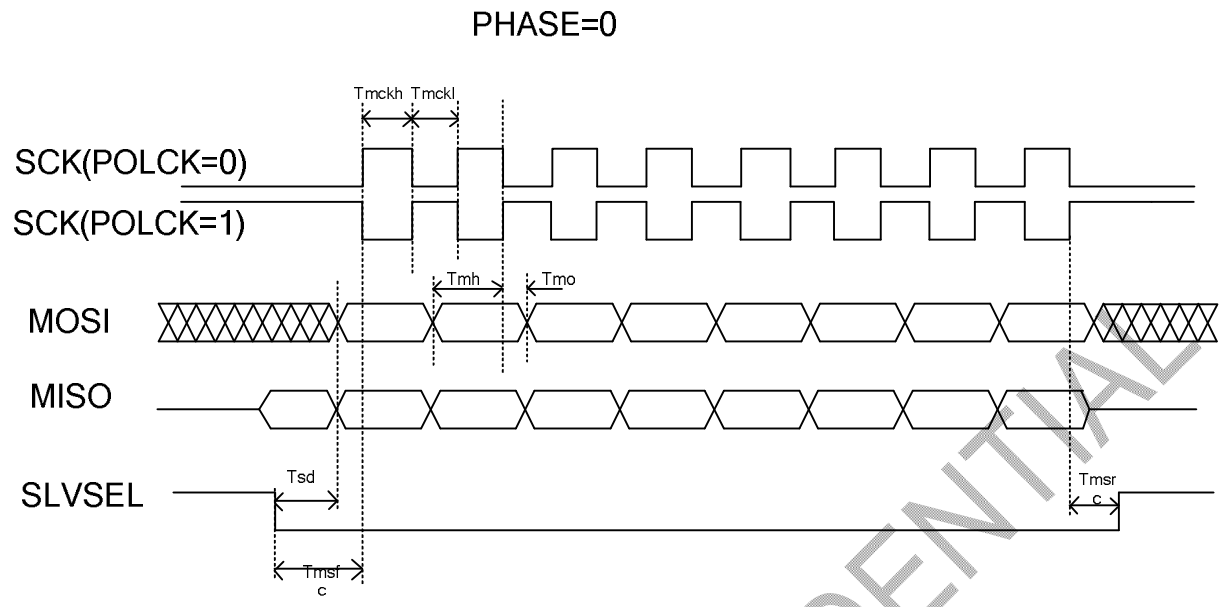


Figure 2-11 SPI master Timing PHASE =0

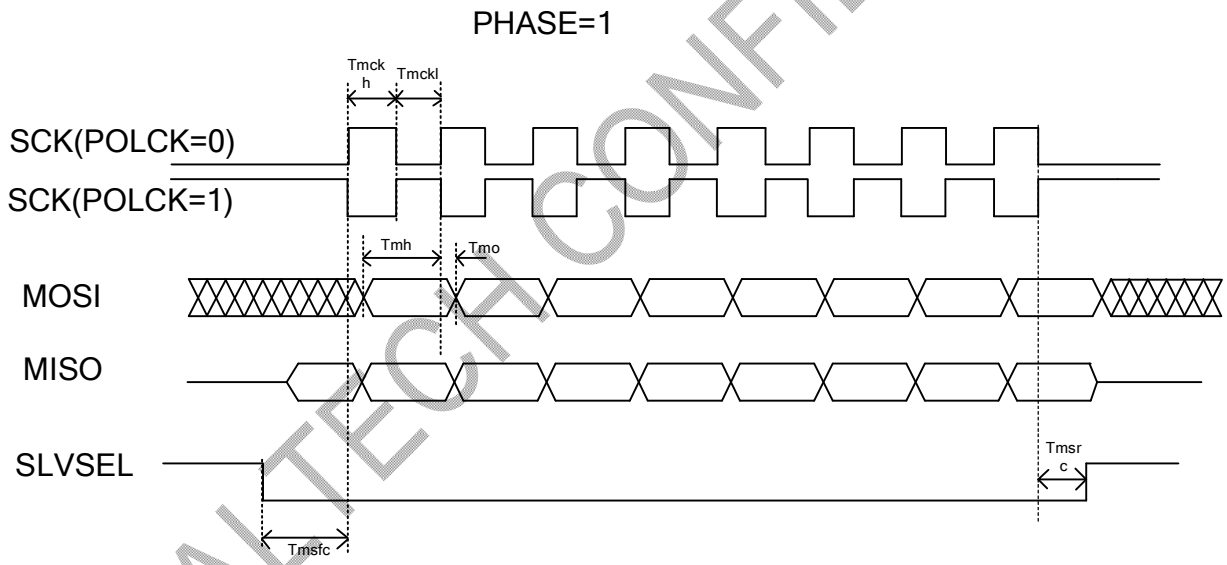


Figure 2-12 SPI master Timing PHASE =1

PHASE=0

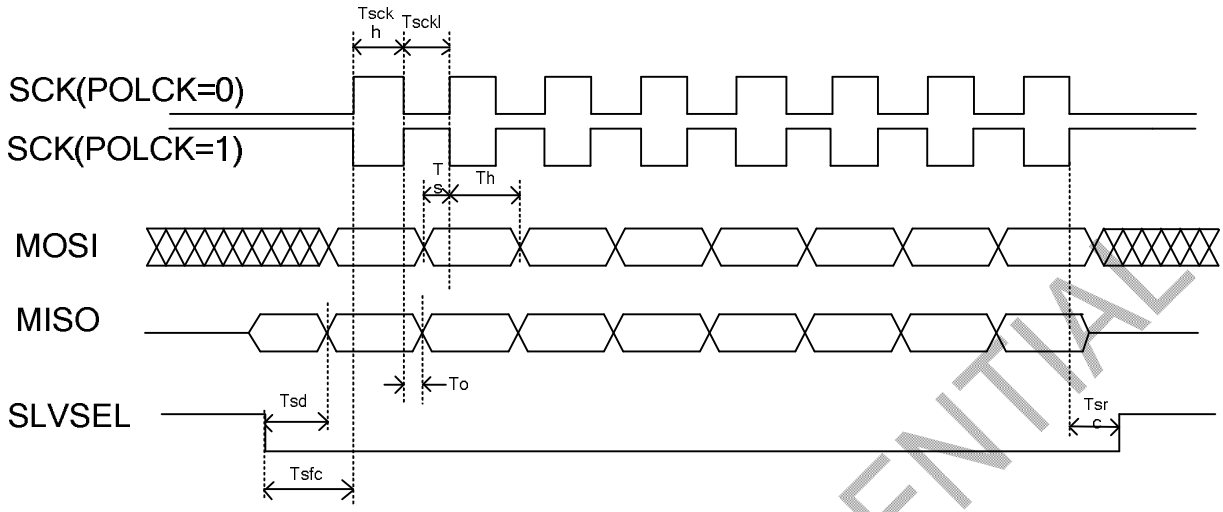


Figure 2-13 SPI slave Timing PHASE = 0

PHASE=1

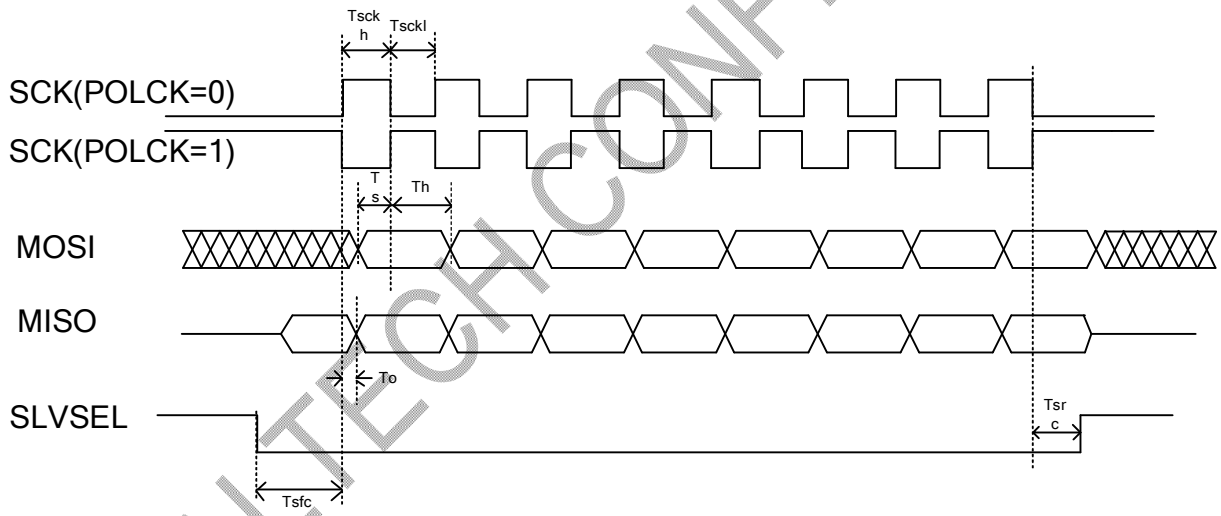


Figure 2-14 SPI slave Timing PHASE = 1

Table 2-3 SPI Timing Parameters

Parameter	Description	Min	Max	Units
Master Mode timing (see figure 2-11,2-12)				
Tmckh	sck high time	4×Tsysclk	--	ns
Tmckl	sck low time	4×Tsysclk	--	ns
Tmo	sck shift edge to mosi data change	0	--	ns
Tmh	mosi data valid to sck shift edge	3×Tsysclk	--	ns
Tsd	slvsel falling edge to mosi data valid	4×Tsysclk	--	ns
Tmsfc	slvsel falling edge to first sck edge	(Tmckh+Tmckl)/2	--	ns
Tmsrc	last sck edge to slvsel rising edge	(Tmckh+Tmckl)/2	--	ns
Slave mode timing(See figure 2-13,2-14)				

Tsckh	sck high Time	4×Tsysclk	--	ns
Tsckl	sck low Time	4×Tsysclk	--	ns
Tsd	slvsel falling edge to Miso valid data time	0	4xTsysclk	ns
Ts	Mosi Data valid to sck sample edge	0	--	ns
Th	sck sample edge to Mosi data change	4×Tsysclk	--	ns
To	sck shift edge to Miso data change	0	4xTsysclk	ns
Tsfc	slvsel falling edge to first sck edge	4×Tsysclk	--	ns
Tsrc	last sck edge to slvsel rising edge	4×Tsysclk	--	ns
*Tsysclk is equal to one period of the device system clock				

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VDDA - VSSA	V	-0.3 ~ +3.6	1, 2
Power Supply Voltage 2	VDD3 – VSS	V	-0.3 ~ +3.6	1, 3
I/O Power Supply Voltage	Vt	V	-0.3 ~ IOVCC + 0.3	1,4
Operating Temperature	Topr	℃	-20 ~ +85	1
Storage Temperature	Tstg	℃	-55 ~ +150	1

Notes

1. If used beyond the absolute maximum ratings, FT5x06 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VDDA (high) ≥VSSA (low)
3. Make sure VDD (high) ≥VSS (low)
4. IOVCC is set to VDD3 or VDDD by software configuration.

3.2 DC Characteristics

Table 3-2 DC Characteristics (VDDA=VDD3=2.8~3.6V, Ta=-20~85℃)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.7 x IOVCC	--	IOVCC	
Input low -level voltage	VIL	V		-0.3	--	0.3 x IOVCC	
Output high -level voltage	VOH	V	IOH=-0.1mA	0.7 x IOVCC	--	--	
Output low -level voltage	VOL	V	IOH=0.1mA	--	--	0.3 x IOVCC	
I/O leakage current	ILI	μA	Vin=0~VDDA	-1	--	1	
Current consumption （Normal operation mode）	Iopr	mA	VDDA=VDD3 = 2.8V Ta=25℃ MCLK=24MHz	--	6	--	
Current consumption （Monitor mode）	Imon	mA	VDDA=VDD3 = 2.8V Ta=25℃ MCLK=24MHz	--	4	--	
Current consumption （Sleep mode）	Islp	mA	VDDA=VDD3 = 2.8V Ta=25℃ MCLK=24MHz	--	0.03	--	
Step-up output voltage	VDD5	V	VDDA=VDD3= 2.8V	5	5.25	5.5	
Power Supply voltage	VDDA VDD3	V		2.8	--	3.6	

3.3 AC Characteristics

Table 3-3 AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDD3 = 2.8V Ta=25℃	43	48	52	
OSC clock 2	fosc2	KHz	VDD3 = 2.8V Ta=25℃	29	32	36	

Table 3-4 AC Characteristics of TX & RX

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Note
TX acceptable clock	ftx	KHz		100	150	270	
TX output rise time	Ttxr	nS		--	20	--	
TX output fall time	Ttxf	nS		--	20	--	
RX input voltage	Trxi	V		1.2	--	1.6	

3.4 I/O Ports Circuits

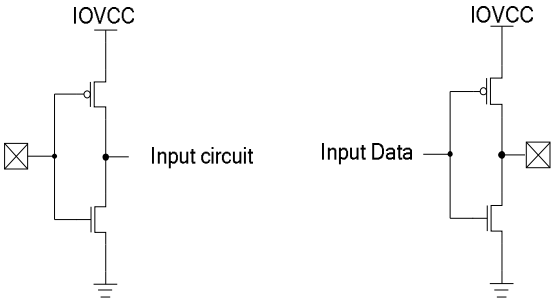


Figure 3-1 Digital Input & Output Port Circuits

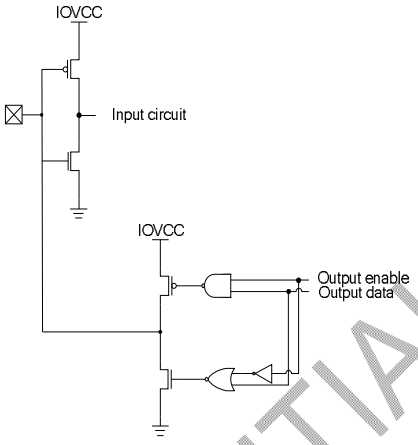


Figure 3-2 Digital In/Out Port Circuit

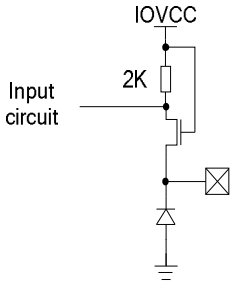


Figure 3-3 Reset Input Port Circuits

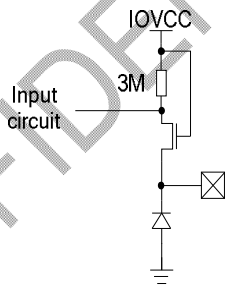


Figure 3-4 Wake Input Port Circuits

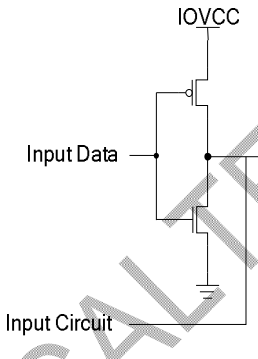


Figure 3-5 INT output Port Circuits

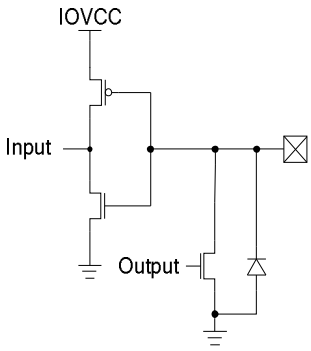


Figure 3-6 SCL/SDA Port Circuits

3.5 POWER ON/Reset/Wake Sequence

Reset and GPIO such as Wake, INT and I2C are advised to be low before powering on. The signal of waking up should be set to be high after powering on. INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Trst is more than 5ms.

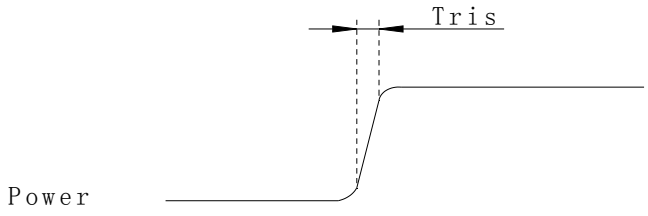


Figure 3-7 Power on time

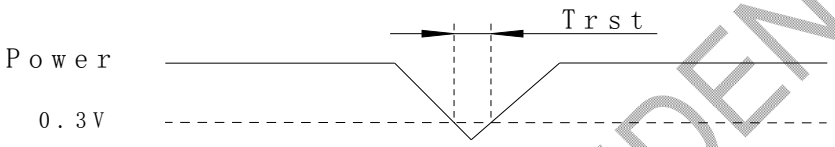


Figure 3-8 Power Cycle requirement

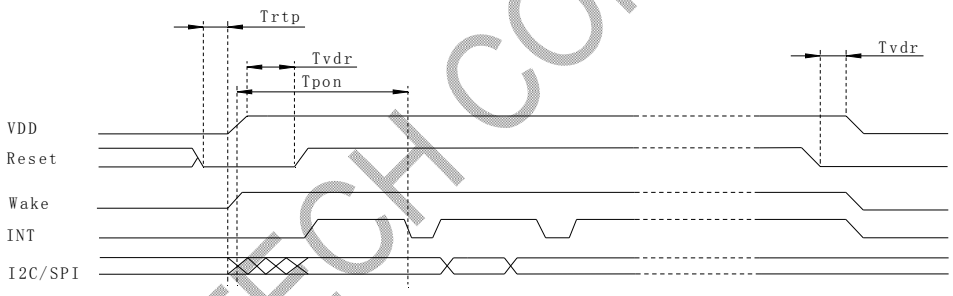


Figure 3-9 Power on / down Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

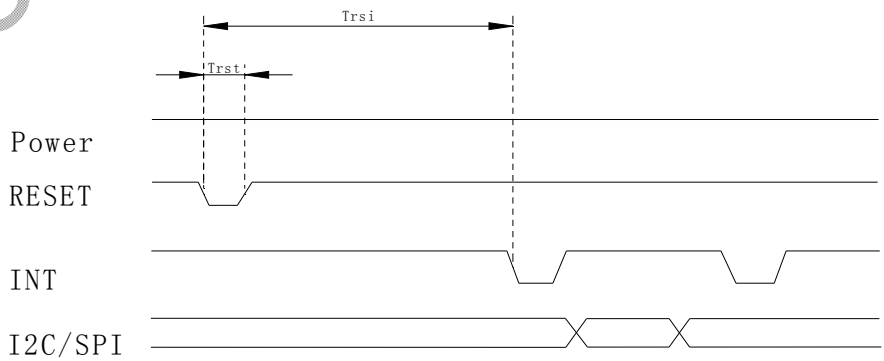


Figure 3-10 Reset Sequence

Wake time must be enough to wake up the system, the time of starting to report point after waking approach to the time of starting to report point after powering on

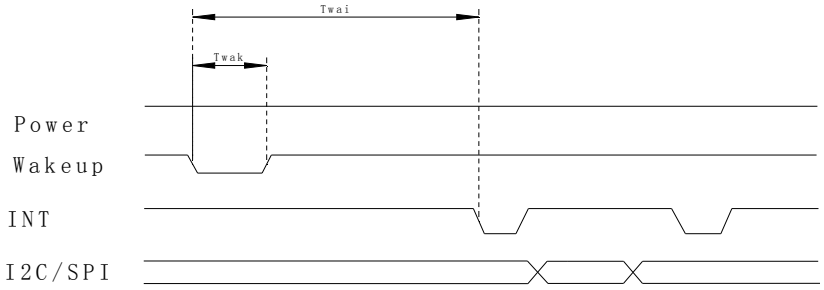


Figure 3-11 Wake Sequence

Table 3-5 Power on/Reset/Wake Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tpon	Time of starting to report point after powering on	400	--	ms
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	400	--	ms
Trst	Reset time	5	--	ms
Twai	Time of starting to report point after waking	300	--	ms
Twak	Wake up time	5	--	ms

4 PIN CONFIGURATIONS

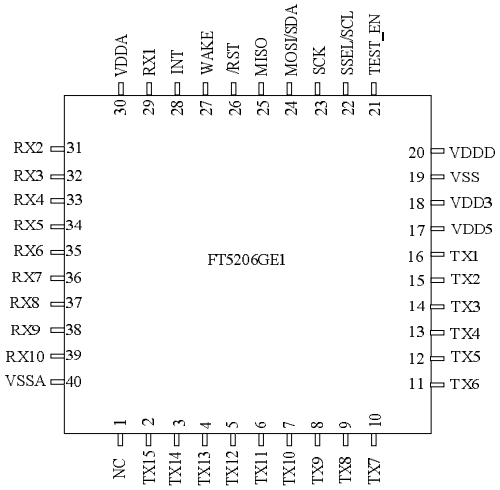
Pin List of FT5x06

Table 4-1 Pin Definition of FT5x06

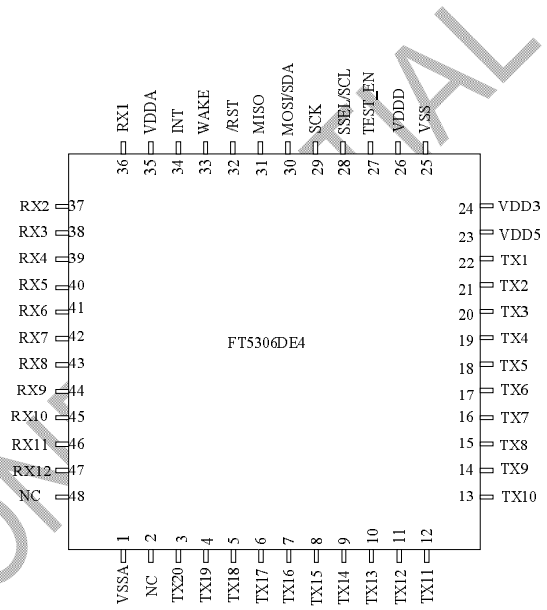
Name	Pin No.				Type	Description
	FT5206GE1	FT5306DE4	FT5406DQ9	FT5406EE8		
VSSA	40	1	56	1	PWR	Analog ground
NC	1	2		2		Not connected
NC		48		3		Not connected
TX28				4	O	Transmit output pin
TX27				5	O	Transmit output pin
TX26			1	6	O	Transmit output pin
TX25			2	7	O	Transmit output pin
TX24			3	8	O	Transmit output pin
TX23			4	9	O	Transmit output pin
TX22			5	10	O	Transmit output pin
TX21			6	11	O	Transmit output pin
TX20		3	7	12	O	Transmit output pin
TX19		4	8	13	O	Transmit output pin
TX18		5	9	14	O	Transmit output pin
TX17		6	10	15	O	Transmit output pin
TX16		7	11	16	O	Transmit output pin
TX15	2	8	12	17	O	Transmit output pin
TX14	3	9	13	18	O	Transmit output pin
TX13	4	10	14	19	O	Transmit output pin
TX12	5	11	15	20	O	Transmit output pin

TX11	6	12	16	21	O	Transmit output pin
TX10	7	13	17	22	O	Transmit output pin
TX9	8	14	18	23	O	Transmit output pin
TX8	9	15	19	24	O	Transmit output pin
TX7	10	16	20	25	O	Transmit output pin
TX6	11	17	21	26	O	Transmit output pin
TX5	12	18	22	27	O	Transmit output pin
TX4	13	19	23	28	O	Transmit output pin
TX3	14	20	24	29	O	Transmit output pin
TX2	15	21	25	30	O	Transmit output pin
TX1	16	22	26	31	O	Transmit output pin
VDD5	17	23	27	32	PWR	internal generated 5V power supply,A 1 μF ceramic capacitor to ground is required.
VDD3	18	24	28	33	PWR	Analog power supply
VSS	19	25	29	34	PWR	Analog ground
VDDD	20	26	30	35	PWR	Digital power supply (1.8V), generated internal. A 1 μF ceramic capacitor to ground is required.
TEST_EN	21	27	31	36	I	Test mode enabled at high and float in normal mode
GPIO0				37	I/O	General Purpose Input/Output port
GPIO1				38	I/O	General Purpose Input/Output port
GPIO2				39	I/O	General Purpose Input/Output port
GPIO3				40	I/O	General Purpose Input/Output port
SSEL/SCL	22	28	32	41	I/O	SPI Slave mode, chip select, active low / I2C clock input
SCK/GPIO	23	29	33	42	I	SPI Slave mode, clock input / General Purpose Input/Output port
MOSI/SDA	24	30	34	43	I/O	SPI Slave mode, data input / I2C data input and output
MISO	25	31	35	44	O	SPI Slave mode, data output
/RST	26	32	36	45	I	External Reset, Low is active
WAKE	27	33	37	46	I	External interrupt from the host
INT	28	34	38	47	O	External interrupt to the host
NC				48		Not connected
NC				49		Not connected
NC				50		Not connected
NC				51		Not connected
VDDA	30	35	39	52	PWR	Analog power supply
RX1	29	36	40	53	I	Receiver input pins
RX2	31	37	41	54	I	Receiver input pins
RX3	32	38	42	55	I	Receiver input pins
RX4	33	39	43	56	I	Receiver input pins
RX5	34	40	44	57	I	Receiver input pins
RX6	35	41	45	58	I	Receiver input pins
RX7	36	42	46	59	I	Receiver input pins
RX8	37	43	47	60	I	Receiver input pins
RX9	38	44	48	61	I	Receiver input pins

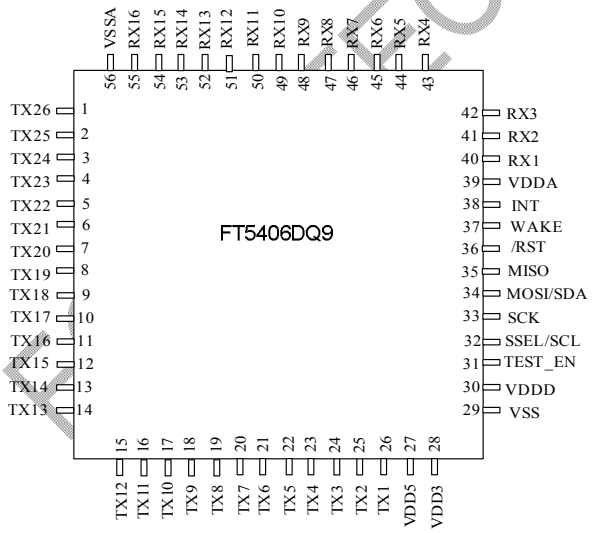
RX10	39	45	49	62	I	Receiver input pins
RX11		46	50	63	I	Receiver input pins
RX12		47	51	64	I	Receiver input pins
RX13			52	65	I	Receiver input pins
RX14			53	66	I	Receiver input pins
RX15			54	67	I	Receiver input pins
RX16			55	68	I	Receiver input pins



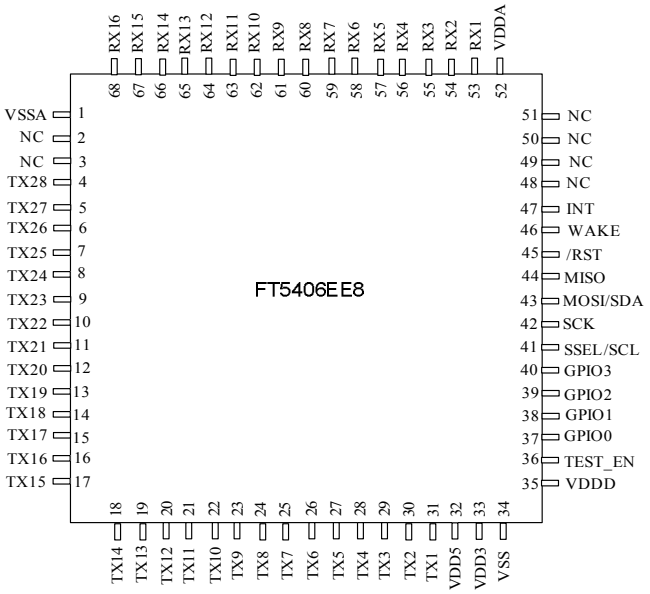
FT5206GE1 Package Diagram



FT5306DE4 Package Diagram



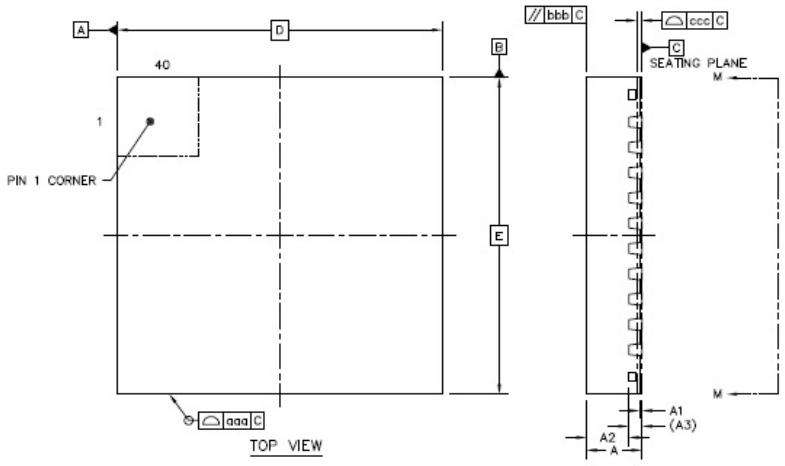
FT5406DQ9 Package Diagram



FT5406EE8 Package Diagram

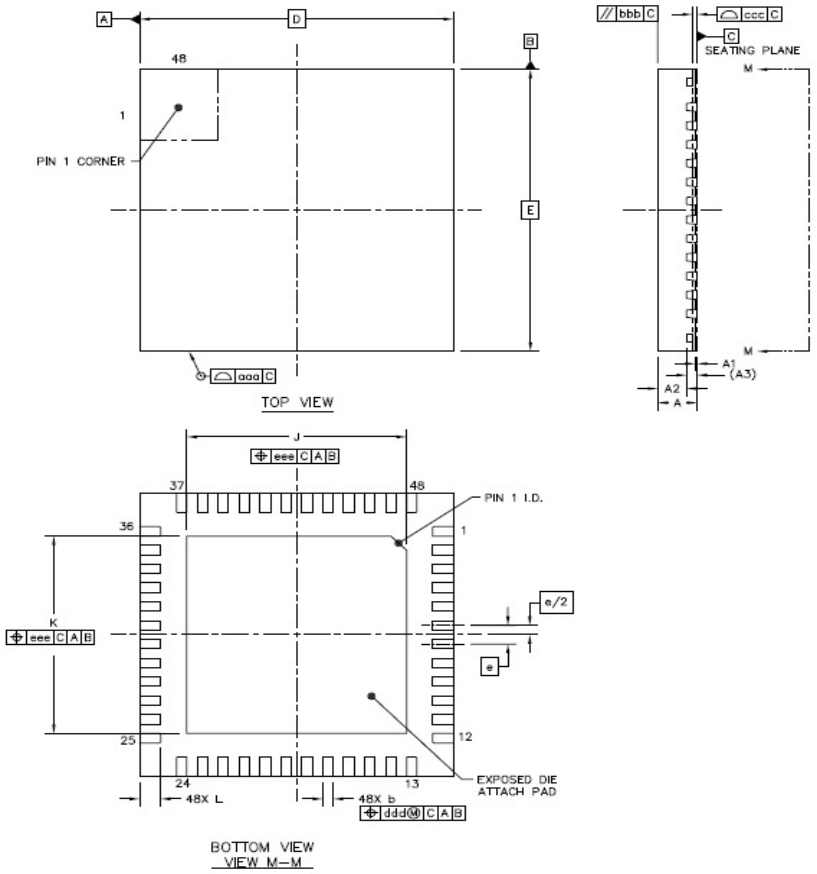
5 PACKAGE INFORMATION

5.1 Package Information of QFN-5x5-40L Package



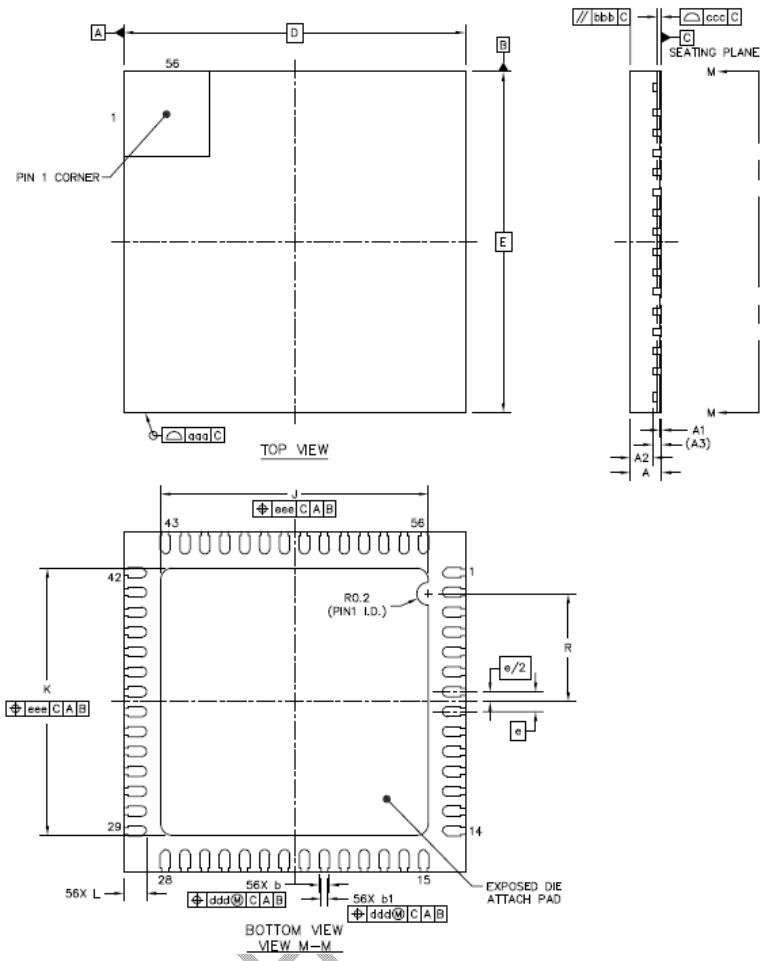
Item	Symbol	Millimeter		
		Min	Type	Max
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.55	0.57
L/F Thickness	A3		0.203 REF	
Lead Width	b	0.15	0.20	0.25
Body Size	D		5 BSC	
	E		5 BSC	
Lead Pitch	e		0.4 BSC	
EP Size	J	3.5	3.6	3.7
	K	3.5	3.6	3.7
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Co Planarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

5.2 Package Information of QFN-6x6-48L Package



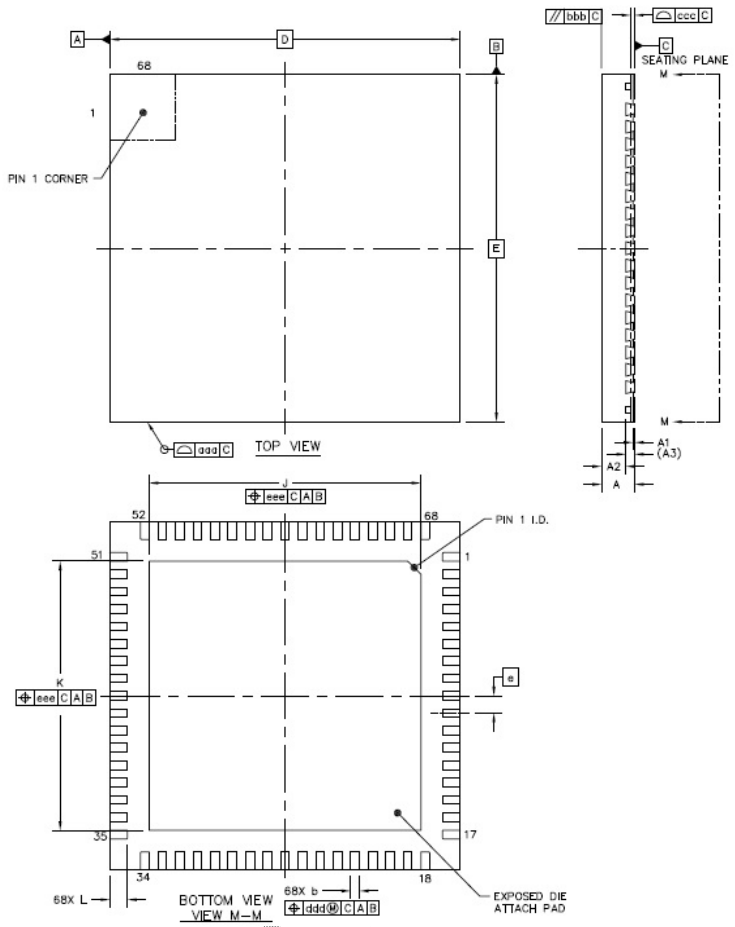
Item	Symbol	Millimeter		
		Min	Type	Max
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.55	0.57
L/F Thickness	A3		0.203 REF	
Lead Width	b	0.15	0.20	0.25
Body Size	D		6 BSC	
	E		6 BSC	
Lead Pitch	e		0.4 BSC	
EP Size	J	4.1	4.2	4.3
	K	4.1	4.2	4.3
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Co Planarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

5.3 Package Information of QFN-6x6-56L Package



Item Name	Symbol	Millimeter		
		Min	Type	Max
Total Thickness	A	0.5	0.55	0.6
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.4	----
L/F Thickness	A3		0.152 REF	
Lead Width	b	0.13	0.18	0.23
Body Size	D		6 BSC	
	E		6 BSC	
Lead Pitch	e		0.35 BSC	
EP Size	J	4.6	4.7	4.8
	K	4.6	4.7	4.8
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Coplanarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

5.4 Package Information of QFN-8x8-68L Package



Item Name	Symbol	Millimeter		
		Min	Type	Max
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.55	0.57
L/F Thickness	A3		0.203 REF	
Lead Width	b	0.15	0.20	0.25
Body Size	D		8 BSC	
	E		8 BSC	
Lead Pitch	e		0.4 BSC	
EP Size	J	6.1	6.2	6.3
	K	6.1	6.2	6.3
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Coplanarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

5.5 Order Information

Package Type	QFN
	40Pin(5 * 5)/48Pin(6 * 6)/56Pin(6 * 6)/68Pin (8 * 8)
	0.75 - P0.4/0.55 - P0.35
Product Name	FT5206GE1/ FT5306DE4/ FT5406DQ9/FT5406EE8

Note:

1). The last two letters in the product name indicate the package type and lead pitch and thickness.

2). The second last letter indicates the package type.
D : QFN-6*6 , **E** : QFN-8*8, **G** : QFN-5*5

3). The last letter indicates the lead pitch and thickness.
E : 0.75 - P0.4 , Q:0.55-P0.35

T: Track Code

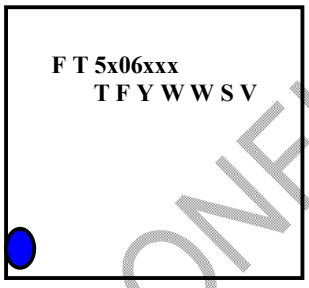
F/R:"F" for Lead Free process,
"R" for Halogen Free process

Y: Year Code

WW: Week Code

S: Lot Code

V：IC Version



Product Name	Package Type	# TX Pins	# RX Pins
FT5206GE1	QFN-40L	15	10
FT5306DE4	QFN-48L	20	12
FT5406DQ9	QFN-56L	26	16
FT5406EE8	QFN-68L	28	16

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