FSC-BW121

Bluetooth 4.2+WLAN 802.11 a/b/g/n/ac Module Datasheet

Version 1.5

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Revision History

Version	Data	Notes	
1.0	2019/02/20	Initial Version	Devin Wan
1.1	2019/04/28	1, Correction module and package image 2, The Notice about the stencil making 3, Add solder mask slivers next to the locating hole of the shield to prevent soldering tin from diffusing to the bonding pad on the back of the module.	Devin Wan
1.2	2020/03/14	Modify Bluetooth Features: Require external MCU to execute Bluetooth protocol stack	Devin Wan
1.3	2020/06/17	Modify the description and update the application circuit diagram (SDIO CLK line adds 5.6pF capacitor to ground)	Devin Wan
1.4	2020/07/21	Selection of version	Devin Wan
1.5	2020/12/03	Update selection of version	Devin Wan

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Contents

1. INTRODUCTION

Overview

FSC-BW121 is a Wi-Fi / Bluetooth combo module that support 1-stream 802.11ac solutions with Multi-user MIMO (Multiple-Input, Multiple-Output) STA mode with integrated Bluetooth Smart Ready controller, SDIO (SDIO 1.1/2.0/3.0) interface, and HS-UART mixed interface. It combines a WLAN MAC, a 1T1R capable WLAN baseband, and RF in s single chip. It provides a complete solution for a high-performance integrated wireless and Bluetooth device.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b, 802.11g and 802.11a data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability are available, and CCK provides support for legacy data rates, with long or short preamble. The high speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation of the individual subcarriers, and rate compatible coding rate of 1/2, 2/3, 3/4, and 5/6, provide up to 433.3Mbps for IEEE 802.11ac MIMO OFDM.

FSC-BW121 builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference.

FSC-BW121 supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control functions to obtain better performance in the analog portions of the transceiver.

FSC-BW121 MAC supports 802.11e for multimedia applications, 802.11i and WAPI (Wireless Authentication Privacy Infrastructure) for security, and 802.11n/802.11ac for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, U-APSD, and MIMO power saving reduce the power wasted during idle time, and compensate for the extra power required to transmit MIMO OFDM. FSC-BW121 provides simple legacy,

20MHz/40MHz/80MHz co-existence mechanisms to ensure backward and network compatibility.

FSC-BW121 Bluetooth controller complies with Bluetooth core specification v4.2, and supports dual mode (BR/EDR + Low Energy Controllers). It is compatible with previous versions, including v2.1 + EDR. For BR/EDR, it supports scatternet topology and allows active links in slave mode, and active links in master mode. For Low Energy, it supports multiple states and allows active links in master mode. The links in BR/EDR and LE can be active simultaneously.

General Features

- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/b/g/n/ac compatible WLAN

- Support 802.11ac 1x1,Wave-2 compliant with MU-MIMO STA mode

- Complete 802.11n MIMO solution for 2.4GHz and 5Ghz band

Host Interface

- Complies with SDIO 1.1/2.0/3.0 for WLAN with clock rate up to 100MHz (SDR50 and DDR50)

Standards Supported

- IEEE 802.11a/b/g/n/ac compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- IEEE 802.11h DFS, TPC, Spectrum Measurement

MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)

- Low latency immediate Block Acknowledgement (BA)

- Long NAV for media reservation with CF-End for NAV release

- Maximum PHY data rate up to 86.7Mbps using

20MHz bandwidth, 200Mbps using 40MHz bandwidth, and 433.3Mbps using 80MHz bandwidth.

- Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates

- Backward compatible with 802.11a/n devices while operating at 802.11ac data rates.

- G-SPI interface for configurable endian for WLAN

- Complies with HS-UART with configurable baud rate for Bluetooth

- IEEE 802.11k Radio Resource Measurement

- WAPI (Wireless Authentication Privacy Infrastructure) certified.

- Cisco Compatible Extensions (CCX) for WLAN devices

- PHY-level spoofing to enhance legacy compatibility

- MIMO power saving mechanism

- Channel management and co-existence

- PHY-level spoofing to enhance legacy compatibility

- MIMO power saving mechanism

- Channel management and co-existence

- Multiple BSSID feature allows the BW121 to assume multiple MAC identities when used as a wireless bridge

- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth

- WiFi Direct supports wireless peer to peer applications

Other Features

- Supports Wake-On-WLAN via Magic Packet and Wake-up frame

- Transmit Beam forming

PHY Features

- IEEE 802.11ac OFDM

- IEEE 802.11n OFDM

- One Transmit and One Receive path

- 5MHz / 10MHz / 20MHz / 40MHz / 80MHz bandwidth transmission

- Support 2.4Ghz and 5Ghz band channels

- Short Guard Interval (400ns)

- Sounding packet.

- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble

- OFDM with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6

- WiFi NAN (Neighborhood Area Network) support

- WiFi FTM (Fine Time Measurement) supported

- WiFi TDLS (Tunneled Direct Link Setup) Supported

- CCA on secondary through RTS/CTS handshake.

- Support TCP/UDP/IP checksum offload

- Generates 40MHz clock for peripheral chip.

- Single external power source 3.3V only

- Maximum data rate 54Mbps in 802.11g, 150Mbps in 802.11n and 433Mbps in 802.11ac.

- Switch diversity used for DSSS/CCK

- Support STBC receiving

- Support LDPC transmitting

- Hardware antenna diversity

- Fast receiver Automatic Gain Control (AGC)

- On-chip ADC and DAC

- Build-in both 2.4GHz and 5GHz PA

- Build-in both 2.4GHz and 5GHz LNA

Bluetooth Features

- Bluetooth 4.2 , Support Simultaneous LE & BR/EDR ,and High Duty Cycle Non-Connectable Advertising

- HS-UART interface for Bluetooth data transmission compliant with H4 and H5 specification

- PCM interface for audio data transmission via Bluetooth controller

- Require external MCU to execute Bluetooth protocol stack

- Supports all packet types in basic rate and enhanced data rate

Bluetooth Transceiver

- Fast AGC control to improve receiving dynamic range

- Integrated internal Class 1, Class 2, and Class 3 PA

- Supports Enhanced Power Control

Peripheral Interfaces

- Supports SCO/eSCO link (allows one link for PCM interface and three links for HS-UART)

- Supports Secure Simple Pairing

- Enhanced BT/WLAN Coexistence Control to improve transmission quality in different profiles

- Supports multiple Low Energy states

- Supports Bluetooth Low Energy

- Integrated 32K oscillator for power management

Application

- Internet-of-Things (IoT) Applications, including:
  - Home and Building Automation
  - Low-Power Video Cameras
  - Thermostats
  - Access Control and Electronic Locks (E-Locks)
  - Asset Tracking and Real Time Location System

(RTLS) Tags
  - Cloud Connectivity
  - Internet Gateway
  - Appliances
  - Security Systems
  - Smart Energy
  - Industrial Control
  - Smart Plug and Metering
  - Wireless Audio
  - IP Network Sensor Nodes
  - Medical Devices

- Car audio and video system
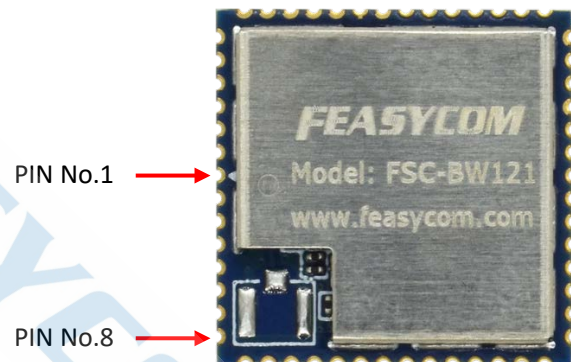
Module picture as below showing

PIN No.1

PIN No.8

Figure 1:   FSC-BW121 Picture

1.1   Selection of version

Order Number	Descriptions	Module picture as below showing
FSC-BW121 **(Default)**	PIN No.1 RF_IO_WIFI/BT PIN No.45 NC External antenna(stamp hole，PIN No.1)	
FSC-BW121B **(Optional)**	PIN No.1 NC PIN No.45 RF_IO_WIFI/BT External antenna(stamp hole，PIN No.45)	
FSC-BW121C **(Optional)**	PIN No.1 NC PIN No.45 NC External antenna (IPEX connector)	

🔷 *See chapter 3.2 for details*

2.   General Specification

Table 1: General Specifications

Categories	Features	Implementation
Bluetooth		
Bluetooth Standard		Bluetooth V4.2 LE & BR/EDR
Frequency Band		2402MHz~2480MHz
Interface		UART/PCM
WIFI		
WiFi Standard		802.11 a/b/g/n/ac
Frequency Band		2412MHz~2484MHz /4900MHZ~5925MHz
Interface		SDIO
General		

Size	17mm × 17 mm × 2.4mm
Operating temperature	-40°C ~+85°C
Storage temperature	-55°C ~+125°C
VDD_3V3_WL	3.0V~3.6V
VDD_IO	1.62V~3.6V
Miscellaneous	Lead Free	Lead-free and RoHS compliant
	Warranty	One Year
Humidity	10% ~ 90% non-condensing
MSL grade:	MSL 3
ESD grade:	Human Body Model: Pass ±2000 V, all pins Charge device model: Pass ±400 V, all pins

3.   HARDWARE   SPECIFICATION

3.1   Block Diagram and PIN Diagram
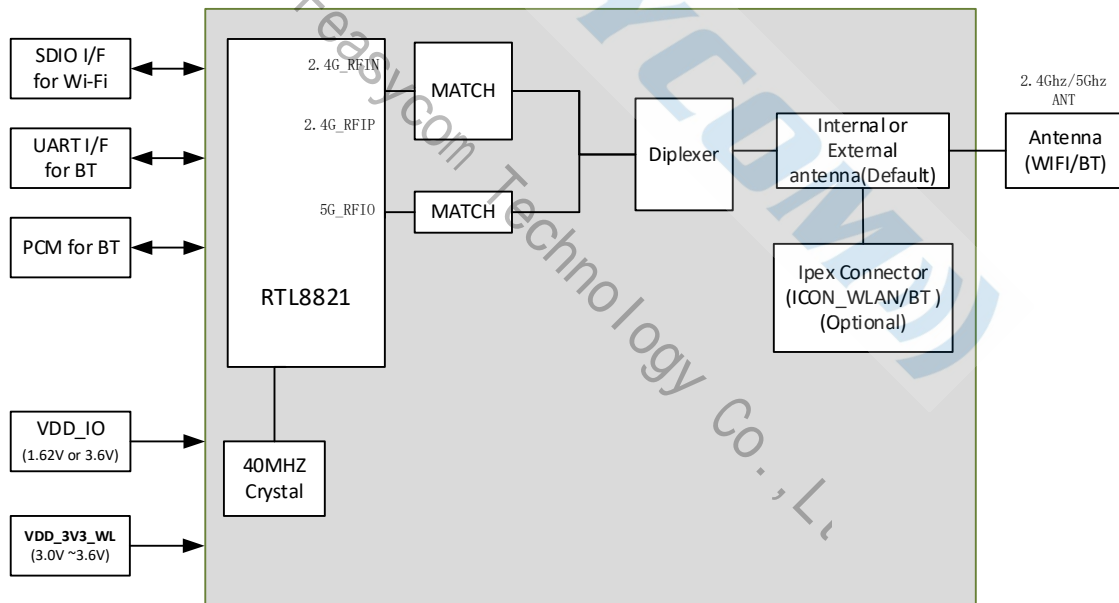
Figure 2: Block Diagram
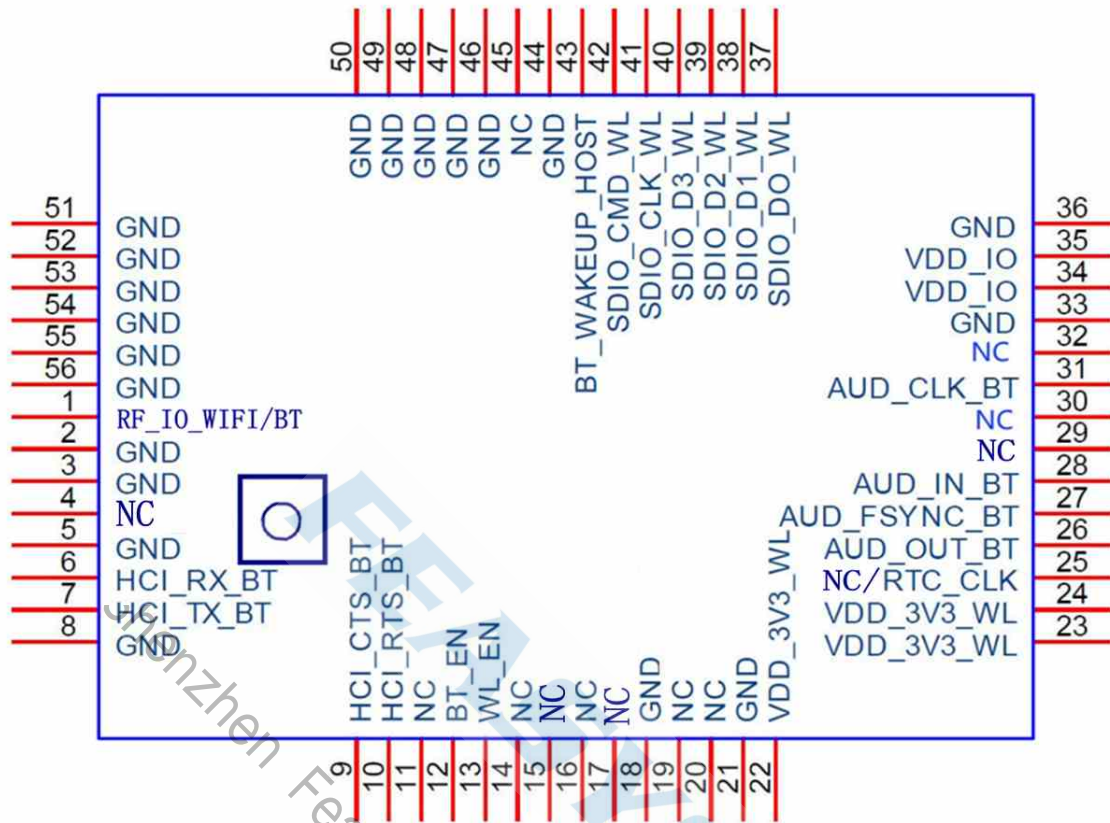
Figure 3: FSC-BW121 PIN Diagram(Top View)

3.2　PIN Definition Descriptions

Table 2: Pin definition

Pin	Pin Name	Type	Pin Descriptions	Notes
1	RF_IO_WIFI/BT	RF	WIFI 2.4G/5G RF and BT RF in/out port(FSC-BW121 only) ***No function （FSC-BW121B and FSC-BW121C only，）**	
2	GND		Ground	
3	GND		Ground	
4	NC			
5	GND		Ground	
6	HCI_RX_BT	I	High-Speed UART Data In	
7	HCI_TX_BT	O	High-Speed UART Data Out	
8	GND		Ground	
9	HCI_CTS_BT	I	High-Speed UART CTS	
10	HCI_RTS_BT	O	High-Speed UART RTS	
11	NC			
12	BT_EN	I	Bluetooth Function Enable(High Active)(BT_Reset)	
13	WL_EN	I	Wi-Fi Function Enable(High Active) (Wi-Fi_Reset)	
14	NC			
15	NC			

16	NC		
17	NC		
18	GND		Ground
19	NC		
20	NC		
21	GND		Ground
22	VDD_3V3_WL	PWR	3.3V Supply Voltage
23	VDD_3V3_WL	PWR	3.3V Supply Voltage
24	VDD_3V3_WL	PWR	3.3V Supply Voltage
25	NC/RTC_CLK	I	Sleep Clock(32.768kHz) *By default, this pin is not connected and is left floating.*
26	AUD_OUT_BT	O	BT PCM/I2S Bus. Data out ; NC if not used
27	AUD_FSYNC_BT	I	BT PCM/I2S Bus. Frame sync ; NC if not used.
28	AUD_IN_BT	I	BT PCM/I2S Bus. Data in ; NC if not used.
29	NC		
30	NC		
31	AUD_CLK_BT	I	BT PCM/I2S Clock; NC if not used.
32	NC		
33	GND		Ground
34	VDD_IO	PWR	1.8V~3.3V Supply Voltage
35	VDD_IO	PWR	1.8V~3.3V Supply Voltage
36	GND		Ground
37	SDIO_D0_WL	I/O	SDIO Data Line 0
38	SDIO_D1_WL	I/O	SDIO Data Line1
39	SDIO_D2_WL	I/O	SDIO Data Line 2
40	SDIO_D3_WL	I/O	SDIO Data Line 3
41	SDIO_CLK_WL	I	WLAN SDIO Clock. Must be driven by the host
42	SDIO_CMD_WL	I	SDIO Command Input
43	BT_WALEUP_HOST	O	Host wakeup Bluetooth; NC if not used.
44	GND		Ground
45	NC		No function (FSC-BW121 and FSC-BW121C only) *** WIFI 2.4G/5G RF and BT RF in/out port (FSC-BW121B only)*
46	GND		Ground
47	GND		Ground
48	GND		Ground
49	GND		Ground
50	GND		Ground
51	GND		Ground
52	GND		Ground
53	GND		Ground
54	GND		Ground
55	GND		Ground
56	GND		Ground

4. PHYSICAL INTERFACE

4.1 UART Interface

FSC-BW121 UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. The interface supports the Bluetooth UART HCI H4 and H5 specifications. The default baud rate is 115.2 kbaud. In order to support high and low speed baud rate, FSC-BW121 provides multiple UART clocks.

The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the UART interface via the VIO_HOST pin .

Table 3: Possible UART Settings

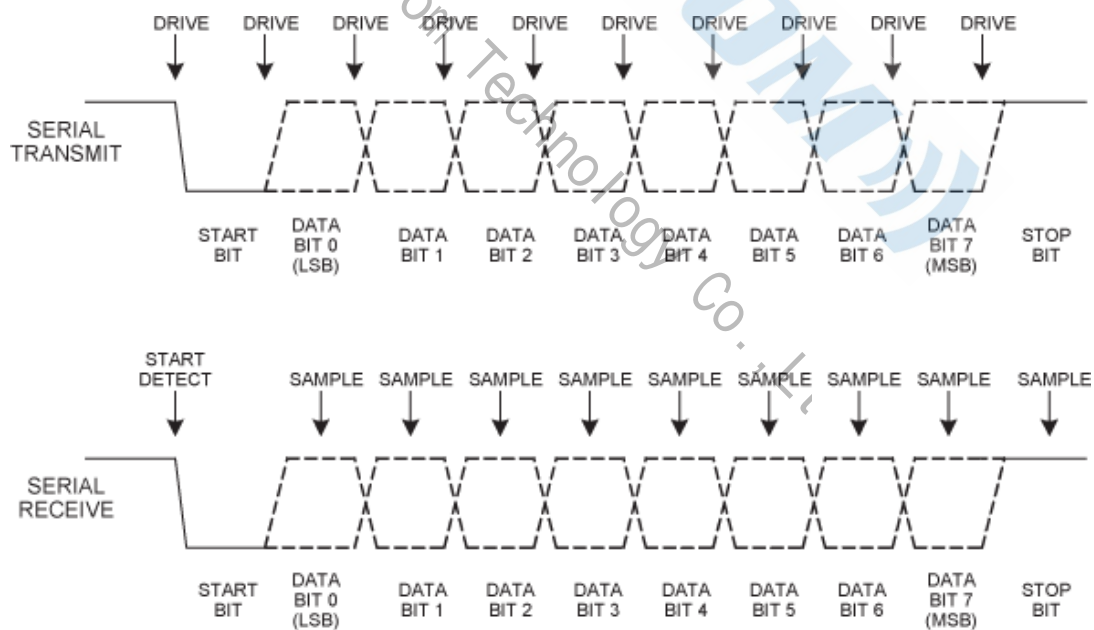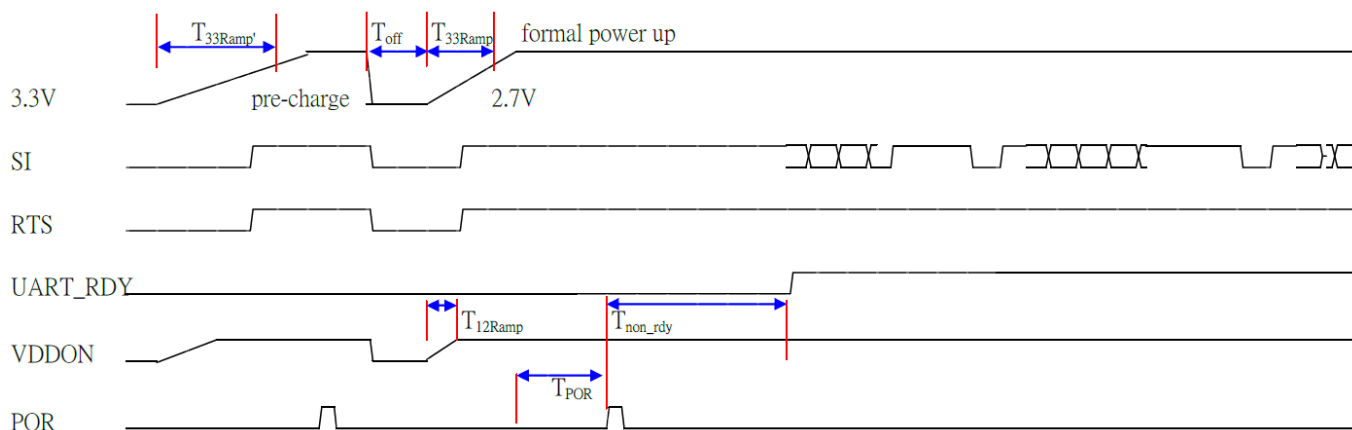| Parameter		Possible Values
Baudrate	Minimum	1200 baud (≤0%Error)
	Standard	115200bps(≤0.08%Error)
	Maximum	4Mbps(≤0%Error)
Flow control		Supports Automatic Flow Control (CTS and RTS lines)
Parity		None, Odd or Even
Number of stop bits		1
Bits per channel		8

Figure 4: UART Timing

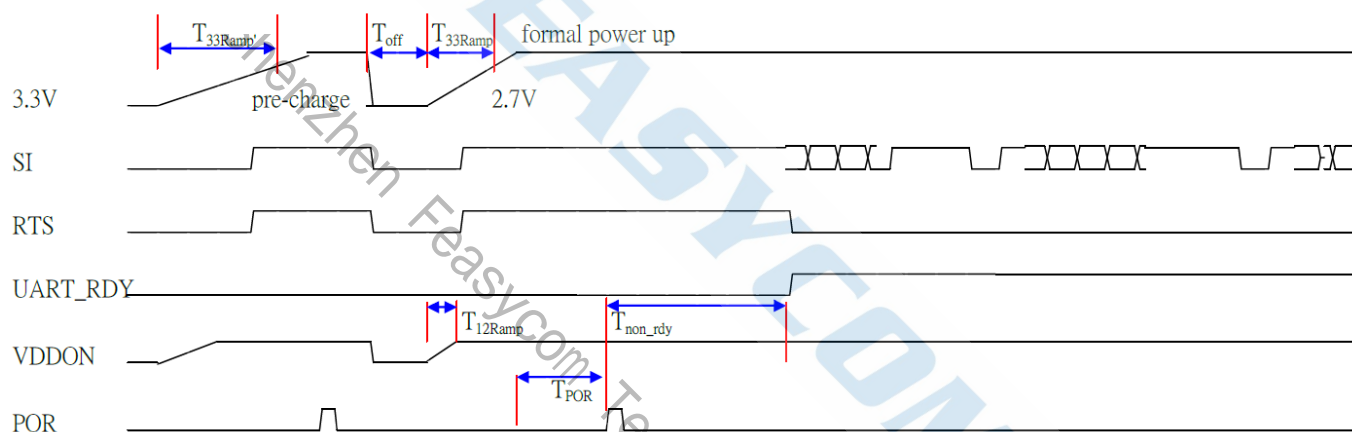**Figure 5:** UART Power-On Sequence Without Hardware Flow Control

Figure 6: UART Power-On Sequence Without Hardware Flow Control

Table 4: UART Interface Power-On Sequence

Symbol	Description
$T_{33ramp'}$	3.3V Power Pre-Charge Ramp Up Duration Before Formal Power Up. We recommend that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power on sequence. This procedure can eliminate host card detection issues when power ramp up duration is too long, or when a system warm reboot fails.
T_{off}	The duration 3.3V is cut off before formal power up.
T_{33ramp}	The 3.3V main power ramp up duration
T_{12ramp}	The internal 1.2V ramp up duration.
T_{POR}	The duration from when the power-on reset releases and the power management unit executes power on tasks. A power on reset will detect both 3.3V and 1.2V power ramp up after a predetermined duration.
T_{non_rdy}	UART Not Ready Duration. In this state, the RTL8821CS will not respond to any commands.

We recommend that the card detection procedures are divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.

During the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V power is cut off and is turned on after the T_{off} period. The ramp up time is specified in the T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the Bluetooth block. The Bluetooth firmware then initializes all circuits, included the UART. In addition to wait the T_{non_rdy} time, if the host supports UART hardware flow control it can detect RTS signals and follow the formal UART flow control handshake.

Table 5: UART Interface Power On Timing Parameters

Parameter	Min	Type	Max	Unit
T_{33ramp}	-	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{POR}	2	2	8	ms
T_{non-rd}	1	2	10	ms

4.2 Bluetooth PCM Interface

FSC-BW121 supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit A-law/μ-law, and 13/16-bit linear PCM formats
- Supports sign-extension and zero-padding for 8-bit and 13-bit samples
- Supports padding of Audio Gain to 13-bit samples
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports SCO/ESCO link

The PCM signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the PCM interface via the VDD-IO pin .
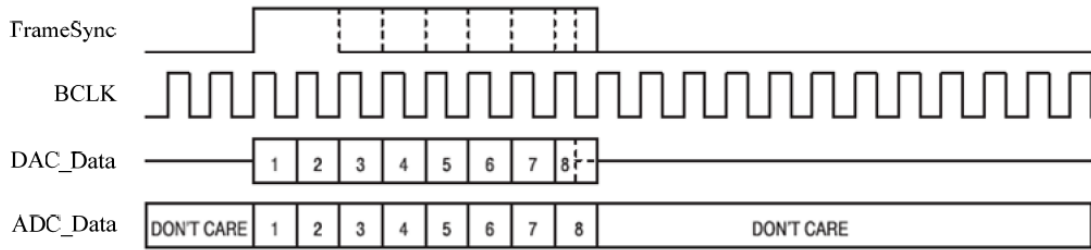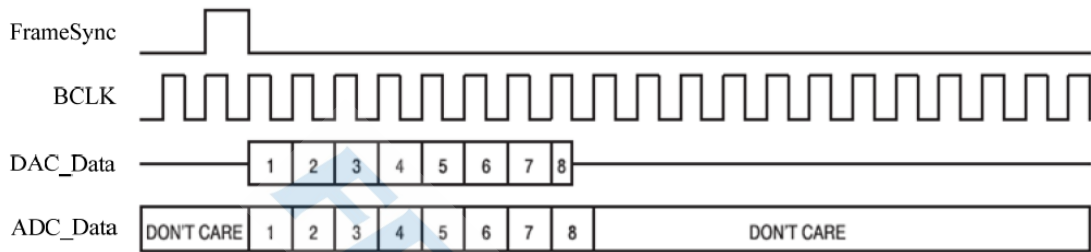
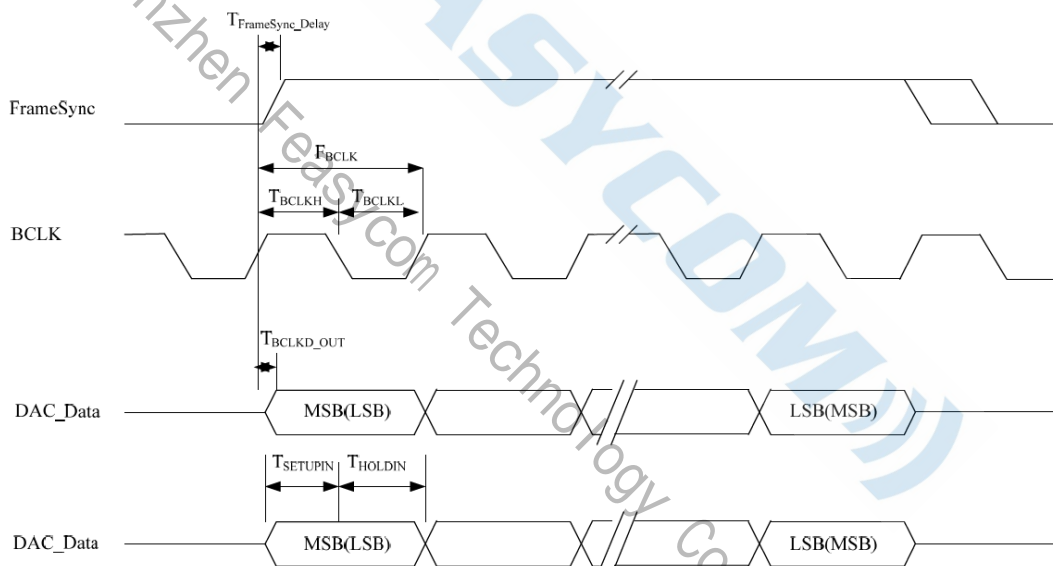**Figure 7:** PCM Long FrameSync

Figure 8: PCM Short FrameSync

Figure 9: PCM interface timing (Long FrameSync)
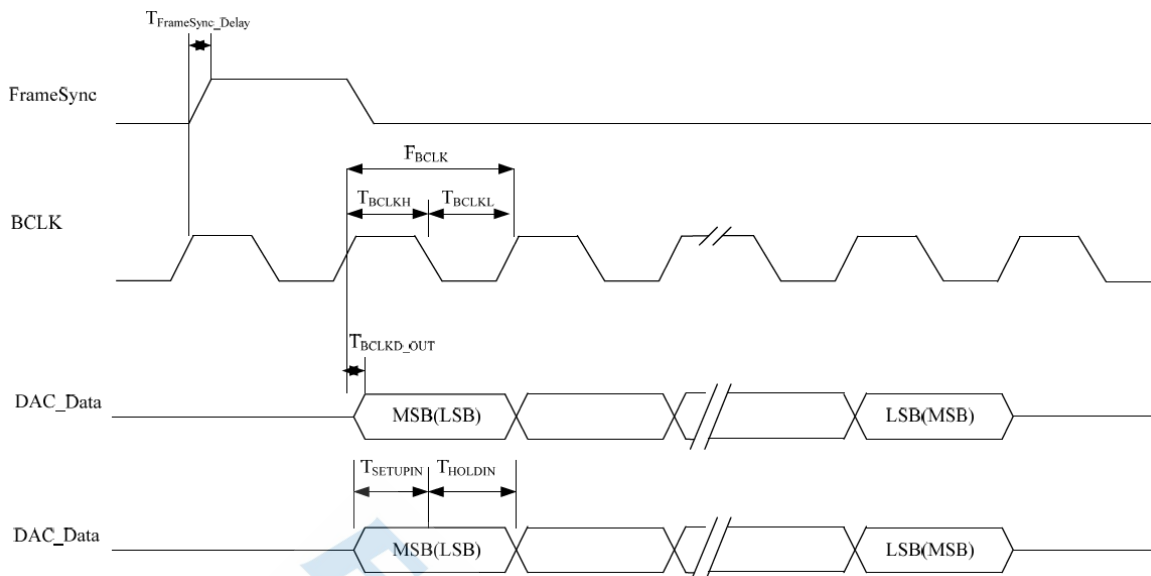
Figure 10: PCM interface timing (Short FrameSync)

Table 6: PCM Interface Clock Specifications

Parameter	Min	Type	Max	Unit
Frequency of BCLK (Master)	64	-	512	KHz
Frequency of Frame Sync (Master)	-	8	-	KHz
Frequency of BCLK (Slave)	64	-	512	KHz
Frequency of Frame Sync (Slave)	-	8	-	KHz
Data Size	8	8	16	KHz
Number of Slots Per Frame	1	1	1	Slots

Table 7: PCM interface timing

Parameter	Min	Type	Max	Unit
High Period of BCLK	980	-	-	ns
Low Period of BCLK	970	-	-	ns
Delay Time from BCLK High to Frame Sync High	-	-	75	ns
Delay Time from BCLK High to Valid DAC_Data	-	-	125	ns
Set-up Time for ADC_Data Valid to BCLK Low	10	-	-	ns
Hold Time for BCLK Low to ADC_Data Invalid	125	-	-	ns

4.3   I2S Interfaces

FSC-BW121 supports I2S digital audio interface used for transmitting digital audio/voice data to/from Audio Codec. The Interface shares the same pins with PCM interface, but mutually exclusive in its stage.There are features supported by RTL8821CS:

- Support both Master and Slave mode

- Programmable MSB/LSB bit 1st SCK(Left-Justified) or 2nd SCK(I2S-Compatible) latch time

- Programmable SCK rising/falling edge trigger for latching data bits Support 8-bit a-Law/u-Law and 16-bit linear formats

- Support sign-extension and zero-padding for 8-bit and 13-bit samples

- Support padding of Audio Gain to 13-bit samples

- Programmable MSB/LSB first

- I2S Master clock output: 128/256kHz

- Support one SCO/ESCO link only

FSC-BW121 can be configured as either master or slave mode. As master mode, the RTL8821CS generate SCK and WS, thus controls the data transfer over DAC_Data and ADC_Data. RTL8821CS supports audio sampling rate 8kHz(FrameSync), depends on I2S data format. The clock output(SCK) will be up to 256kHz.

In slave mode, RTL8821CS responds with DAC_Data and ADC_Data to SCK and WS it receives from Audio Codec. RTL8821CS can receive audio sampling rate 8kHz(WS), depends on I2S data format. The clock input(BCLK) accepted will be up to 256kHz.

FSC-BW121 supports audio sampling rate 8kHz(WS), depends on the I2S data format, in Master mode the clock output(SCK) will be 128, 256kHz.

Table 8: I2S Interface Clock Specifications

Parameter	Min	Type	Max	Unit
Frequency of SCK (Master)	128	-	256	KHz
Frequency of Frame WS (Master)	-	8	-	KHz
Frequency of SCK (Slave)	128	-	256	KHz
Frequency of Frame WS (Slave)	-	8	-	KHz
Data Size	8	8	16	KHz
Number of Slots Per Frame	1	1	1	Slots

Table 9: I2S interface timing

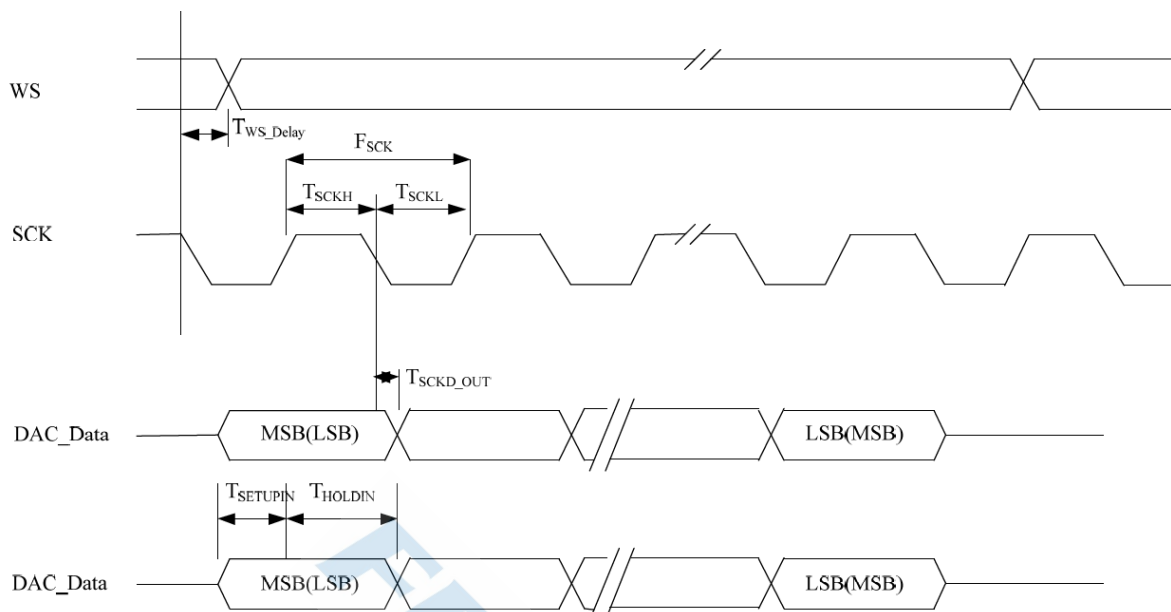| Parameter	Min	Type	Max	Unit
High Period of SCK	1960	-	-	ns
Low Period of SCK	1950	-	-	ns
Delay time from SCK falling to WS high/low	-	-	75	ns
Delay time from SCK falling to valid DAC_Data	-	-	125	ns
Set-up time for ADC_Data valid to SCK rising	10	-	-	ns
Hold time for SCK rising to ADC_Data invalid	125	-	-	ns

Figure 11: I2S interface timing

4.4   WLAN Host Interfaces

4.4.1   SDIO V3.0

The module WLAN section supports SDIO version 3.0, including the new UHS-I modes:

- DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes (3.3V signaling).

- HS: High speed up to 50 MHz (3.3V signaling).

- SDR12: SDR up to 25 MHz (1.8V signaling).

- SDR25: SDR up to 50 MHz (1.8V signaling).

- SDR50: SDR up to 100 MHz (1.8V signaling).

- SDR104: SDR up to 208 MHz (1.8V signaling).

- DDR50: DDR up to 50 MHz (1.8V signaling).

Note: The RTL8821 is backward compatible with SDIO v2.0 host interfaces.

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided.

SDIO mode is enabled by strapping options. Refer to next Table WLAN GPIO Functions and Strapping Options.

The following three functions are supported:

- Function 0 Standard SDIO function (Max. BlockSize/ByteCount = 32B)

- Function 1 Backplane Function to access the internal system-on-chip (SoC) address space (Max.

BlockSize/ByteCount = 64B)

- Function 2 WLAN Function for efficient

Table 10: SDIO Pin Description

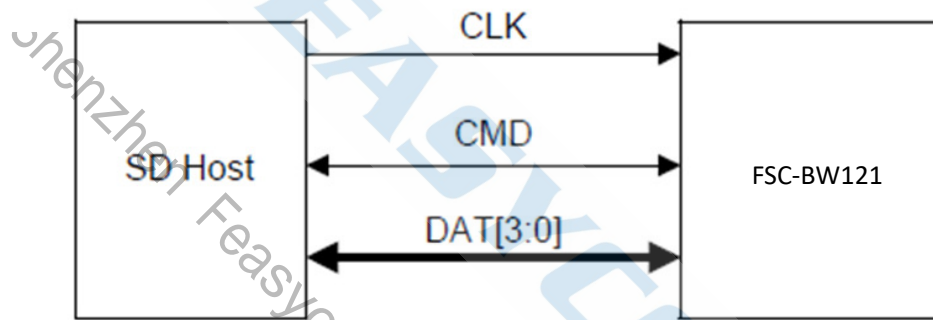| SD 4-Bit Mode	
DATA0	Data line 0
DATA1	Data line 1 or Interrupt
DATA2	Data line 2 or Read Wait
DATA3	Data line 3
CLK	Clock
CMD	Command line

Figure 12: Signal Connections to SDIO Host (SD 4-Bit Mode)
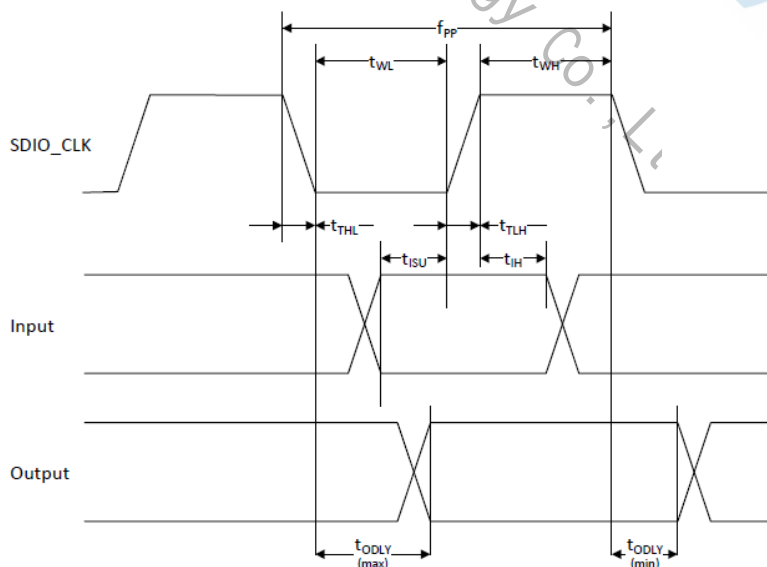
4.4.2 SDIO Default Mode Timing

Figure 13: SDIO Bus Timing (Default Mode)

Table 11: SDIO Bus Timing[a] Parameters (Default Mode)

Parameter	Min	Type	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])				
Frequency – Data Transfer mode	0	-	25	MHz
Frequency – Identification mode	0	-	400	KHz
Clock low time	10	-	-	ns
Clock high time	10	-	-	ns
Clock rise time	8	-	10	ns
Clock fall time	0	-	10	ns
Inputs: CMD, DAT (referenced to CLK)				
Input setup time	5	-	-	ns
Input hold time	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)				
Output delay time – Data Transfer mode	0	-	14	ns
Output delay time – Identification mode	0	-	50	ns

a. Timing is based on CL <= 40pF load on CMD and Data.

b. Min. (Vih) = 0.7 X VDDIO and max (Vil) = 0.2 X VDDIO.
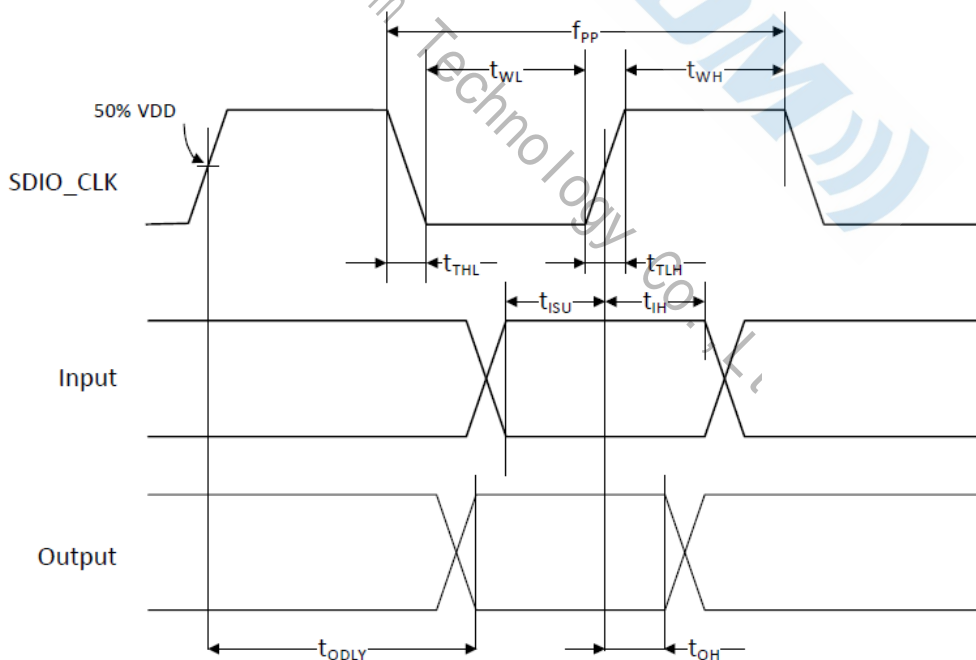
4.4.3 SDIO High-Speed Mode Timing

Figure 14: SDIO Bus Timing (Default Mode)

**Table 12:** SDIO Bus Timing[a] Parameters (High-Speed Mode)

Parameter		Min	Type	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode		0	-	50	MHz
Frequency – Identification mode		0	-	400	KHz
Clock low time		7	-	-	ns
Clock high time		7	-	-	ns
Clock rise time		-	-	3	ns
Clock fall time		-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time		6	-	-	ns
Input hold time		2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode		-	-	14	ns
Output hold time		2.5	-	-	ns
Total system capacitance (each line)		-	-	40	

a. Timing is based on CL <= 40pF load on CMD and Data.

b. Min. (Vih) = 0.7 X VDDIO and max (Vil) = 0.2 X VDDIO.

4.4.4   SDIO Bus Timing Specifications in SDR Modes
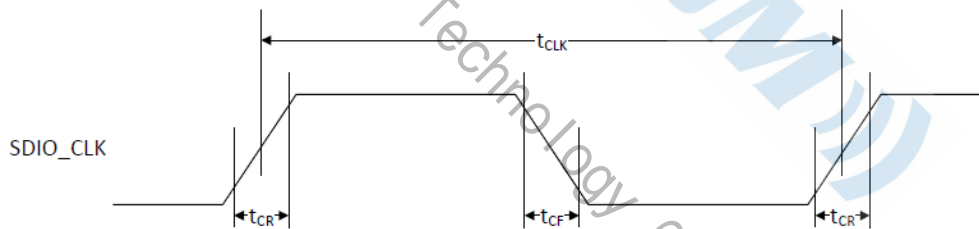
Figure 15: SDIO Clock Timing (SDR Modes)

Table 13: SDIO Bus Clock Timing Parameters (SDR Modes)

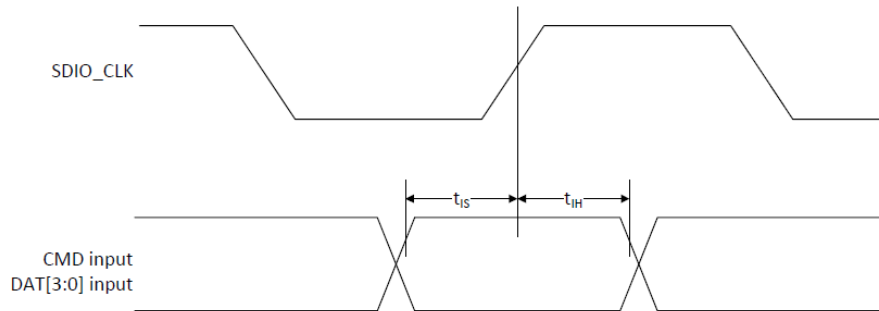| Parameter	Min	Type	Max	Unit	Unit
	40	-	-	ns	SDR12 mode
	20	-	-	ns	SDR25 mode
	10	-	-	ns	SDR50 mode
	4.8	-	-	ns	SDR104 mode
	-	-	3	ns	tCR, tCF < 2.00 ns (max.) @100 MHz, CCARD = 10 pF
					tCR, tCF < 0.96 ns (max.) @208 MHz, CCARD = 10 pF
Clock duty cycle	30	-	70	%	ns

4.4.5 Device Input Timing

Figure 16: SDIO Bus Input Timing (SDR Modes)

Table 14: SDIO Bus Input Timing Parameters (SDR Modes)

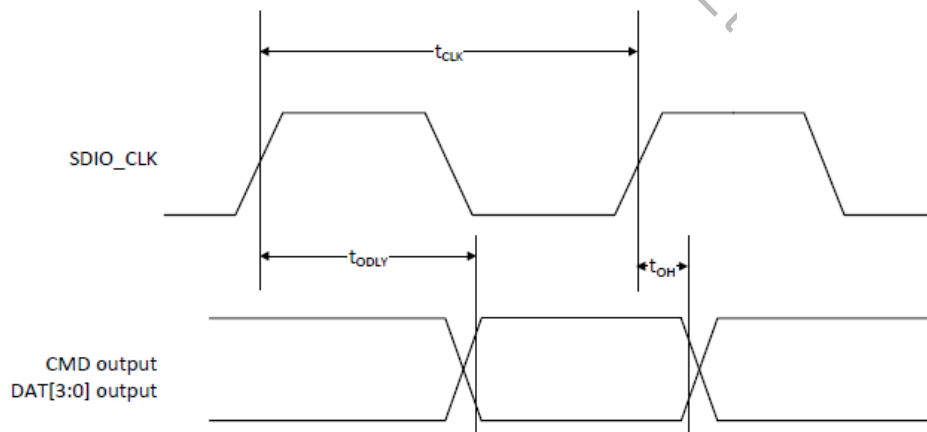| Symbol	Min	Type	Max	Unit	Unit
SDR104 Mode					
t_{IS}	1.4	-	-	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	-	-	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR50 Mode					
t_{IS}	3.0	-	-	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	-	-	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR25 Mode					
t_{IS}	3.0	-	-	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	-	-	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR12 Mode					
t_{IS}	3.0	-	-	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	-	-	ns	C_{CARD} = 5 pF, VCT = 0.975V

4.4.6 Device Output Timing

Figure 17: SDIO Bus Output Timing (SDR Modes up to 100MHz)

Table 15: SDIO Bus Output Timing Parameters (SDR Modes up to 100 MHz)

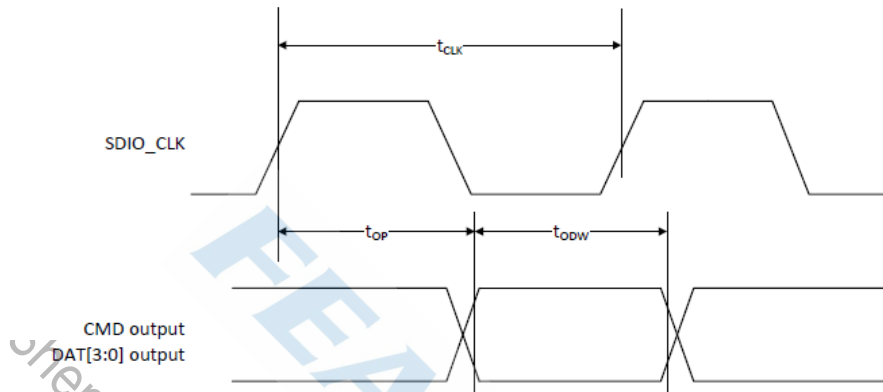| Symbol	Min	Type	Max	Unit	Unit
t_{ODLY}	-	-	7.5	ns	t_{CLK} ≥10 ns C_L= 30 pF using driver type B for SDR50
t_{ODLY}	-	-	14.0	ns	t_{CLK} ≥20 ns C_L= 40 pF using for SDR12, SDR25
T_{OH}	1.5	-	-	ns	Hold time at the t_{ODLY} (min) C_L= 15 pF

Figure 18: SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)

Table 16: SDIO Bus Output Timing Parameters (SDR Modes 100 MHz to 208 MHz)

Symbol	Min	Type	Max	Unit	Unit
t_{OP}	0	-	2	UI	Card output phase
Δt_{OP}	-350	-	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	-	-	UI	t_{ODW}=2.88 ns @208 MHz

- Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90 degrees during operation
- Δt_{OP} = −350 ps for junction temperature of Δt_{OP} = −20 degrees during operation
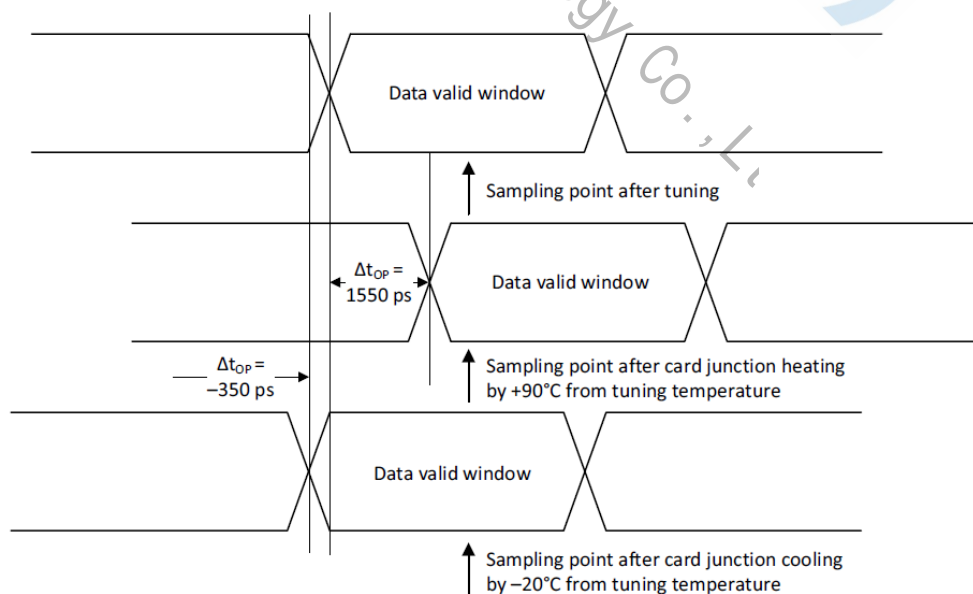- Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = −20 to +125 degrees during operation

Figure 19: ΔtOP Consideration for Variable Data Window (SDR 104 Mode)

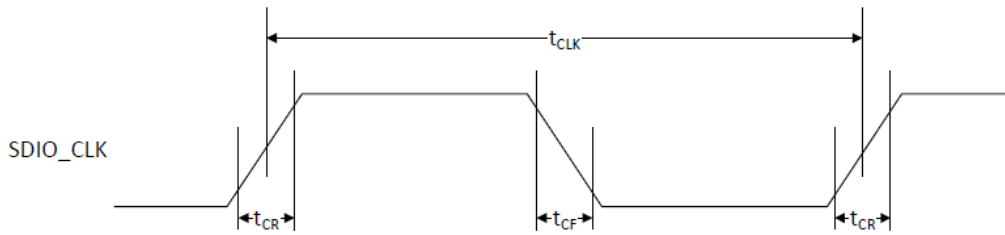## 4.4.7   SDIO Bus Timing Specifications in DDR50 Mode

Figure 20: SDIO Clock Timing (DDR50 Mode)

Table 17: SDIO Bus Clock Timing Parameters (DDR50 Mode)

Parameter	Min	Type	Max	Unit	Unit
	20	-	7.5	ns	DDR50 mode
	-	-	$0.2 \times t_{CLK}$	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty cycle	45	-	55	%	-

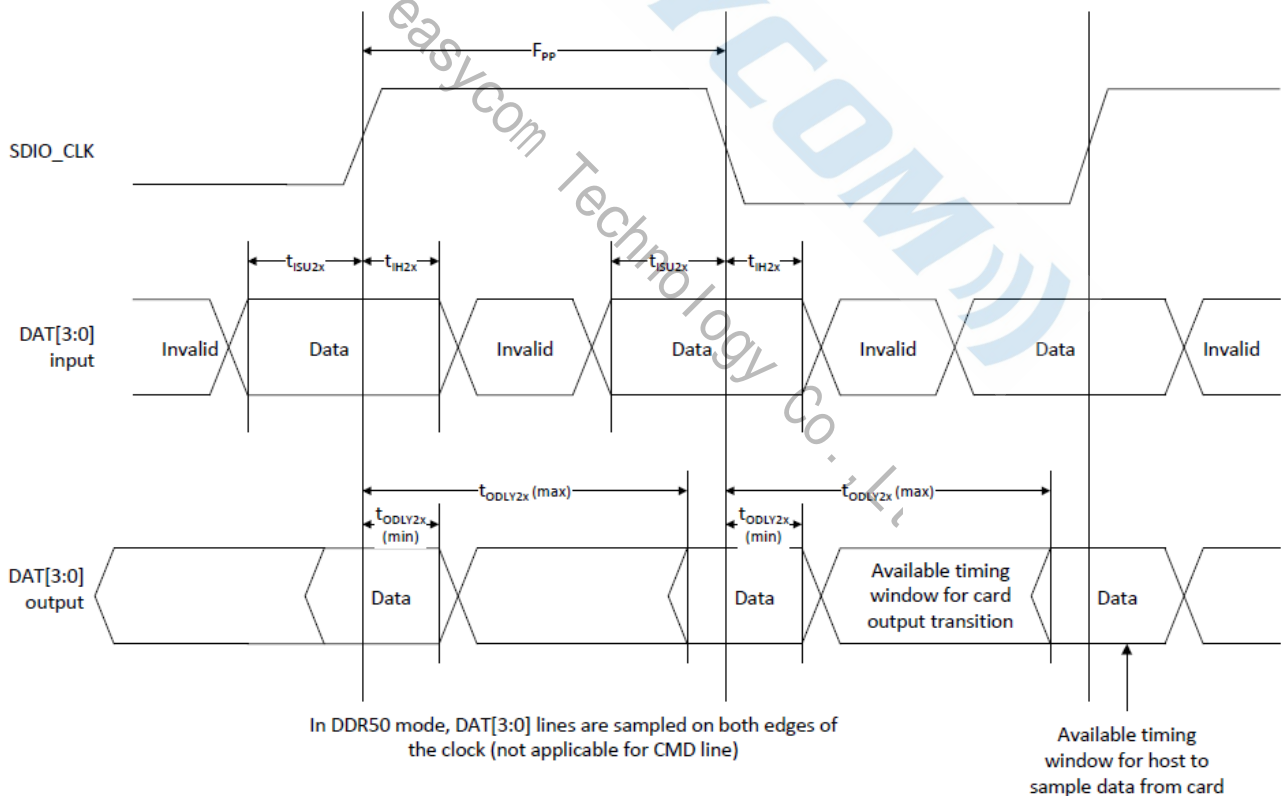In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line)

Figure 21: SDIO Data Timing (DDR50 Mode)

Table 18: SDIO Bus Timing Parameters (DDR50 Mode)

Parameter	Min	Type	Max	Unit	Comments
Input CMD					
Input setup time	6	-	-	ns	$C_{CARD} < 10pF$ (1 Card)
Input hold time	0.8	-	-	ns	$C_{CARD} < 10pF$ (1 Card)
Outputs CMD					
Output delay time	-	-	13.7	ns	$C_{CARD} < 30pF$ (1 Card)
Output hold time	1.5	-	-	ns	$C_{CARD} < 15pF$ (1 Card)
Input DAT					
Input setup time	3	-	-	ns	$C_{CARD} < 10pF$ (1 Card)
Input hold time	0.8	-	-	ns	$C_{CARD} < 10pF$ (1 Card)
Outputs DAT					
Output delay time	-	-	7.0	ns	$C_{CARD} < 25pF$ (1 Card)
Output hold time	1.5	-	-	ns	$C_{CARD} < 15pF$ (1 Card)

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

All measurements are referenced at the module pins unless otherwise indicated. All specifications are over process and voltage unless otherwise indicated.

Over operating free-air temperature range (unless otherwise noted)

Table 19: Absolute Maximum Rating

Parameter	Min	Max	Unit
VDD_3V3_WL(SWREG Supply Input)	-0.3	+3.6	V
VDD_IO(DC supply voltage for digital I/O)	-0.3	+3.6	V
Operating temperature (T_A)	-40	+85	°C
Storage temperature (T_{stg})	-55	+125	°C
Maximum junction temperature(T_j)		+125	°C

5.2 Recommended Operating Conditions

Table 20: Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
VDD_3V3_WL	3.0	3.3	3.6	V
VDD_IO	1.62	1.8~3.3	3.6	°C
Operating temperature (T_A)	-40	25	+85	°C
Storage temperature (T_{stg})	-55	25	+125	°C
High-level input voltage	0.7 X VDD_IO		VDD_IO + 0.3	V

Low-level input voltage	-0.3	0.3 X VDD_IO	V
Input low leakage current	-5.0	5.0	uA
High-level output voltage	0.9 X VDD_IO	VDD_IO	V
Low-level output voltage	0	0.1 X VDD_IO	V
High-level output current	3		mA
Low-level output current		-11	mA

5.3   RF Characteristic

5.3.1   WLAN RF Characteristics(Transmitter)

Table 21: WLAN Transmitter

Characteristics	Condition	EVM	Min	Type	Max	Unit
2.4GHz						
Output Power	11M CCK		13	15	18	dBm
	6M OFDM		14	14	17	dBm
	54M OFDM	-25	11	13	16	dBm
	6.5M,MCS0(HT20)		12	13	17	dBm
	65M,MCS7(HT20)	-27	10	11	15	dBm
	6.5M,MCS0(HT40)		11	12	16	dBm
	65M,MCS7(HT40)	-27	10	11	15	dBm
	180M,MCS9(VHT40)	-32	8	9	13	dBm
5GHz						
Output Power	54M OFDM	-25	10	12	16	dBm
	65M,MCS7(HT20)	-27	8	12	16	dBm
	65M,MCS7(HT20)	-27	8	12	16	dBm
	78M,MCS8(VHT20)	-30	8	12	16	dBm
	180M,MCS9(VHT40)	-32	8	12	16	dBm
	390M,MCS9(VHT80)	-32	6	9	12	dBm

5.3.2   WLAN RF Characteristics(Receive)

Table 22: WLAN Receive

Characteristics	Condition	Min	Type	Max	Unit
2.4GHz					
Sensitivity	11M CCK	-89	-86	-76	dBm
	54M OFDM	-76	-74	-65	dBm
	65M,MCS7(HT20)	-74	-72	-64	dBm
5GHz					
Sensitivity	54M OFDM	-78	-76	-65	dBm
	65M,MCS7(HT20)	-76	-74	-64	dBm

130M,MCS7(HT40)		-74	-72	-64	dBm
78M,MCS8(VHT20)		-70	-68	-59	dBm
180M,MCS9(VHT40)		-67	-65	-54	dBm
390M,MCS9(VHT80)		-65	-62	-51	dBm

5.3.3   Bluetooth RF Characteristics

Table 23: Bluetooth RF Characteristics

| Characteristics	Condition	Min	Type	Max	Unit
BT Transmitter, GFSK					
RF output power		9	11		dBm
Power control step		2	4	8	dB
BT Receiver Characteristics, Basic rate receiver					
Sensitivity	GFSK, BER = 0.1%			-88	dBm
	Pi/4-DQPSK, BER = 0.01%			-90	dBm
	8DPSK, BER = 0.01%			-82	
Max. useable input power	GFSK, BER = 0.1%	-5			dBm
	Pi/4-DQPSK, BER = 0.1%	-10			dBm
	8DPSK, BER = 0.1%	-10			dBm
BLE RF Characteristics					
BLE Transmitter output power				2	dBm
BT Receiver Characteristics, Low energy receiver	BER <= 0.1%			-92	dBm

5.4 System Power Sequence
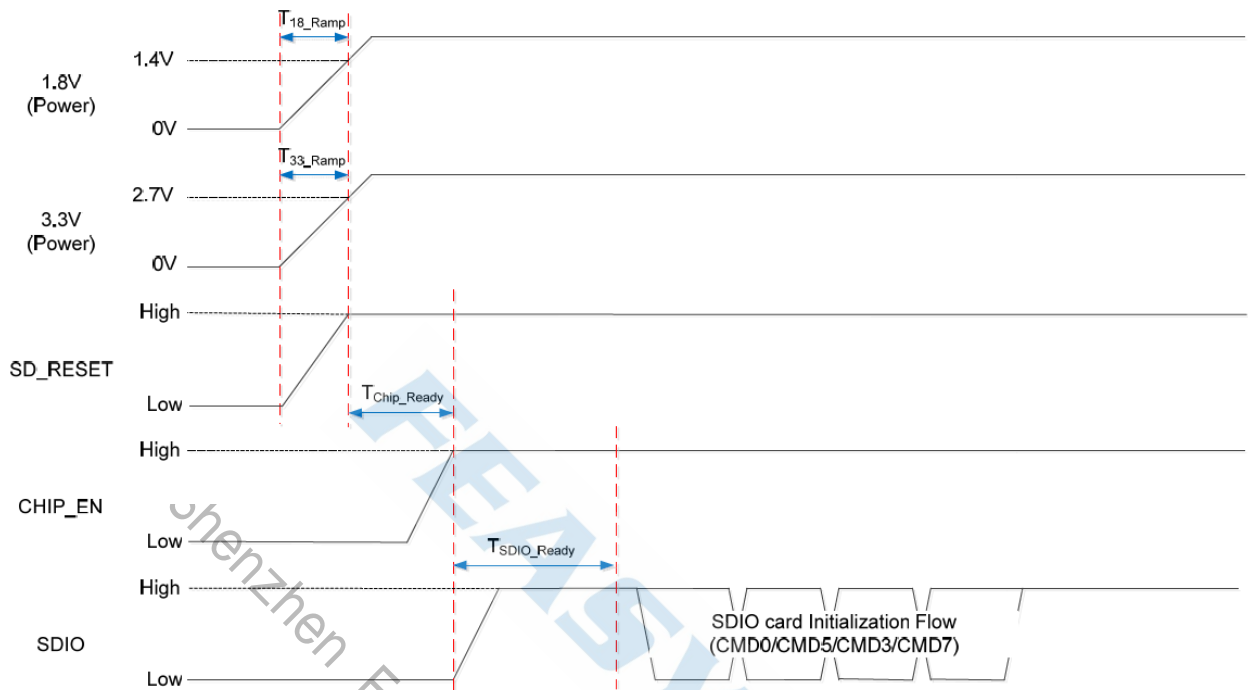
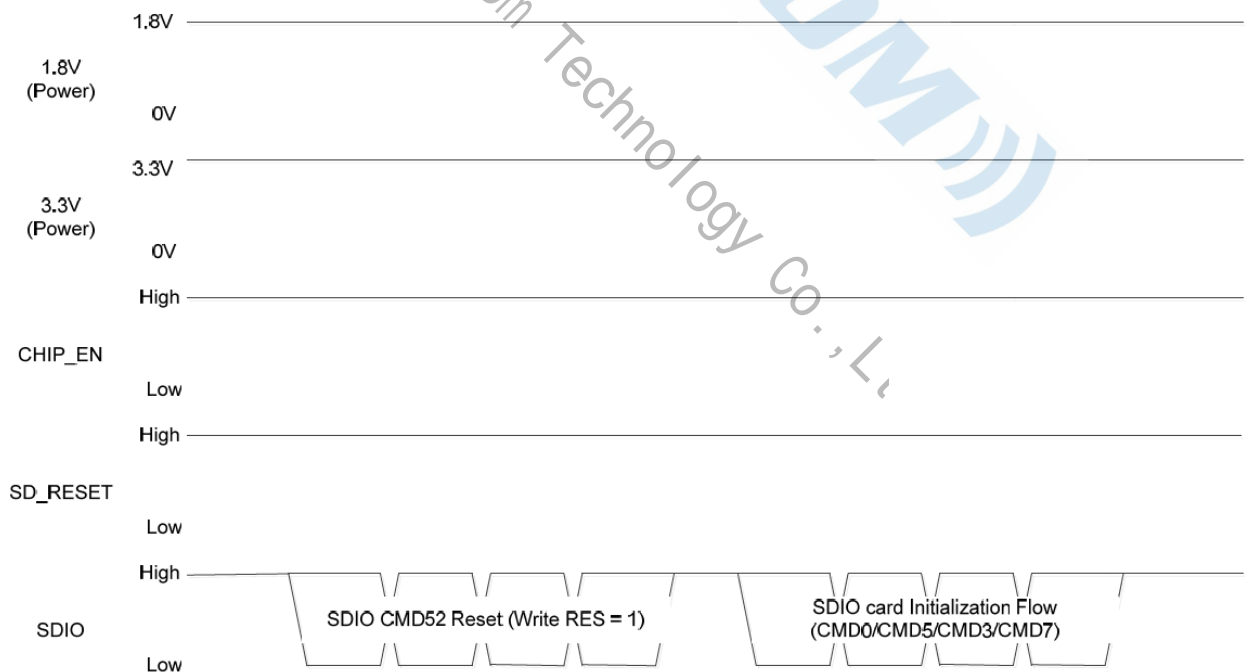**Figure 22:** System Power-On Sequence
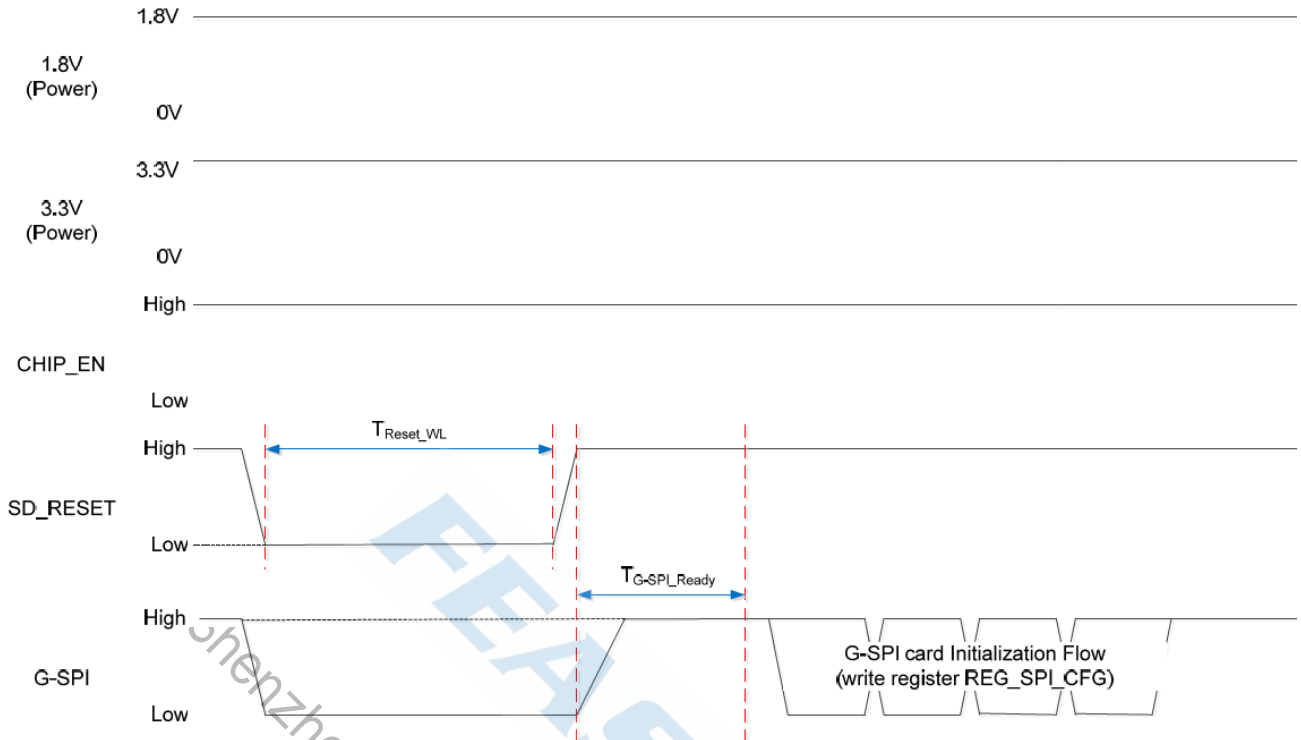

Figure 23: SDIO Reset Sequence
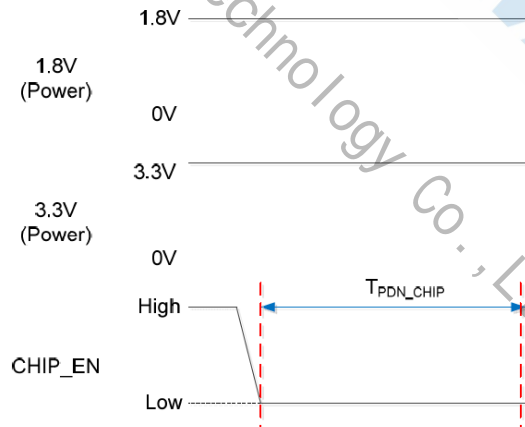
Figure 24: Wlan Reset Sequence

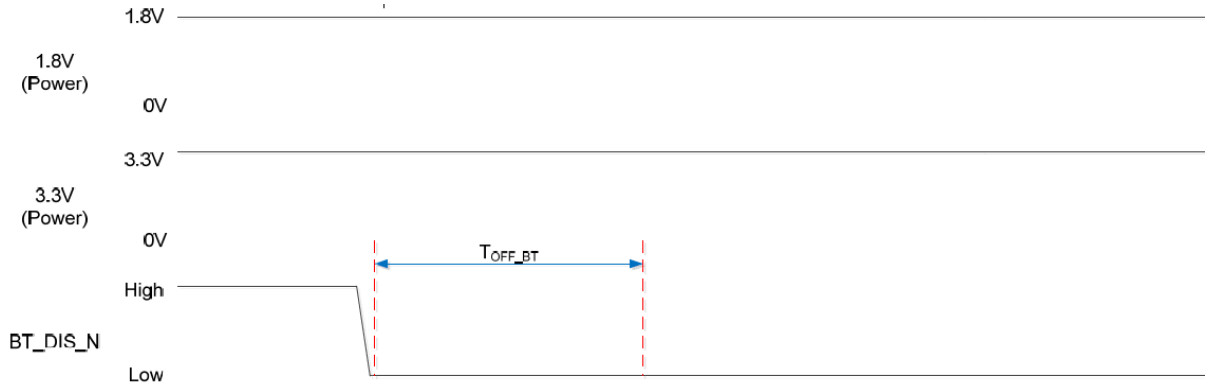**Figure 25:** Wlan Reset Sequence

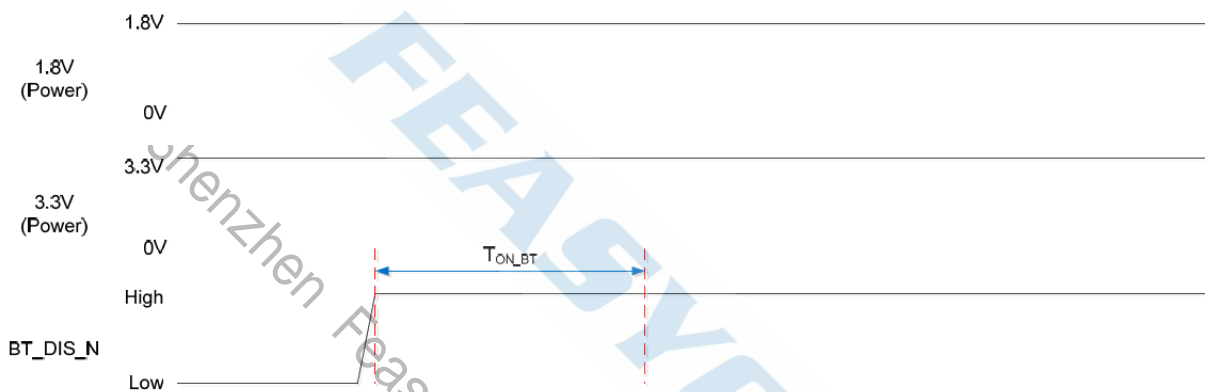**Figure 26:** BT Power On Sequence

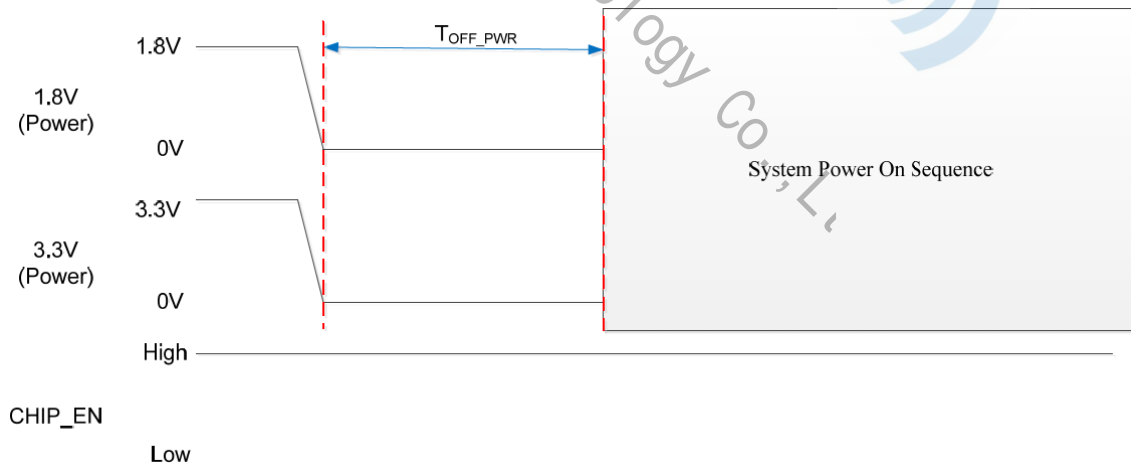**Figure 27:** BT Power Off Sequence

Figure 28: Power Reset Sequence

5.5   Power Consumption

Table 24: Power Consumption:

Internal Pull Resistor	Voltage	Power Consumption(mA)(Max)
VDD_3V3_WL	3.3V	500
VDD_IO	3.3V	300
Testing Condition:	2.4GHz Tx MCS0 6.5Mbps	

FSC-BW121 Module Power Consumption:

500mA @ VDD_3V3_WL(Maximum) and 300mA @ VDD_IO(Maximum)

Suggest customer design power capacity are 1000mA@VDD_3V3_WL and 500mA @ VDD_IO for FSC-BW121 Module.

6.   MSL & ESD

Table 25: MSL and ESD

Parameter	Value
MSL grade:	MSL 3
ESD grade	**Electrostatic discharge**
ESD – Human-body model (HBM) rating, JESD22-A114-F (Total samples from one wafer lot)	Pass ±2000 V, all pins
ESD – Charge-device model (CDM) rating, JESD22-C101-D (Total samples from one wafer lot)	Pass ±400 V, all pins

7.   RECOMMENDED TEMPERATURE REFLOW PROFILE

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to bake units on the card, please check the below and follow instructions specified by IPC/JEDEC J-STD-033.

Note: The shipping tray cannot be heated above 65°C. If baking is required at the higher temperatures displayed in the below , the modules must be removed from the shipping tray.

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 3 devices is 168 hours in ambient environment 30°C/60%RH.

Table 26: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

Feasycom surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Feasycom surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

The soldering profile depends on various parameters necessitating a set up for each application.   The data here is given only for guidance on solder reflow.
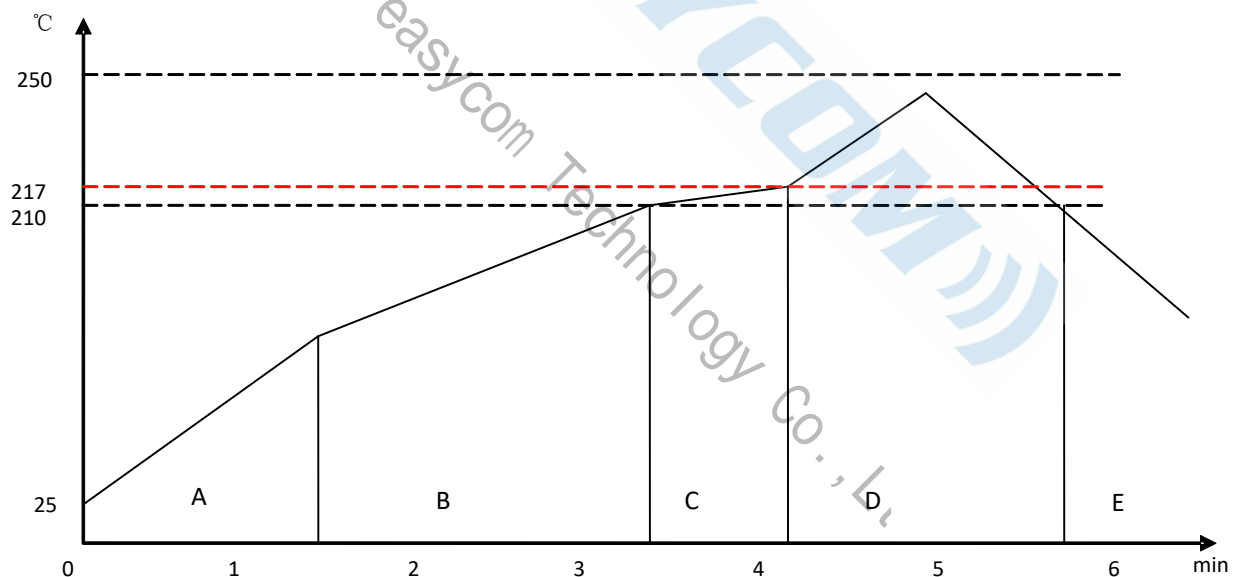
Figure 29: Typical Lead-free Re-flow

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**.   The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C.   This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized.   Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (C) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5.   It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C.   The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longer-lasting joint. **Typical cooling rate should be 4 °C.**

8. MECHANICAL DETAILS

8.1 Mechanical Details

- Dimension: 17mm(W) x 17mm(L) x 2.4mm(H)   Tolerance: ±0.1mm
- Module size: 17mm X 17mm   Tolerance: ±0.2mm
- Pad size: 1.5mmX0.75mm   Tolerance: ±0.1mm
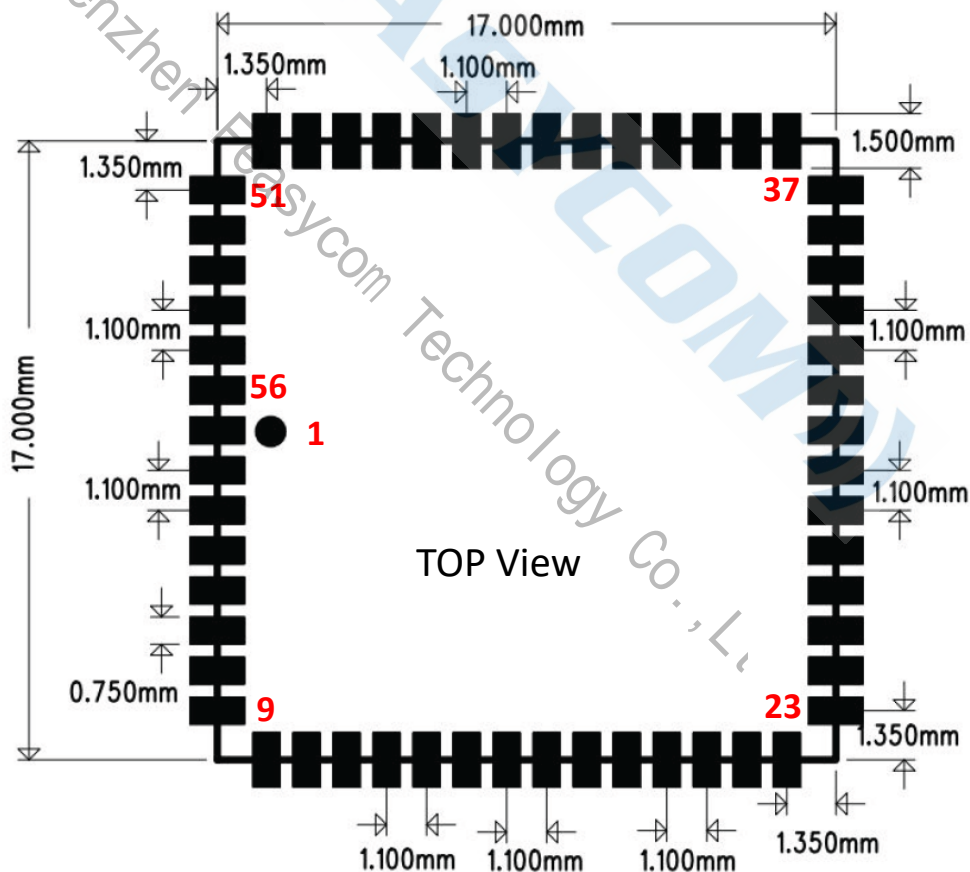- Pad pitch: 1.1mm   Tolerance: ±0.1mm

Figure 30: FSC-BW121 footprint Layout Guide (Top View)

9. HARDWARE INTEGRATION SUGGESTIONS

9.1 Soldering Recommendations

FSC-BW121 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

9.2 Layout Guidelines(Internal Antenna)

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.
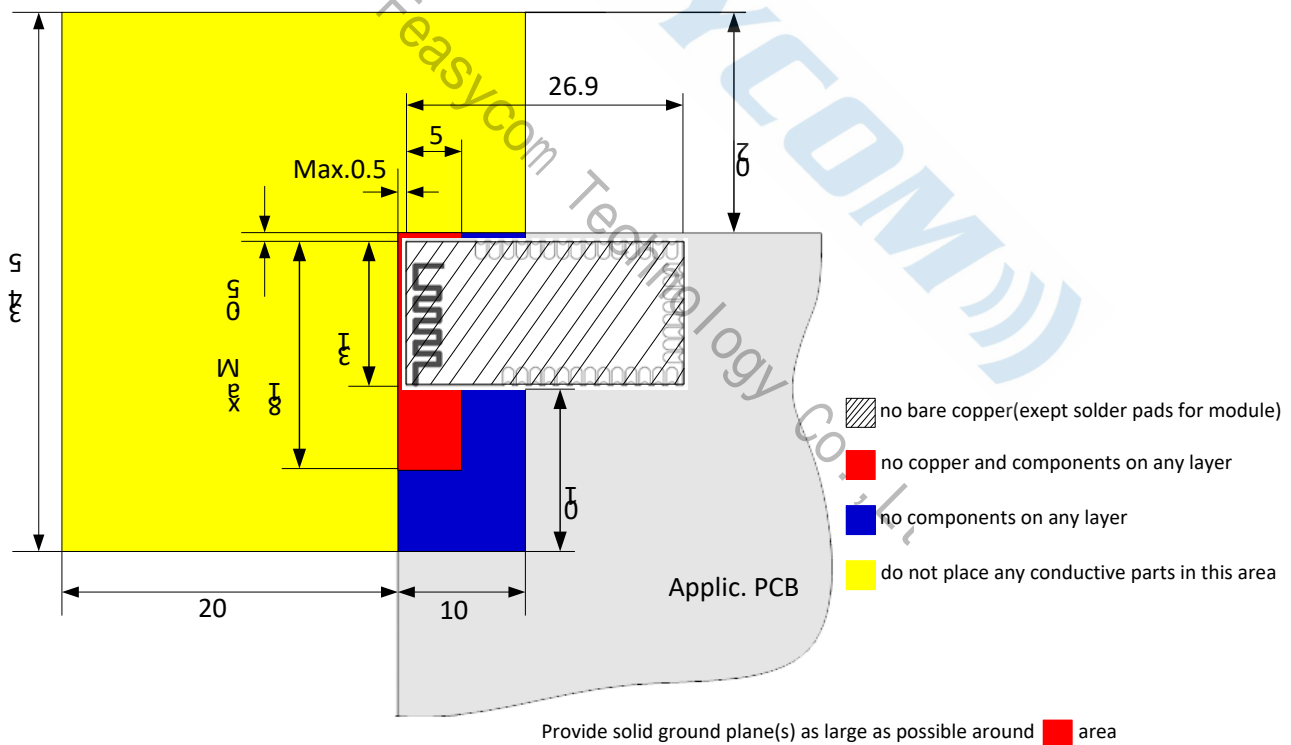

Figure 31: Restricted Area (Design schematic, for reference only.   Unit: mm)

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any

sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9.3   Layout Guidelines(External Antenna)

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module.   The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board.   All RF circuits in the module are close to the antenna port.   The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.
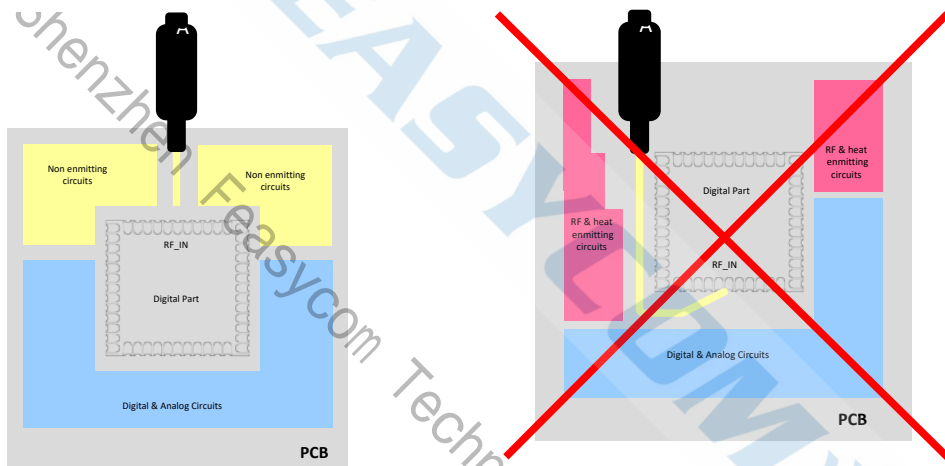

Figure 32: Placement the Module on a System Board

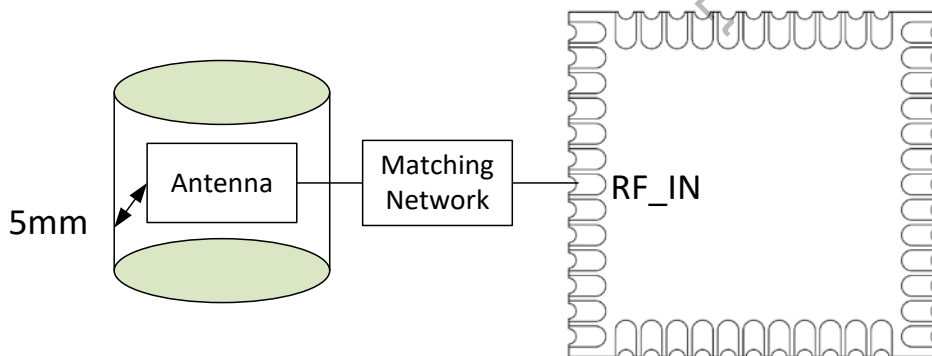### 9.3.1   Antenna Connection and Grounding Plane Design

Figure 33: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.

- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.

- Routing the RF close to digital sections of the system board should be avoided.

- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.
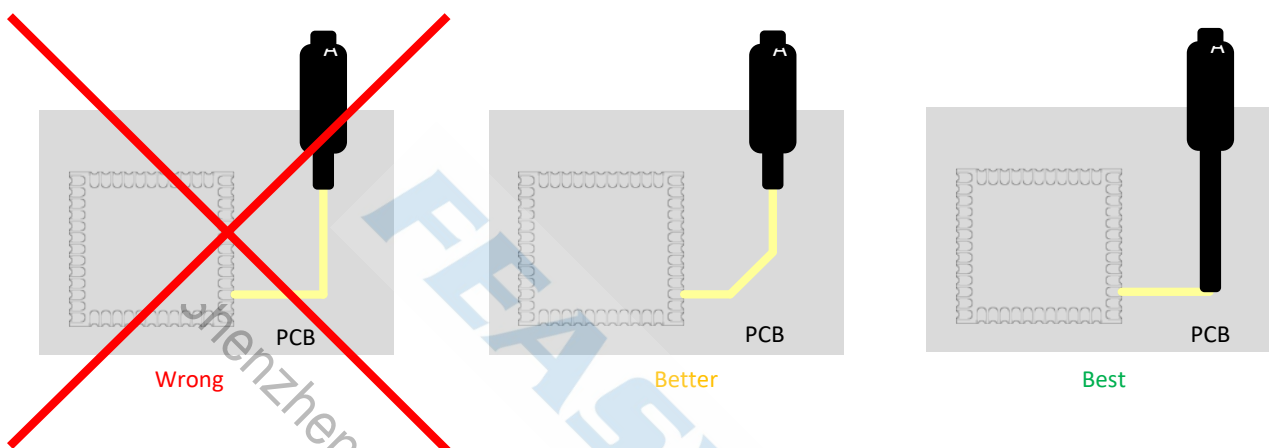

Figure 34: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.

- Use as many vias as possible to connect the ground planes.

9.4 SDIO Lines Layout Guideline

The following SDIO line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 8mA.

SDIO_CMD_WL

SDIO_CLK_WL

SDIO_D0_WL ~ SDIO_D3_WL

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.5 HCI Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

HCI_RX_BT

HCI_TX_BT

HCI_CTS_BT

HCI_RTS_BT

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.6   PCM Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 mA

AUD_FSYNC_BT(PCM_SYNC)

AUD_CLK_BT(PCM_CLK)

AUD_OUT_BT(PCM_OUT)

AUD _IN_BT(PCM_IN)

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω

9.7   RTC Clock(32.768kHz) Lines Layout Guideline

Follow the same guidelines recommended for the fast clock, It is extremely important that the RTC_CLK trace not be routed next to any digital signals and near the analog audio signals. Furthermore, no digital signals should be routed above or below the RTC_CLK trace to avoid coupling.

9.8   Power Trace Lines Layout Guideline

VDD_3V3_WL Trace Width: 40mil

VDD_IO Trace Width: 20mil

9.9   Ground Lines Layout Guideline

A Complete Ground in Ground Layer.

Add Ground Through Holes to FSC-BW121 Module Ground Pads

Decoupling Capacitors close to FSC-BW121 Module Power and Ground Pads

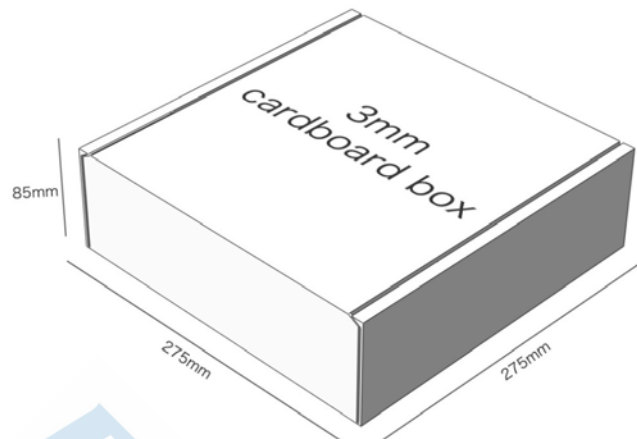# 10.   PRODUCT PACKAGING INFORMATION

10.1   Default Packing

a, Tray vacuum

b, Tray Dimension: 140mm * 265mm

Figure 35: Tray vacuum

10.2   Packing box(Optional)

* If require any other packing, must be confirmed with customer

* Package: 1000PCS Per Carton (Min Carton Package)

Figure 36: Packing Box

11. APPLICATION SCHEMATIC