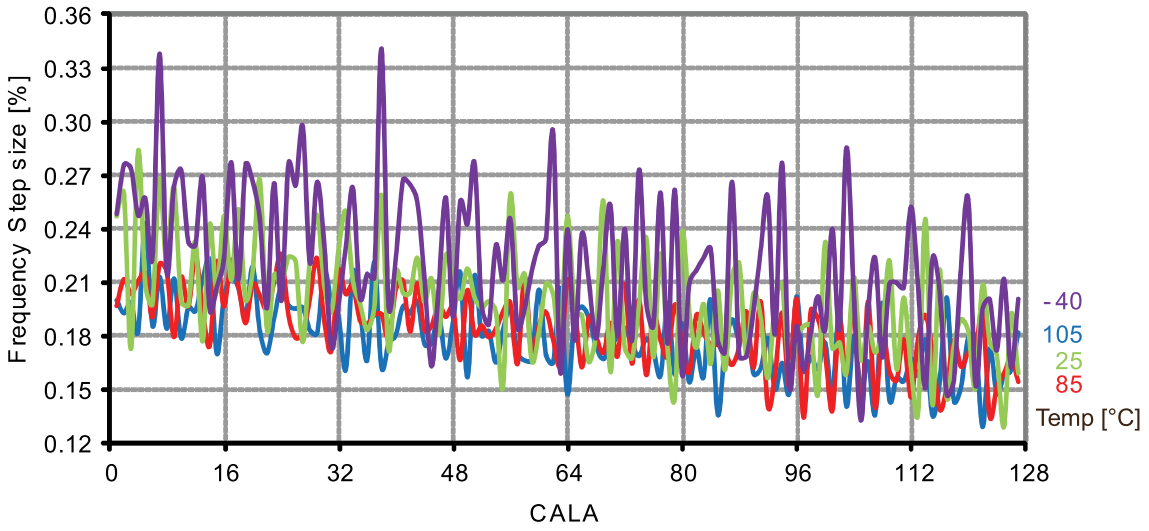
Figure 37-80. 48MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.



37.1.11 Two-Wire Interface characteristics

Figure 37-81. SDA hold time vs. Vcc.

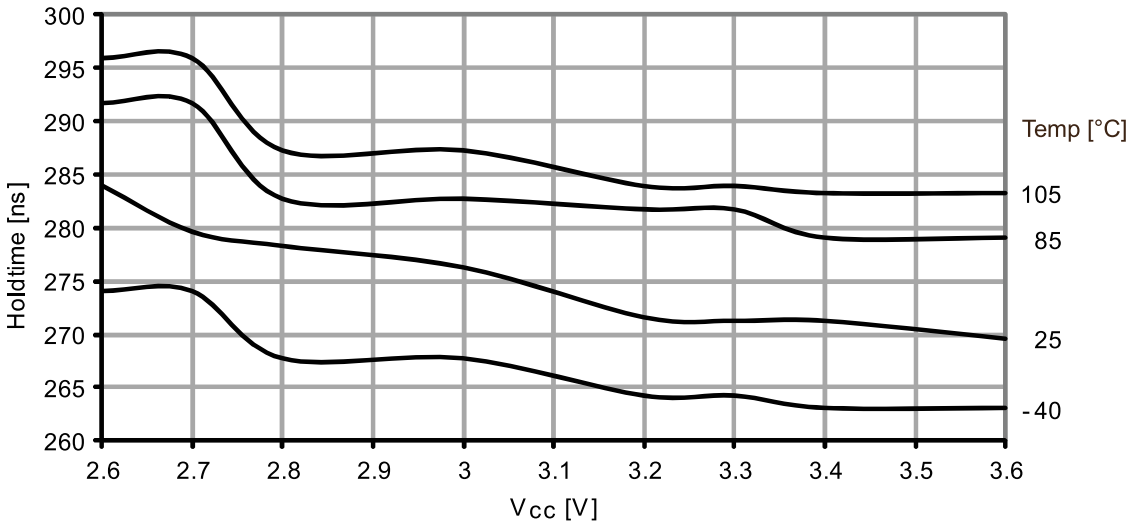
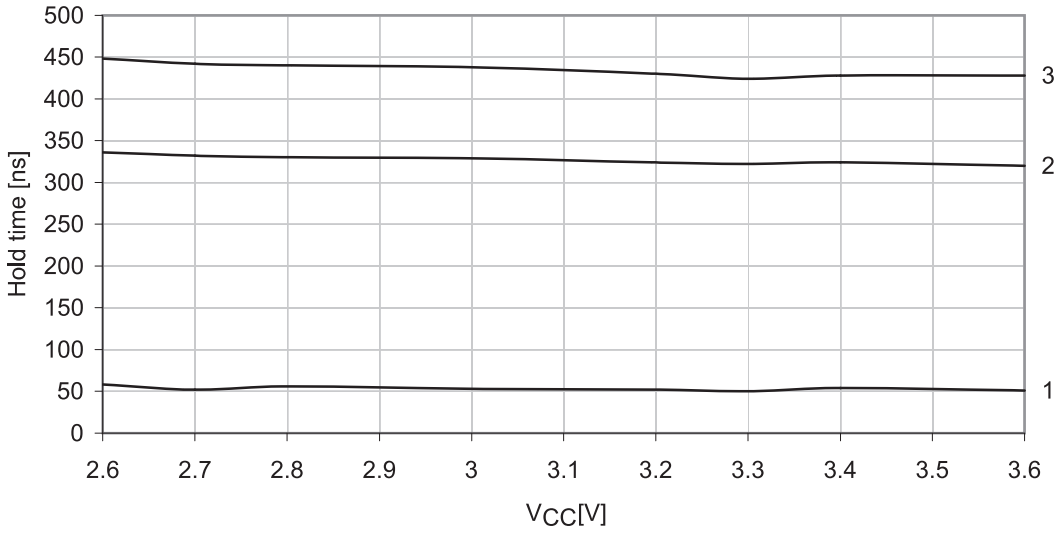
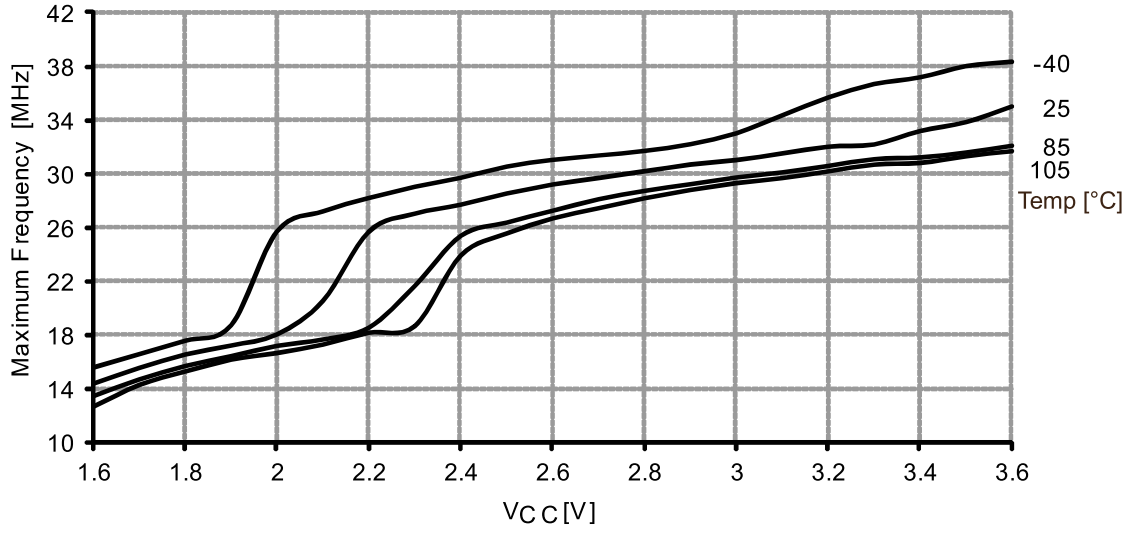


Figure 37-82. SDA hold time vs. supply voltage.



37.1.12 PDI characteristics

Figure 37-83. Maximum PDI frequency vs. V_{CC}.



37.2 ATxmega128A3U

37.2.1 Current consumption

37.2.1.1 Active mode supply current

Figure 37-84. Active supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

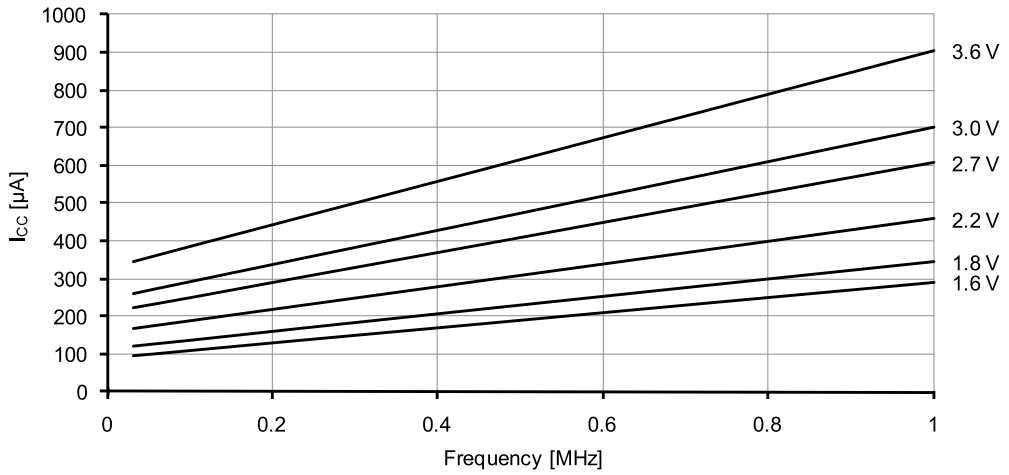


Figure 37-85. Active supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

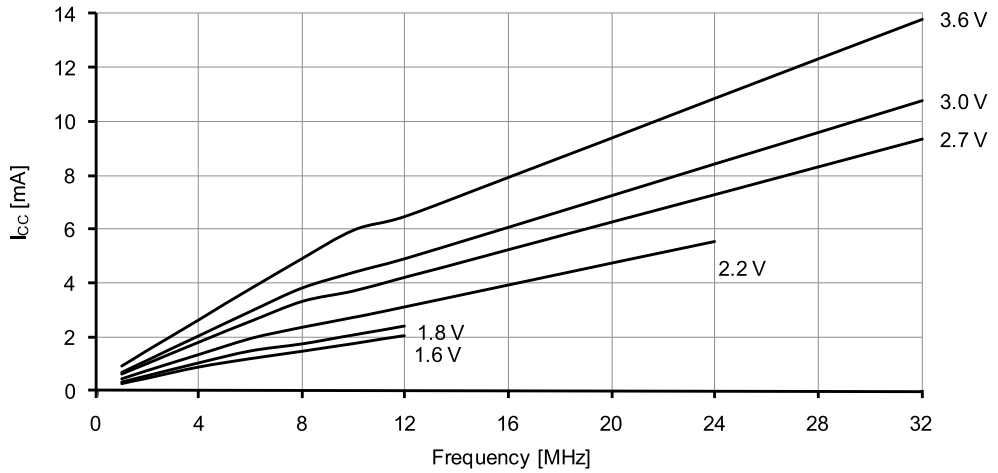


Figure 37-86. Active mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

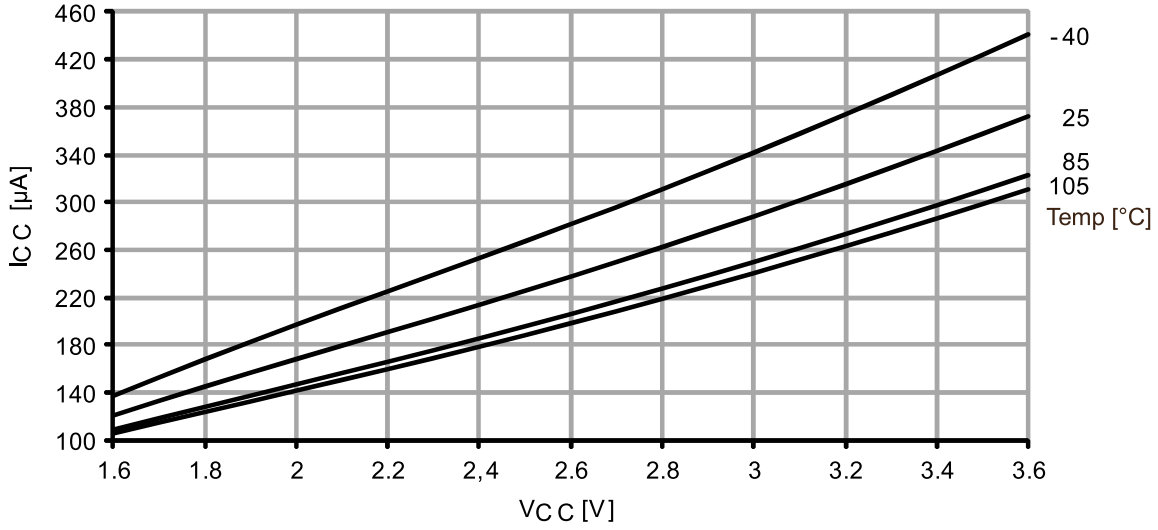


Figure 37-87. Active mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

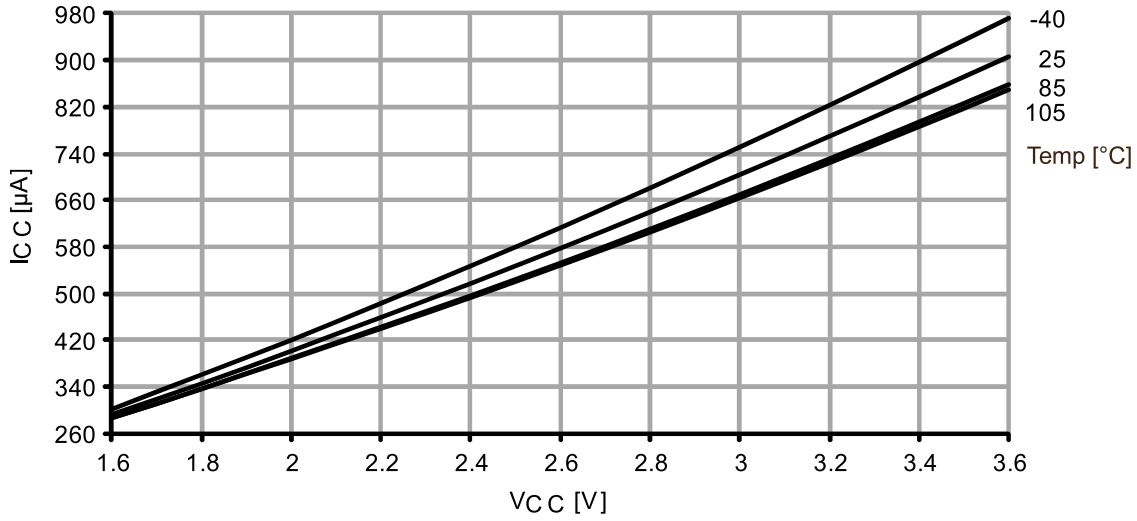


Figure 37-88. Active mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

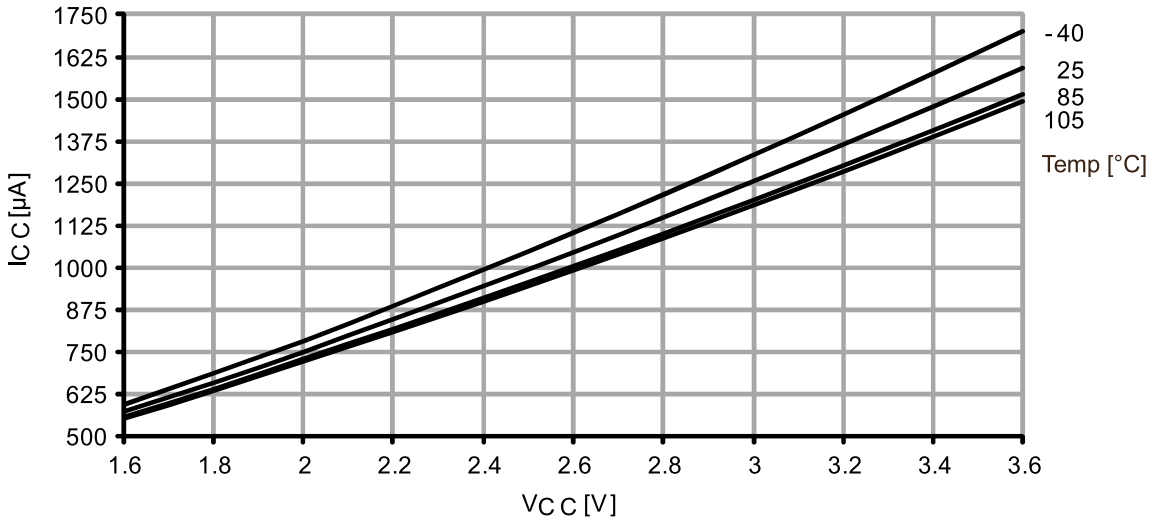


Figure 37-89. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

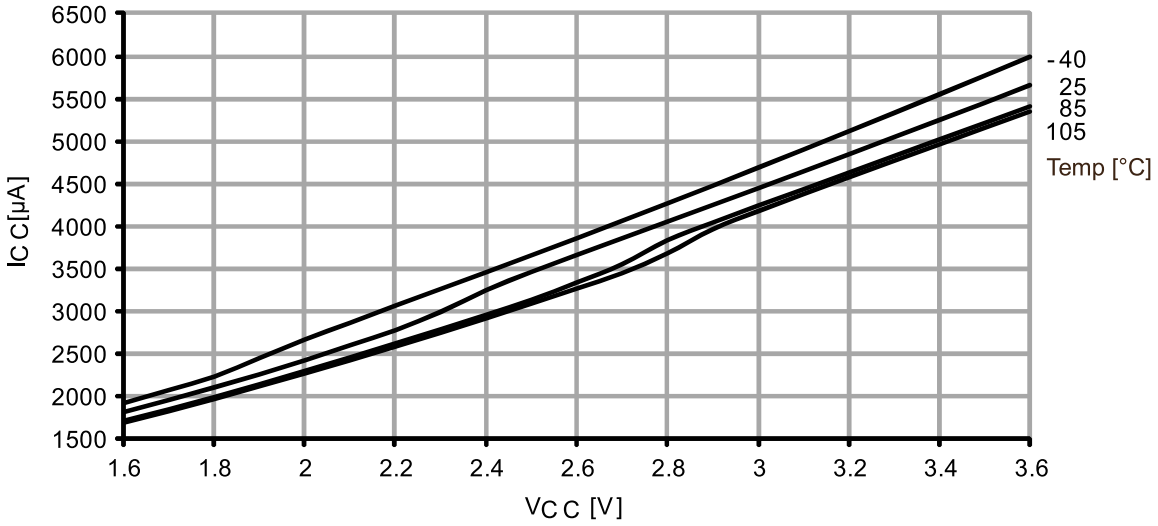
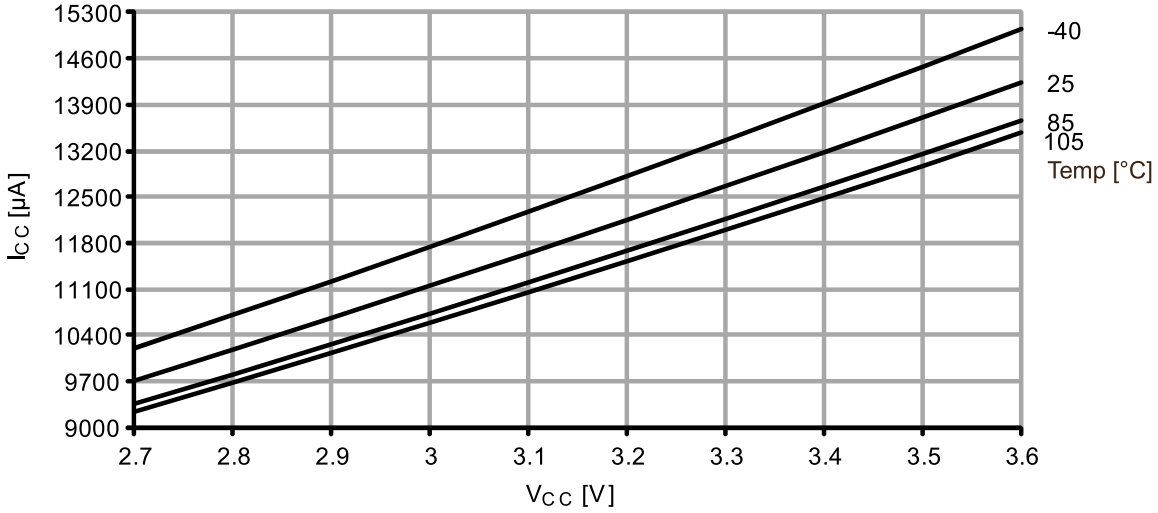


Figure 37-90. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



37.2.1.2 Idle mode supply current

Figure 37-91. Idle mode supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C.

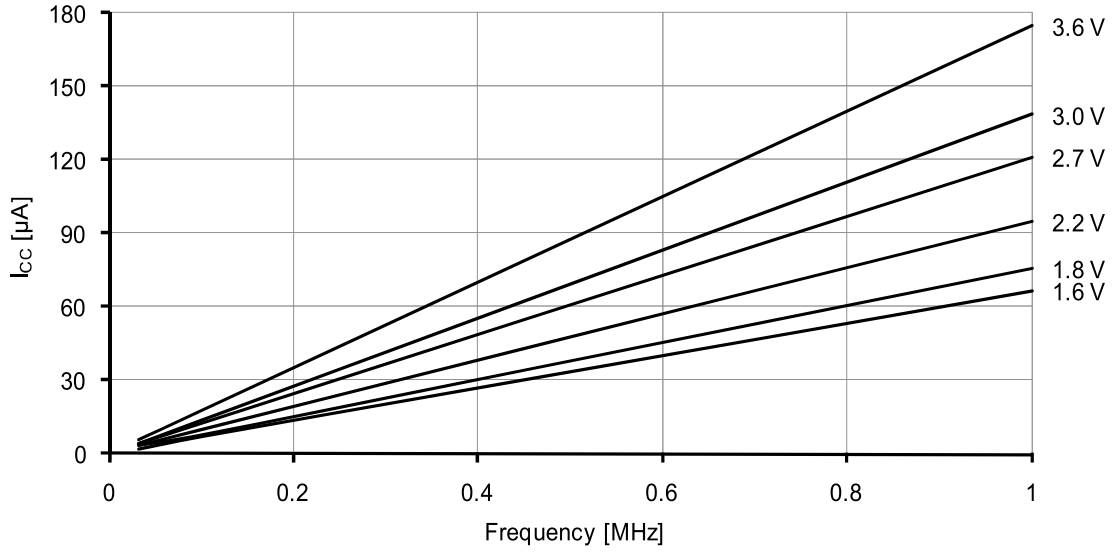


Figure 37-92. Idle mode supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

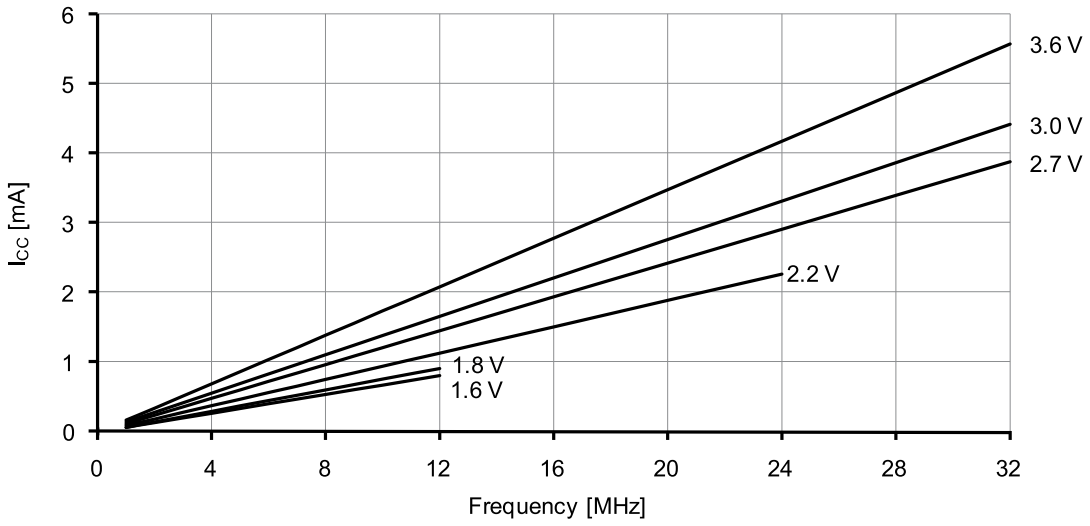


Figure 37-93. Idle mode supply current vs. V_{CC}.
f_{SYS} = 32.768kHz internal oscillator.

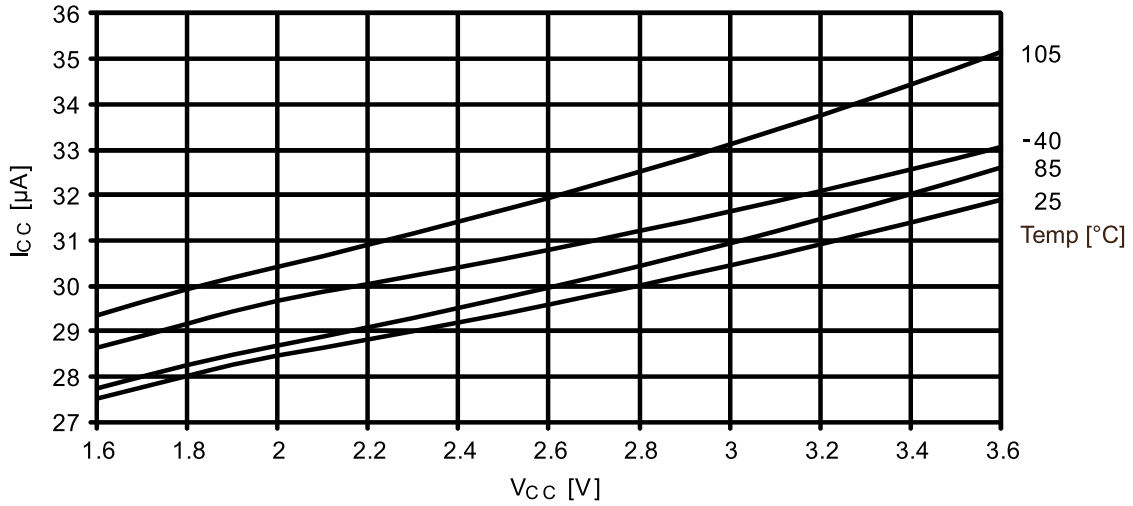


Figure 37-94. Idle mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

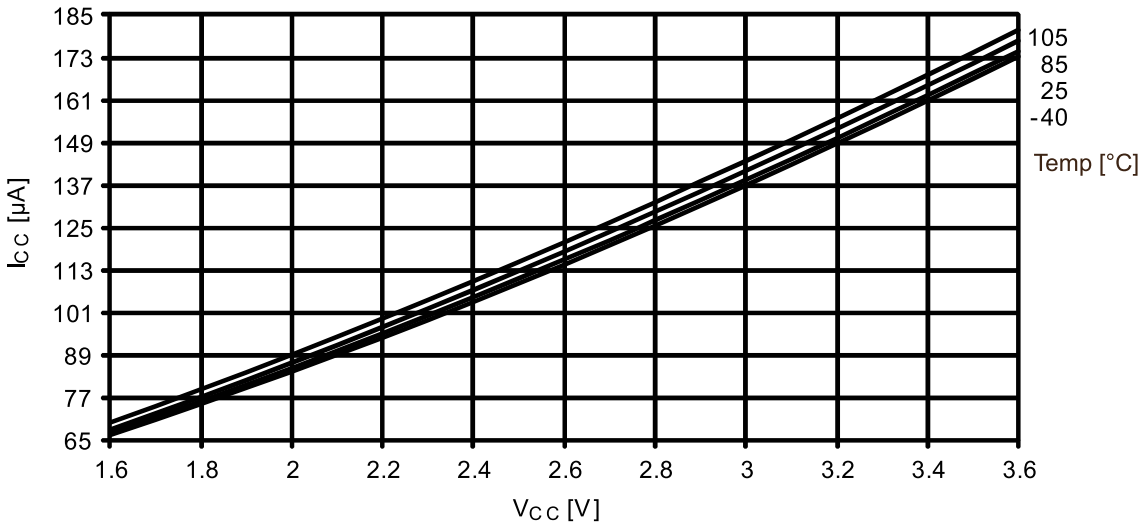


Figure 37-95. Idle mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

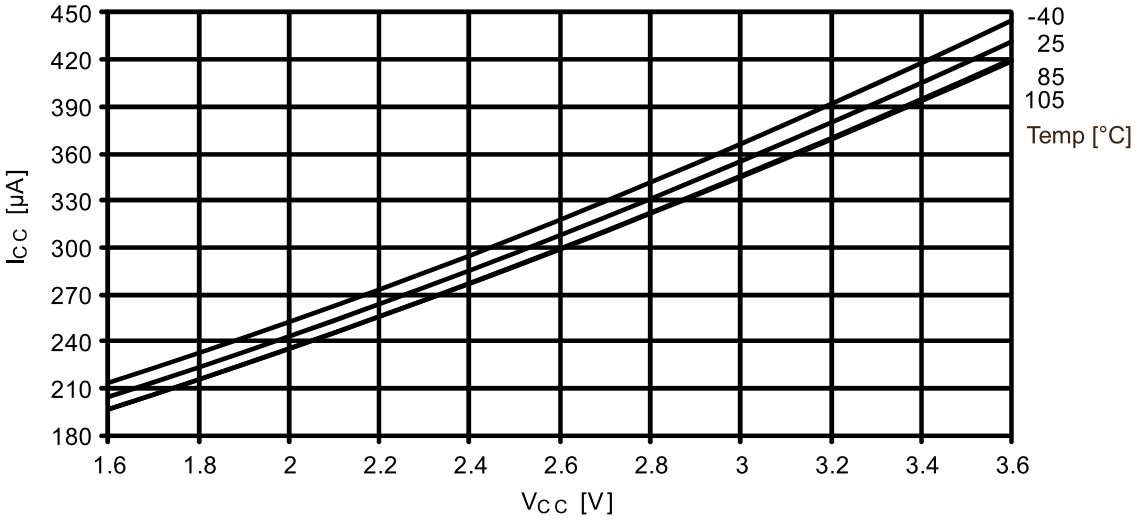


Figure 37-96. Idle mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

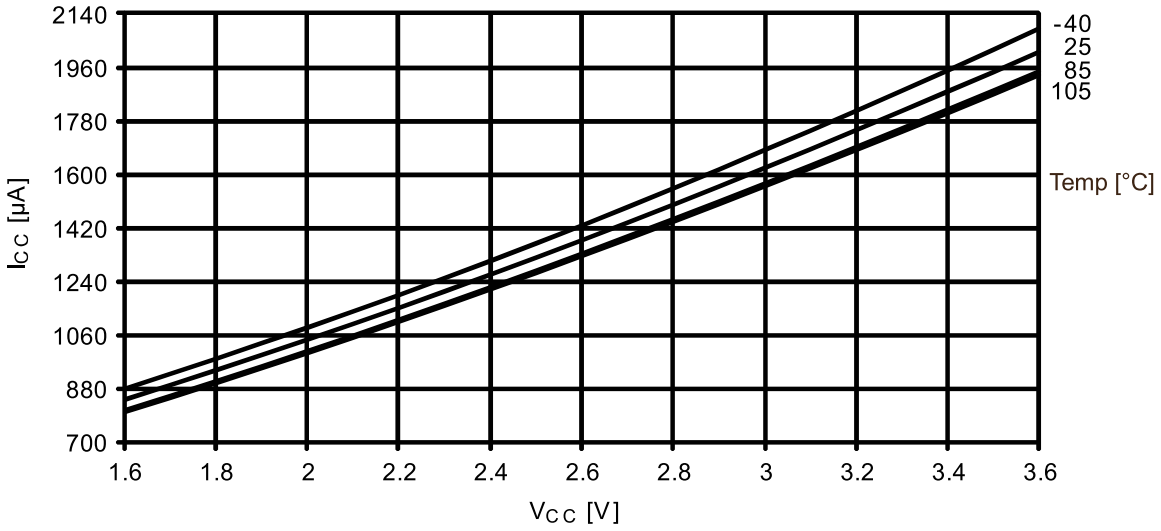
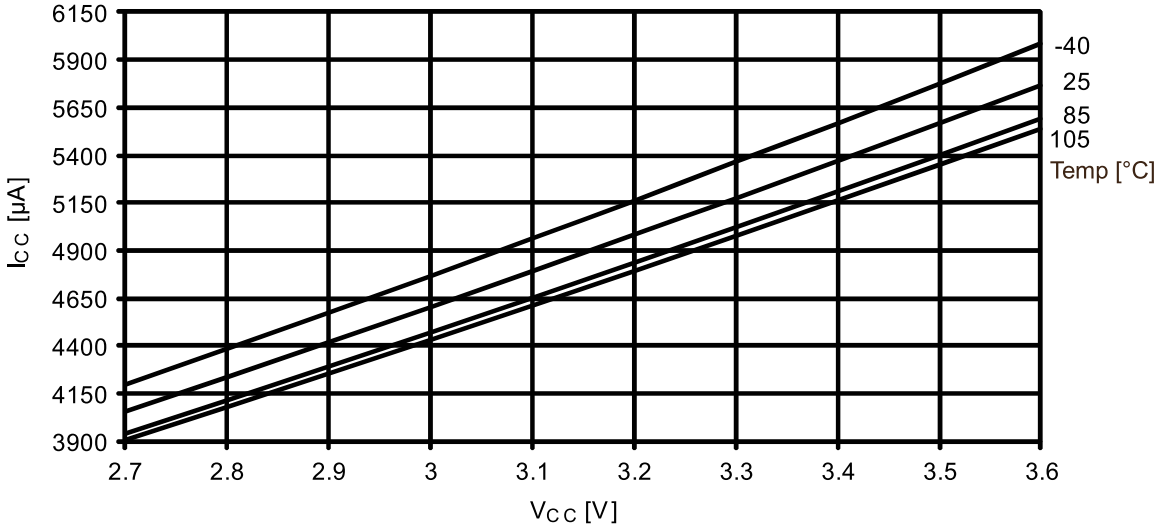


Figure 37-97. Idle mode current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



37.2.1.3 Power-down mode supply current

Figure 37-98. Power-down mode supply current vs. V_{CC}.
All functions disabled.

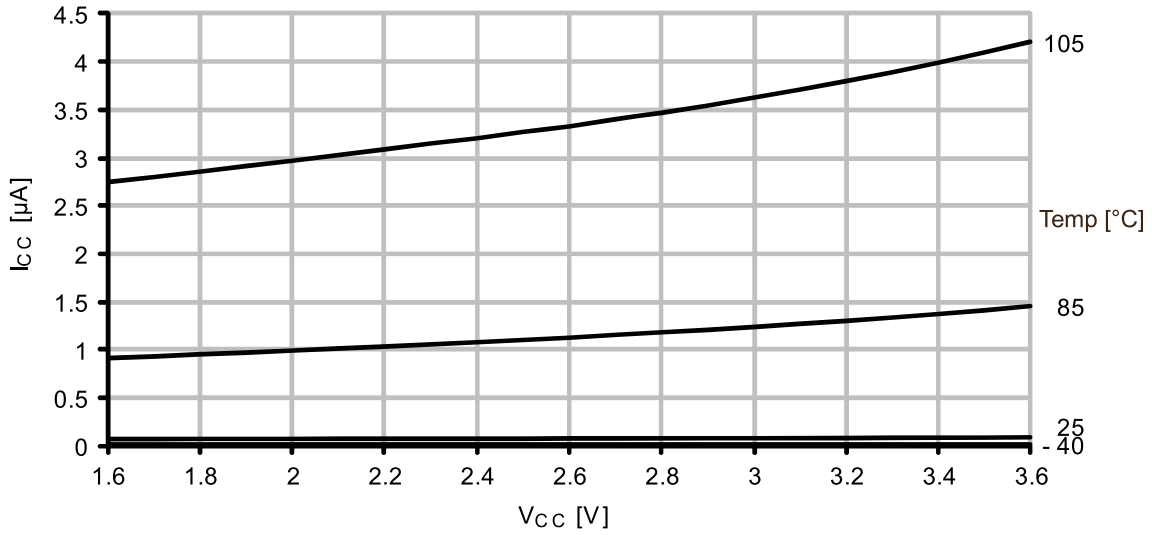
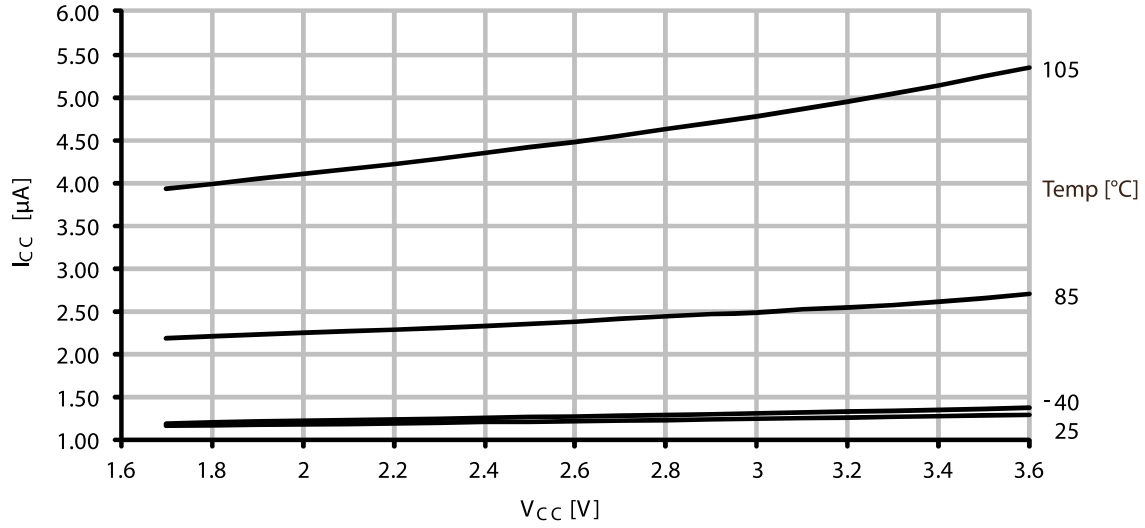


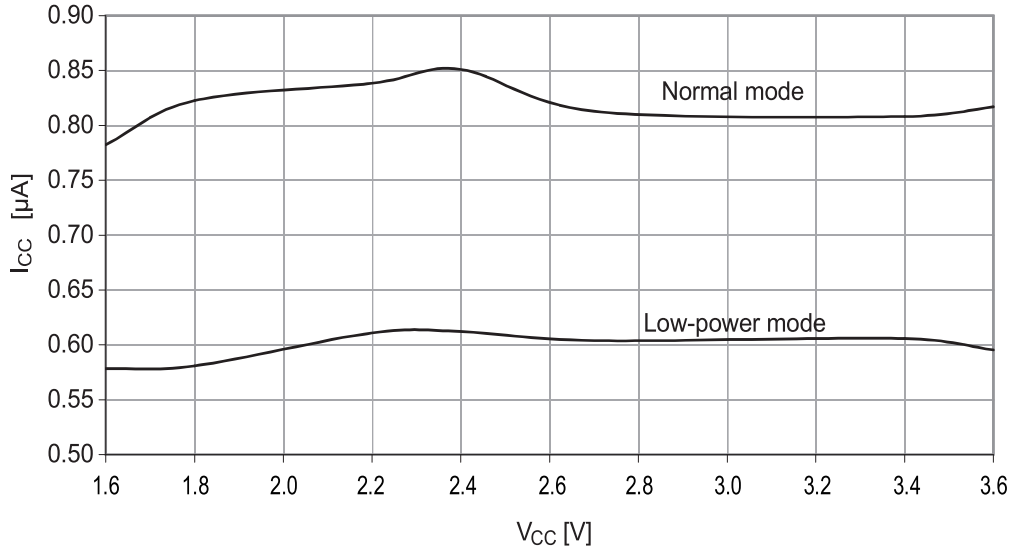
Figure 37-99. Power-down mode supply current vs. V_{CC}.
Watchdog and sampled BOD enabled.



37.2.1.4 Power-save mode supply current

Figure 37-100. Power-save mode supply current vs. V_{CC}.

Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC.



37.2.1.5 Standby mode supply current

Figure 37-101. Standby supply current vs. V_{CC}.

Standby, f_{SYS} = 1MHz.

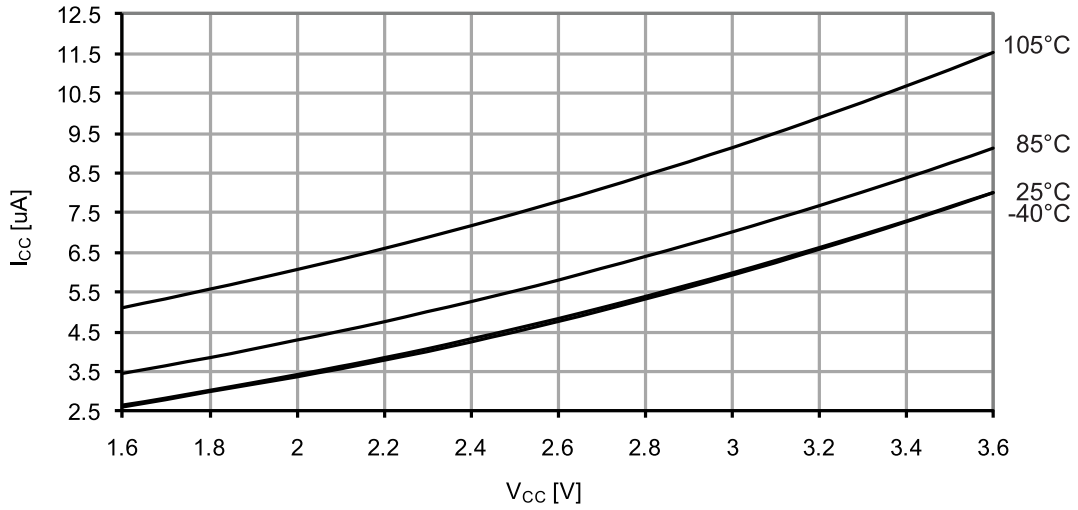
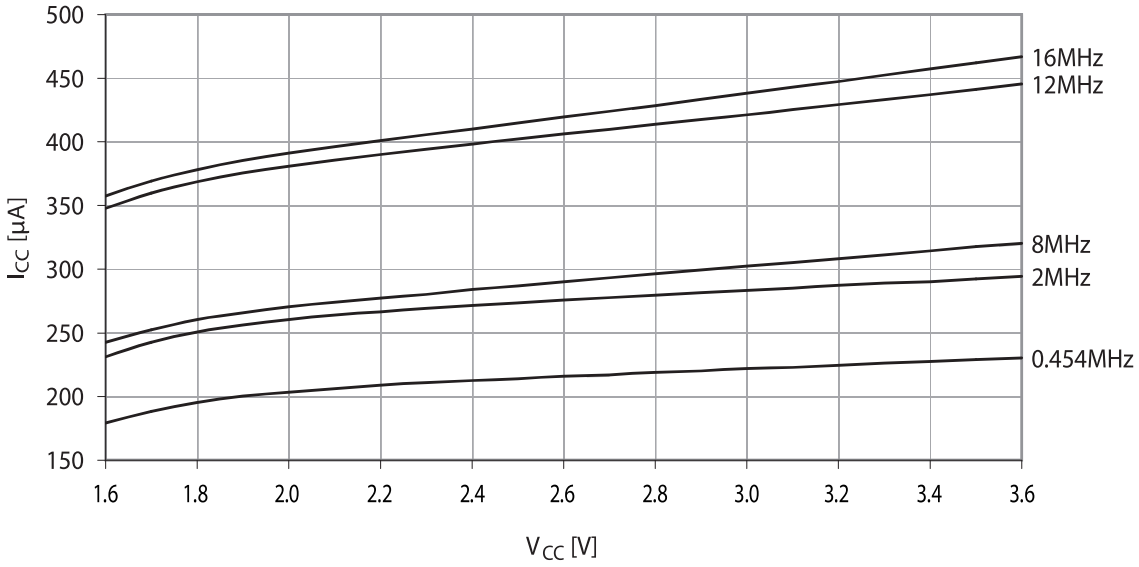


Figure 37-102. Standby supply current vs. V_{CC}.

25°C, running from different crystal oscillators.



37.2.2 I/O Pin Characteristics

37.2.2.1 Pull-up

Figure 37-103. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 1.8V.

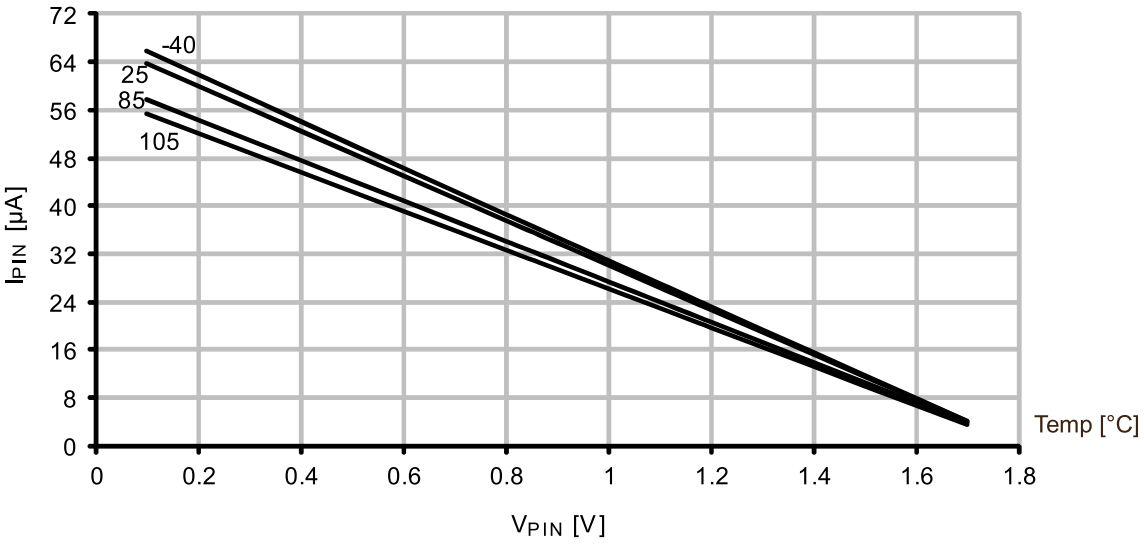


Figure 37-104. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.0V.

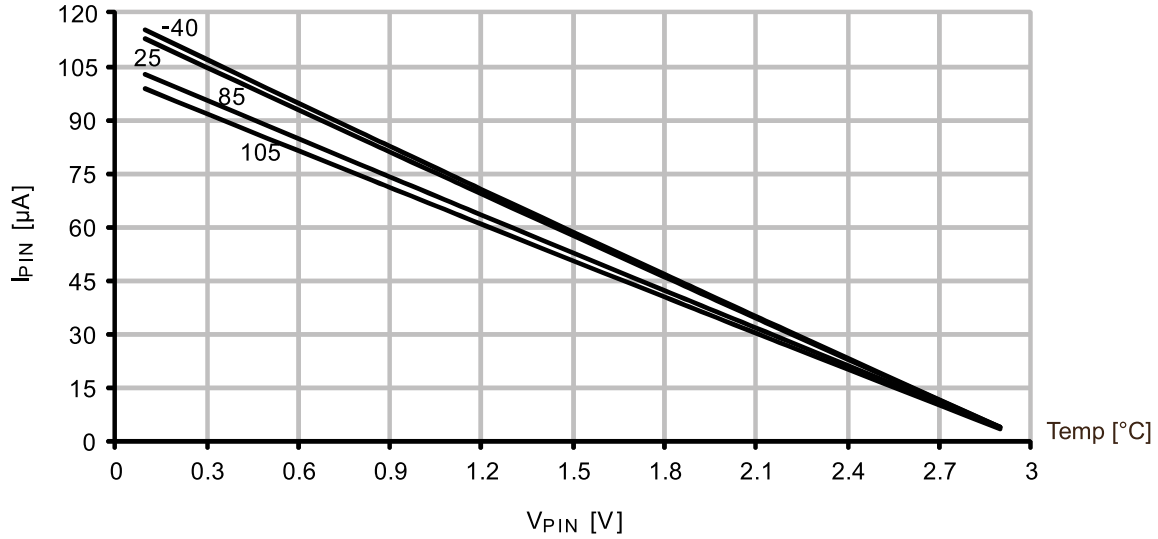
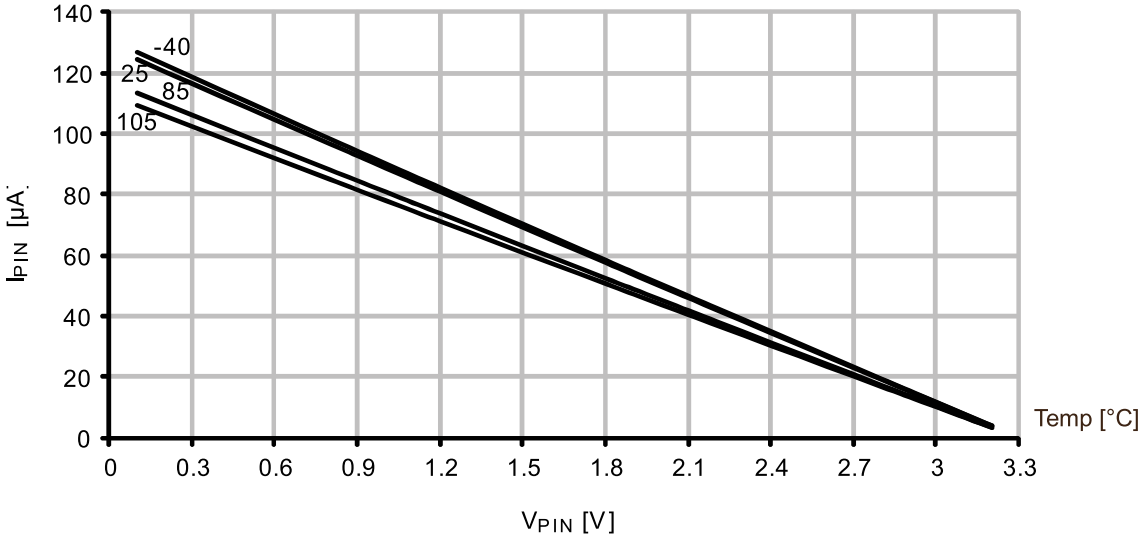


Figure 37-105. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.3V.



37.2.2.2 Output Voltage vs. Sink/Source Current

Figure 37-106. I/O pin output voltage vs. source current.

V_{CC} = 1.8V.

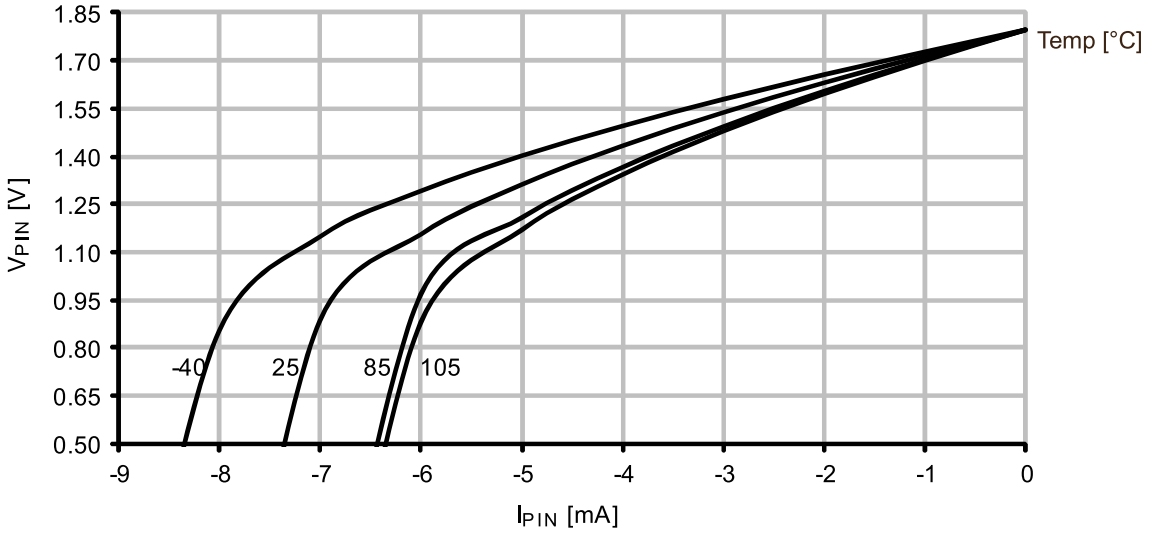


Figure 37-107. I/O pin output voltage vs. source current.

V_{CC} = 3.0V.

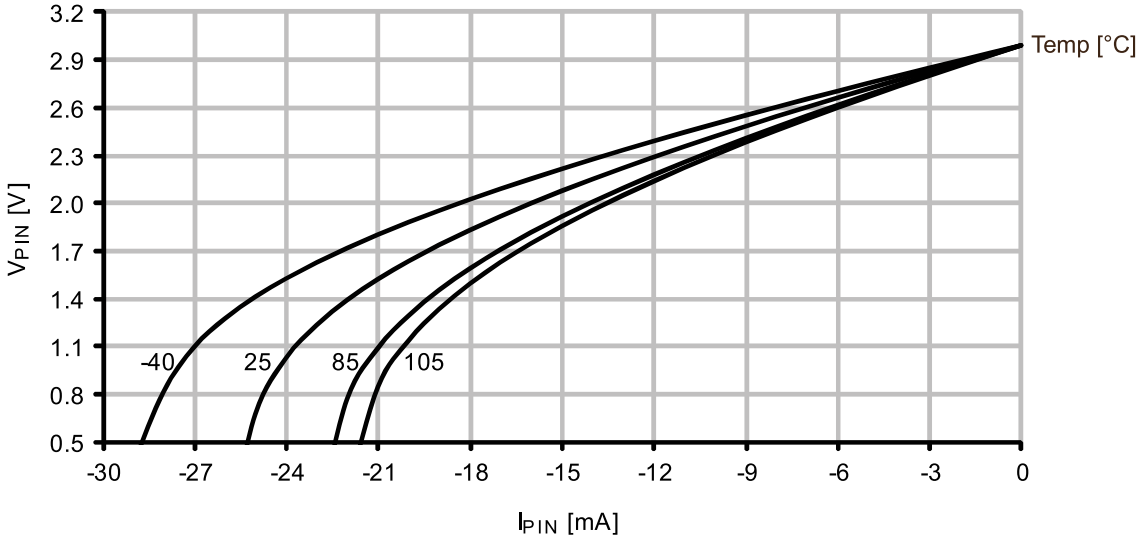


Figure 37-108. I/O pin output voltage vs. source current.

V_{CC} = 3.3V.

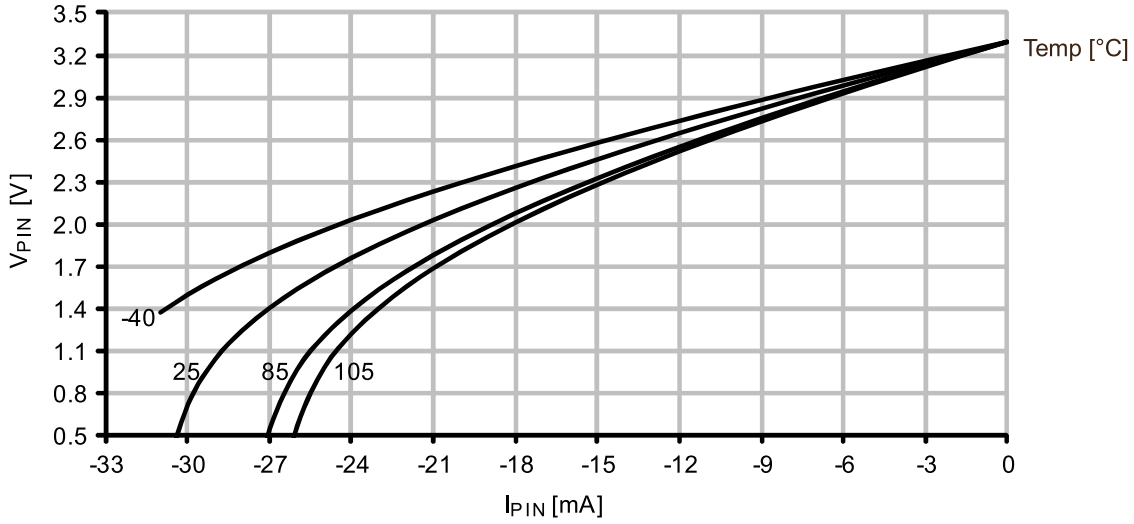


Figure 37-109. I/O pin output voltage vs. source current.

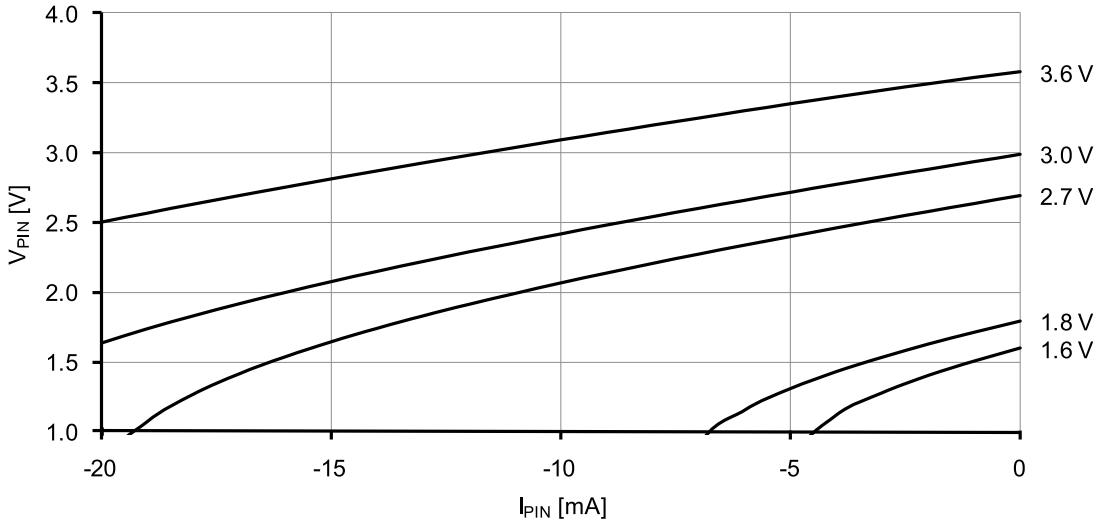


Figure 37-110. I/O pin output voltage vs. sink current.

V_{CC} = 1.8V.

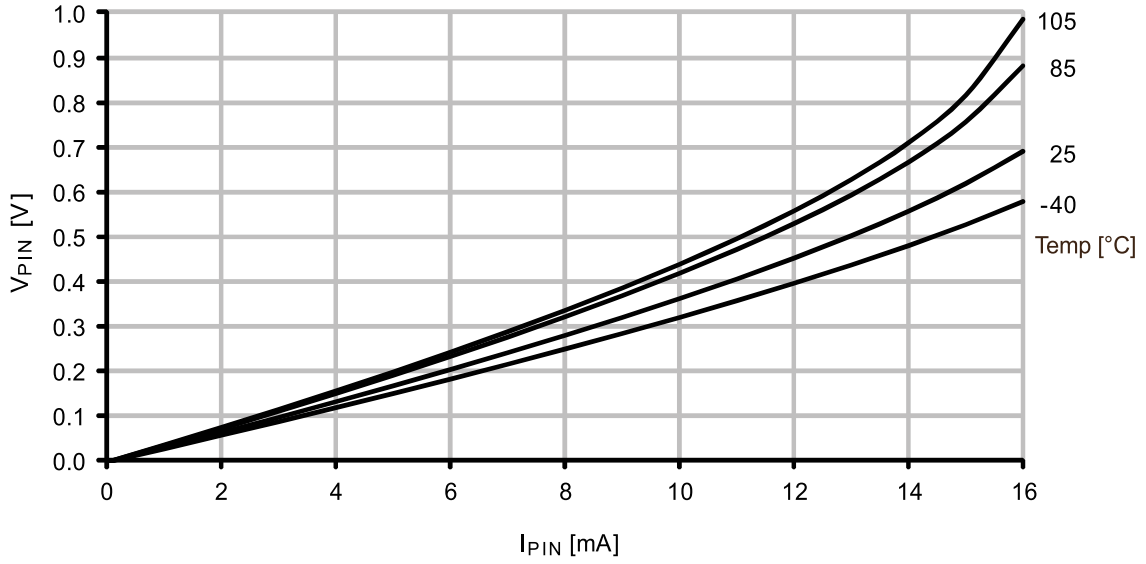


Figure 37-111. I/O pin output voltage vs. sink current.

V_{CC} = 3.0V.

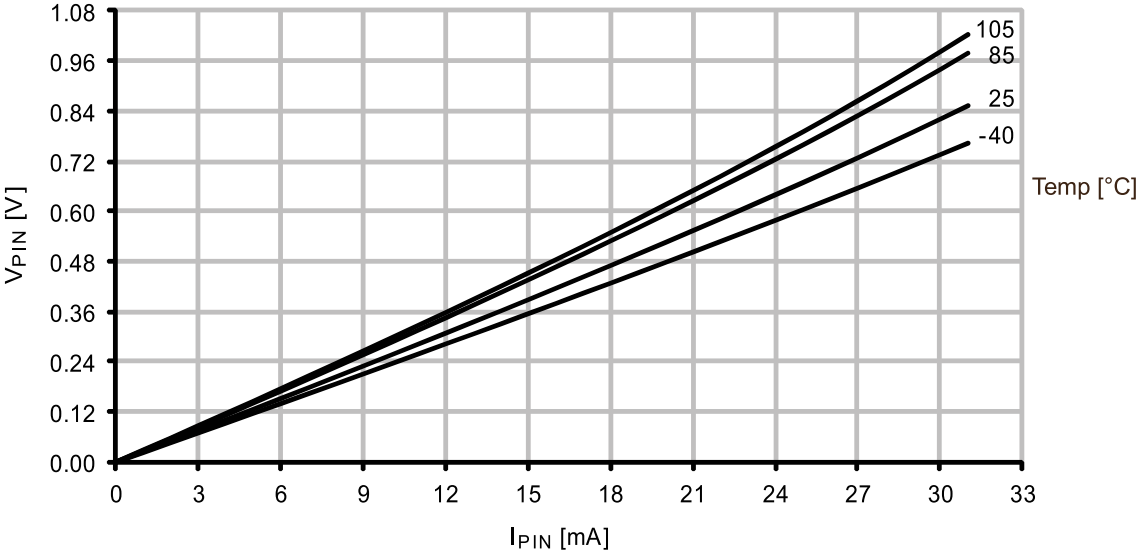


Figure 37-112. I/O pin output voltage vs. sink current.

V_{CC} = 3.3V.

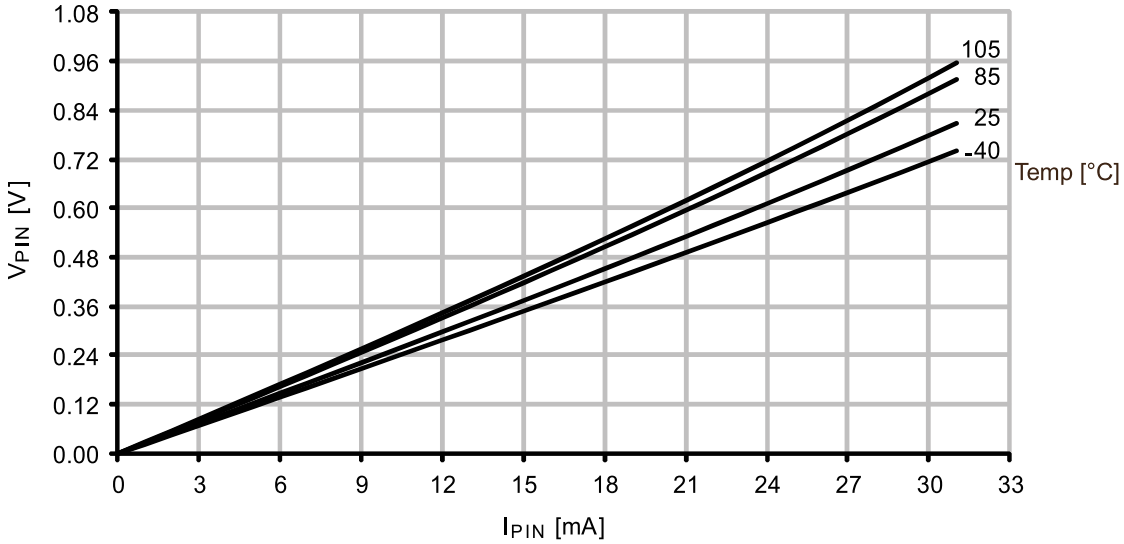
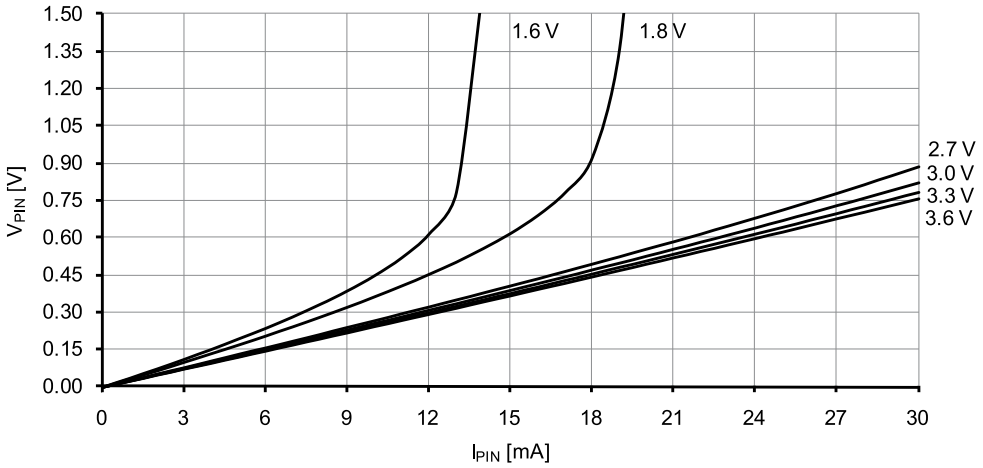


Figure 37-113. I/O pin output voltage vs. sink current.



37.2.2.3 Thresholds and Hysteresis

Figure 37-114. I/O pin input threshold voltage vs. V_{CC}.
T = 25°C.

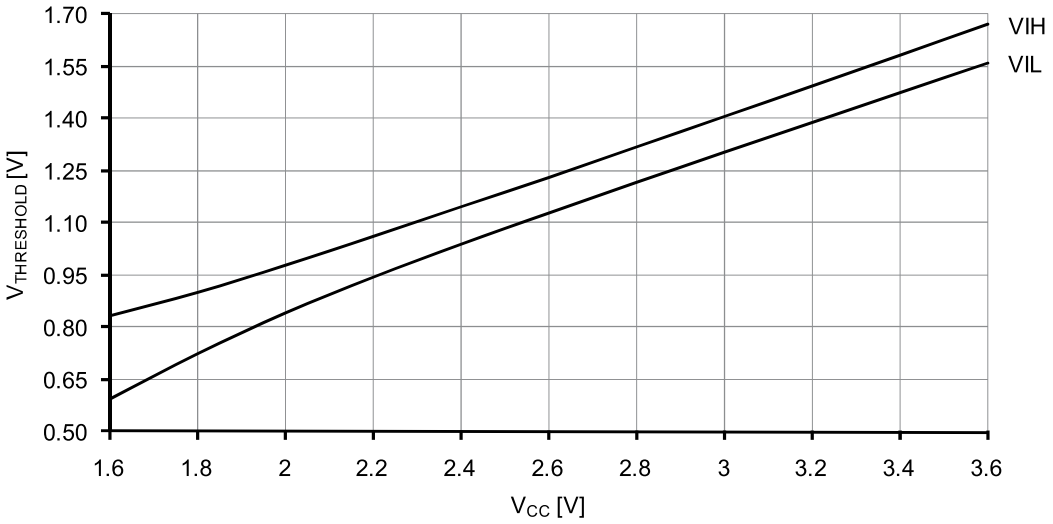


Figure 37-115. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} I/O pin read as "1".

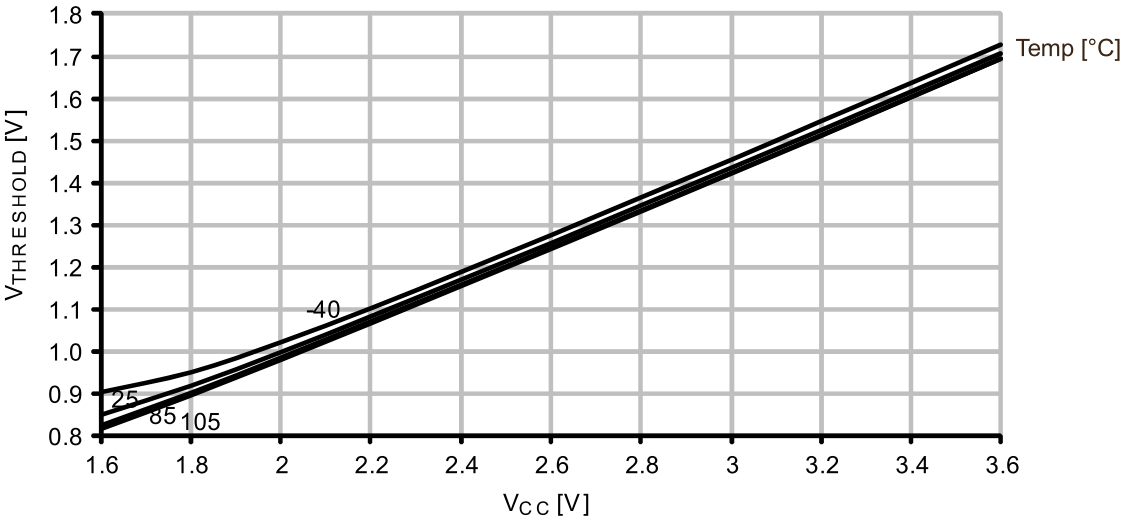


Figure 37-116. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

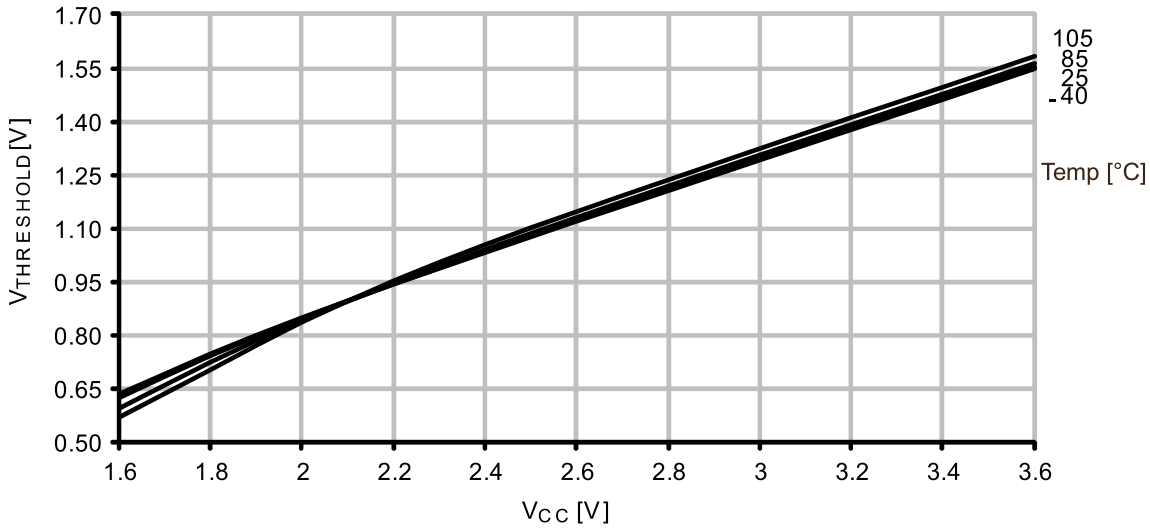
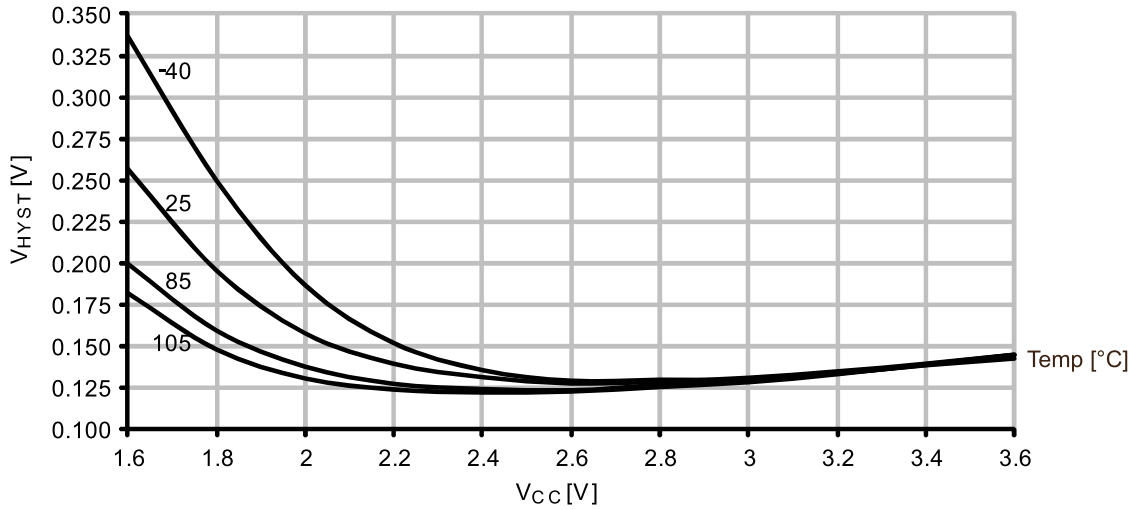


Figure 37-117. I/O pin input hysteresis vs. V_{CC}.



37.2.3 ADC Characteristics

Figure 37-118. INL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

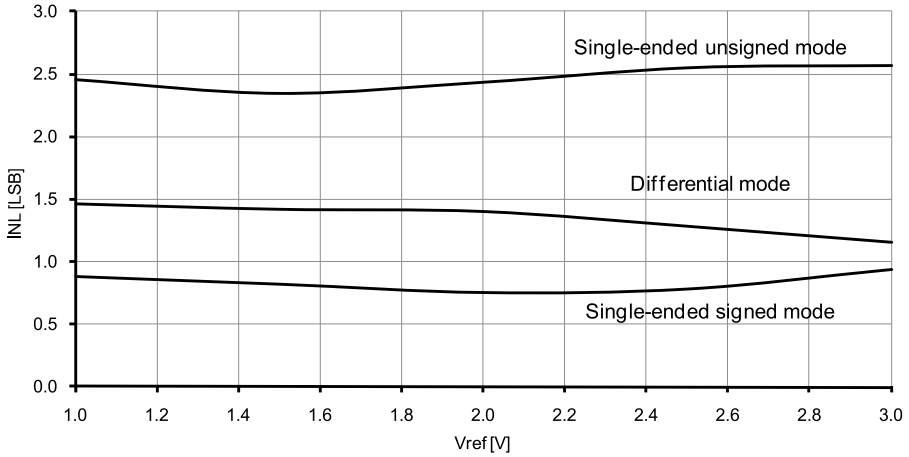


Figure 37-119. INL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

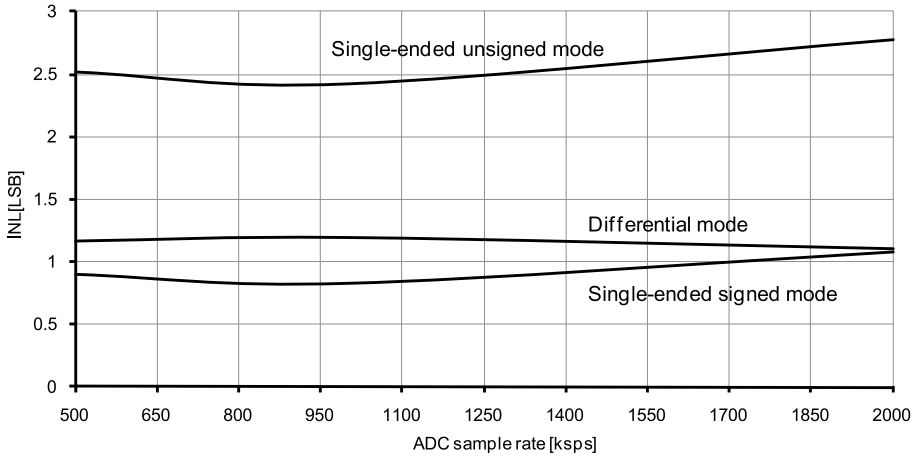


Figure 37-120. INL error vs. input code.

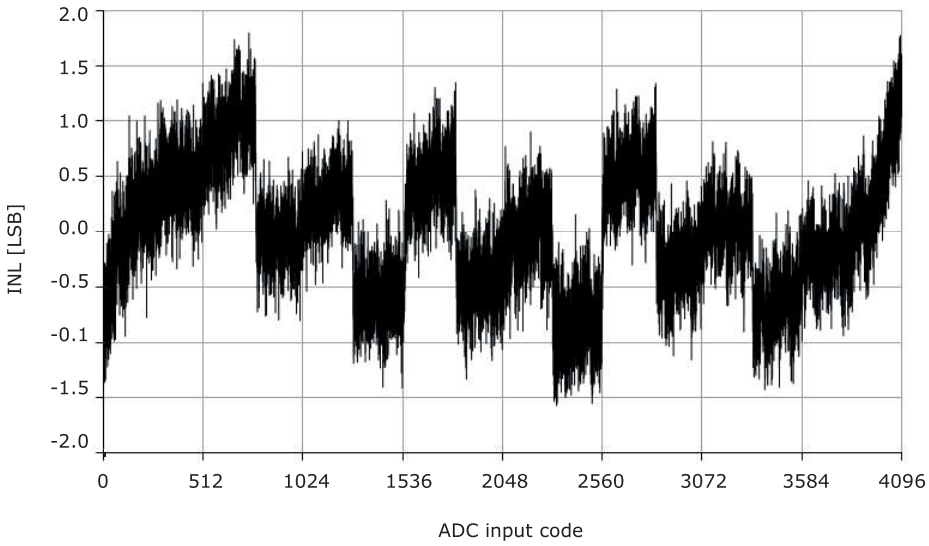


Figure 37-121. DNL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

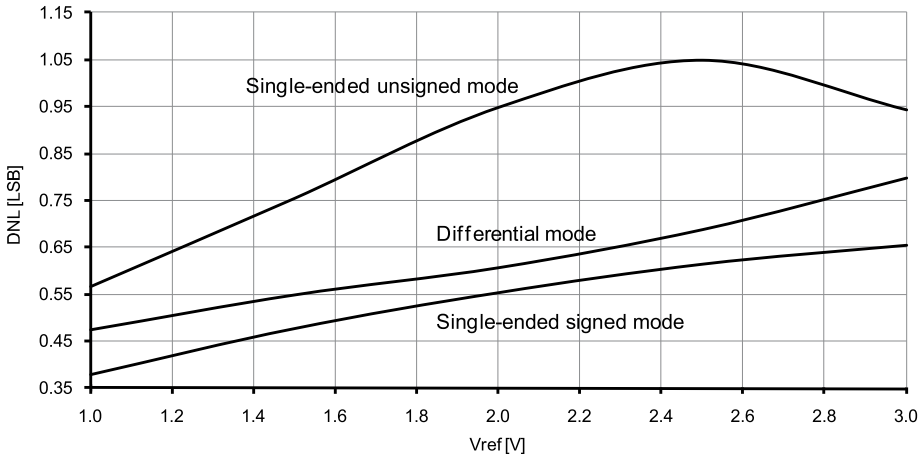


Figure 37-122. DNL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

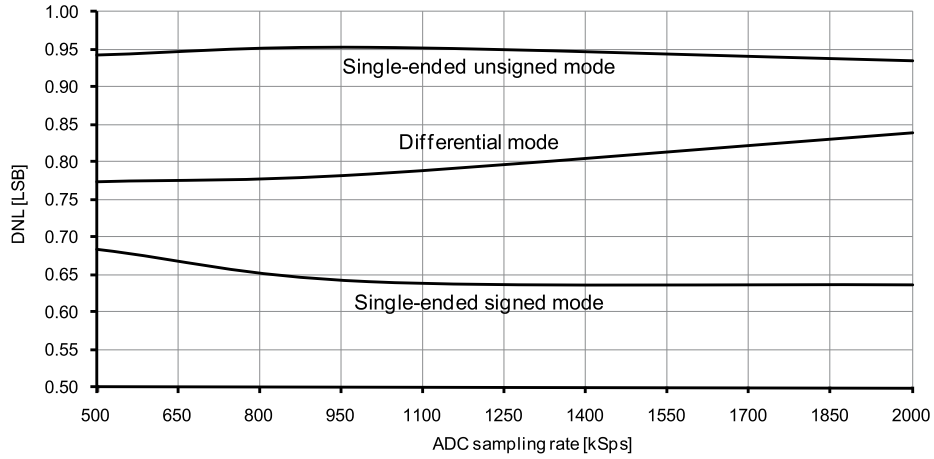


Figure 37-123. DNL error vs. input code.

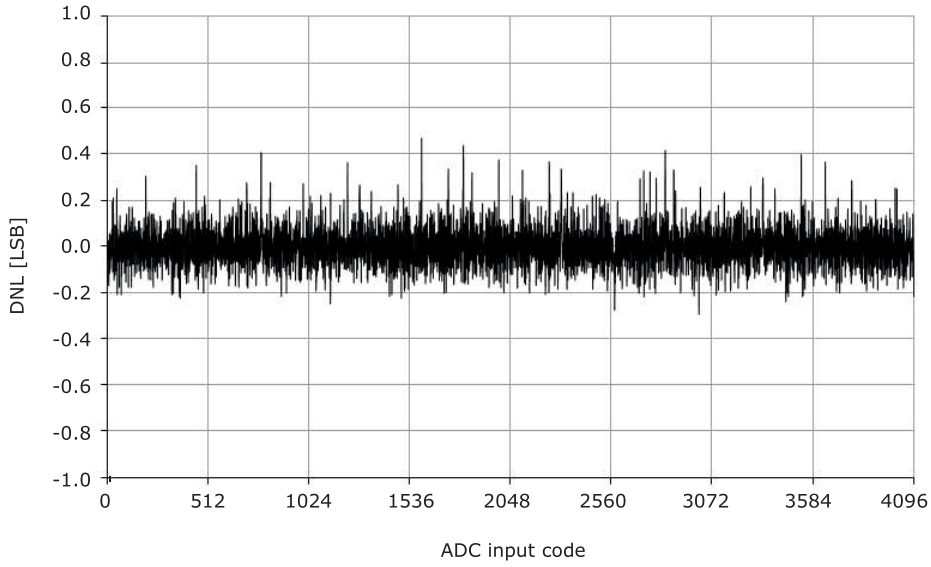


Figure 37-124. Gain error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

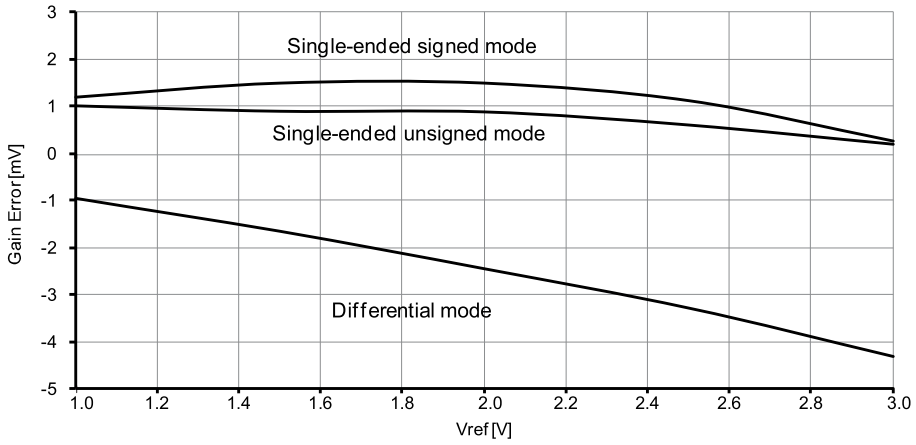


Figure 37-125. Gain error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

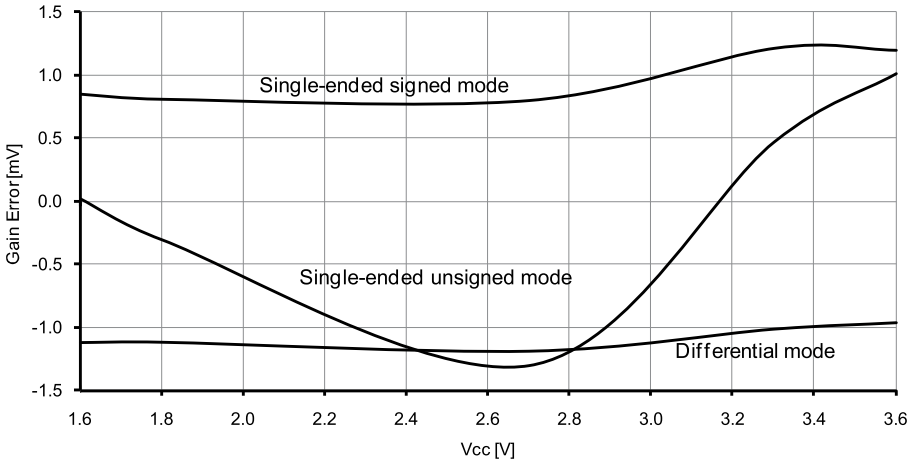


Figure 37-126. Offset error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

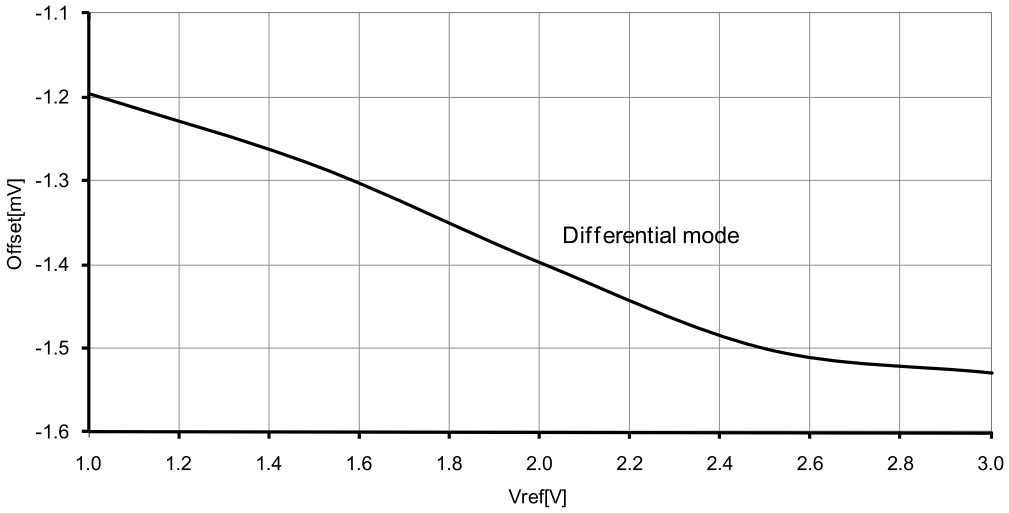


Figure 37-127. Gain error vs. temperature.

V_{CC} = 2.7V, V_{REF} = external 1.0V.

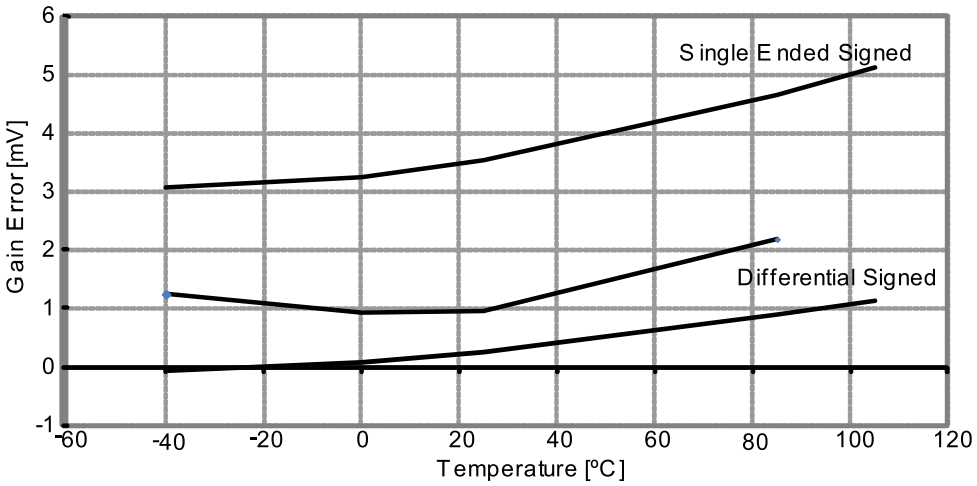


Figure 37-128. Offset error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

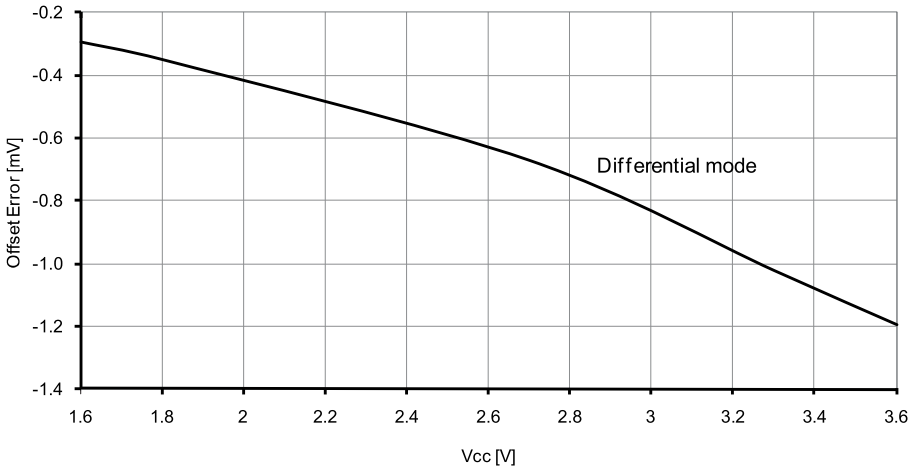


Figure 37-129. Noise vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

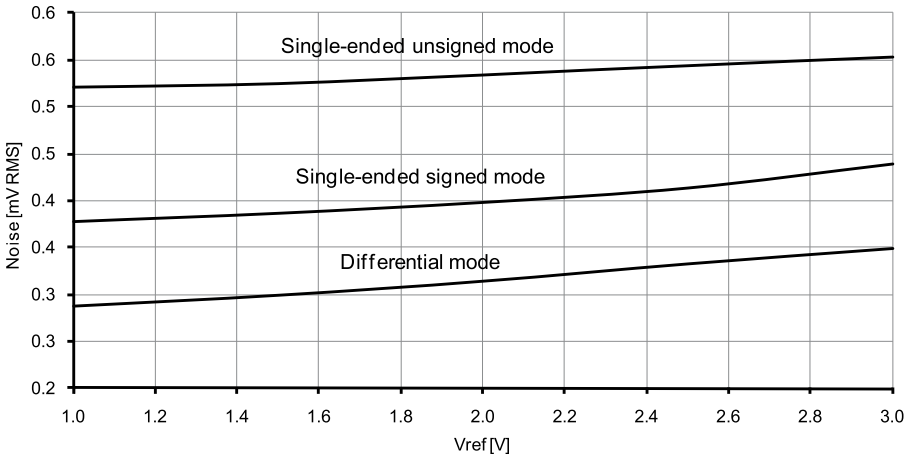
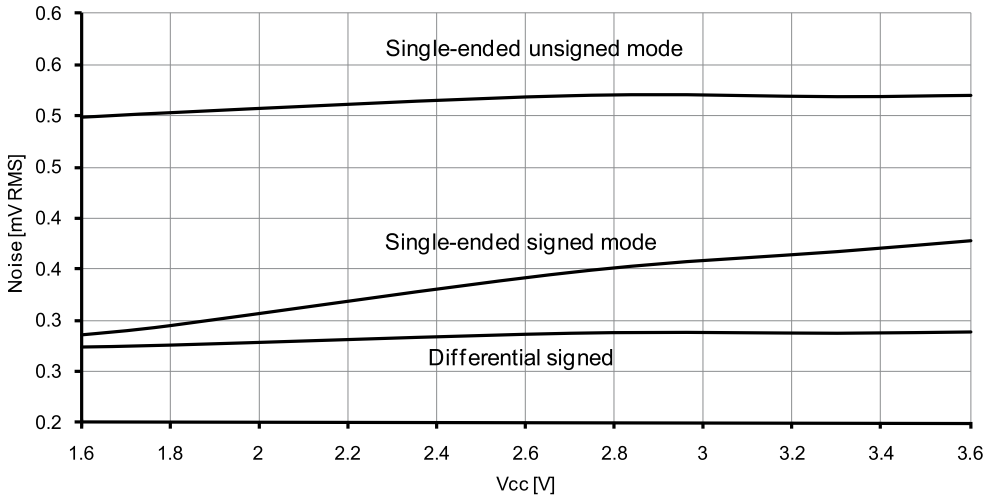


Figure 37-130. Noise vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.



37.2.4 DAC Characteristics

Figure 37-131. DAC INL error vs. V_{REF}.

V_{CC} = 3.6V.

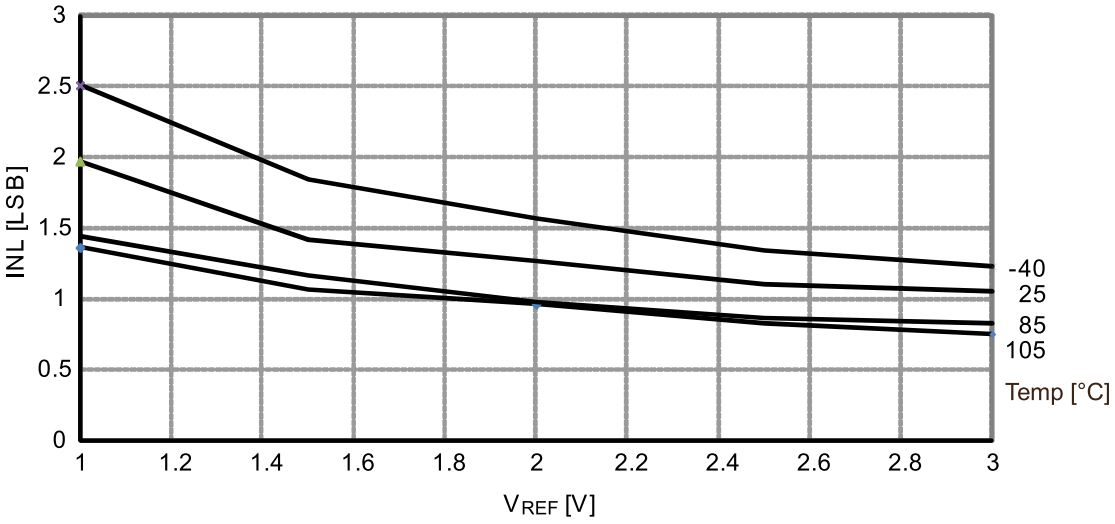


Figure 37-132. DNL error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V.

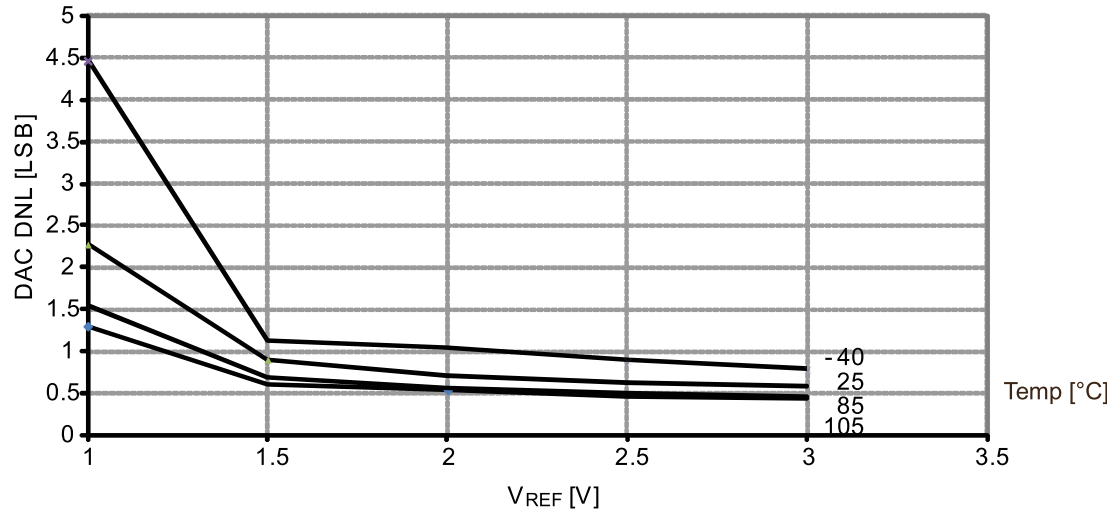
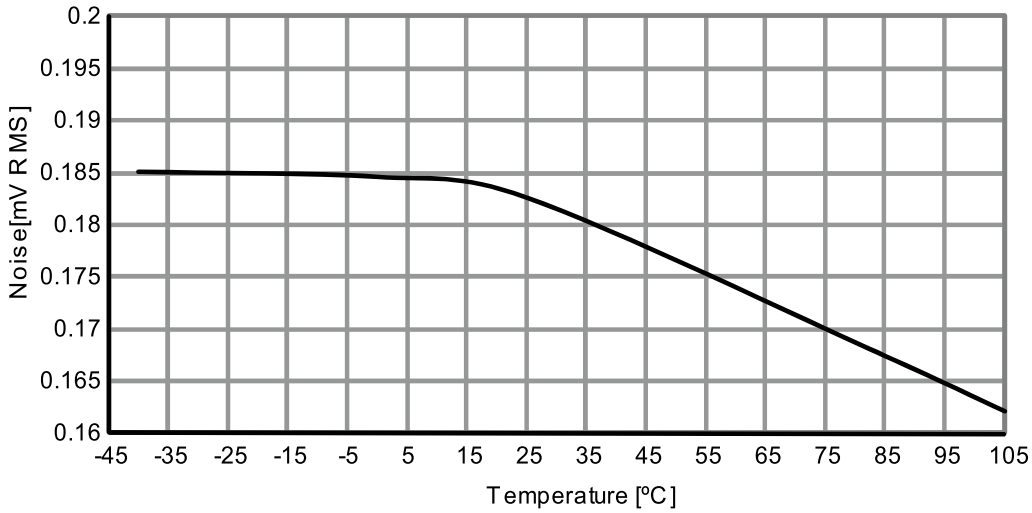


Figure 37-133. DAC noise vs. temperature.

V_{CC} = 3.0V, V_{REF} = 2.0V.



37.2.5 Analog Comparator Characteristics

Figure 37-134. Analog comparator hysteresis vs. V_{CC}.

High-speed, small hysteresis.

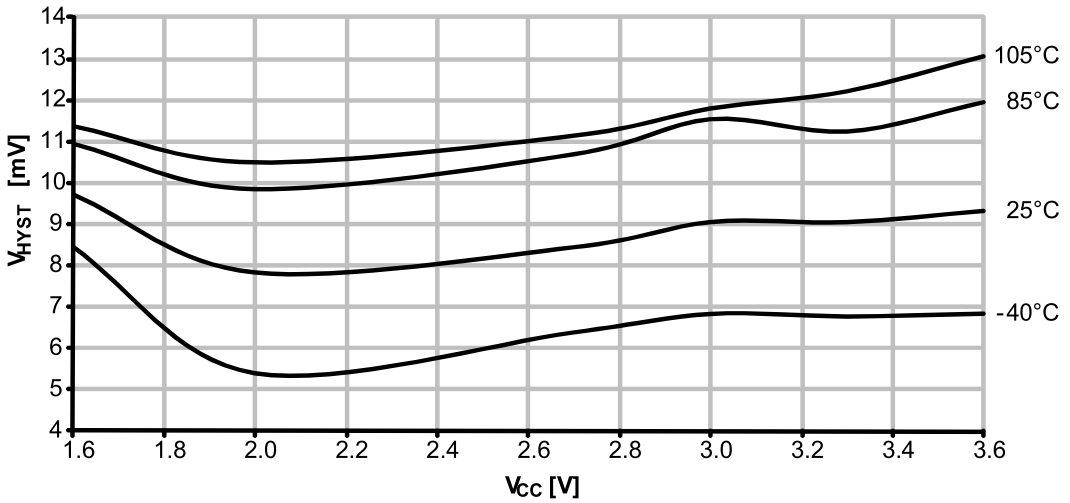


Figure 37-135. Analog comparator hysteresis vs. V_{CC}.

Low power, small hysteresis.

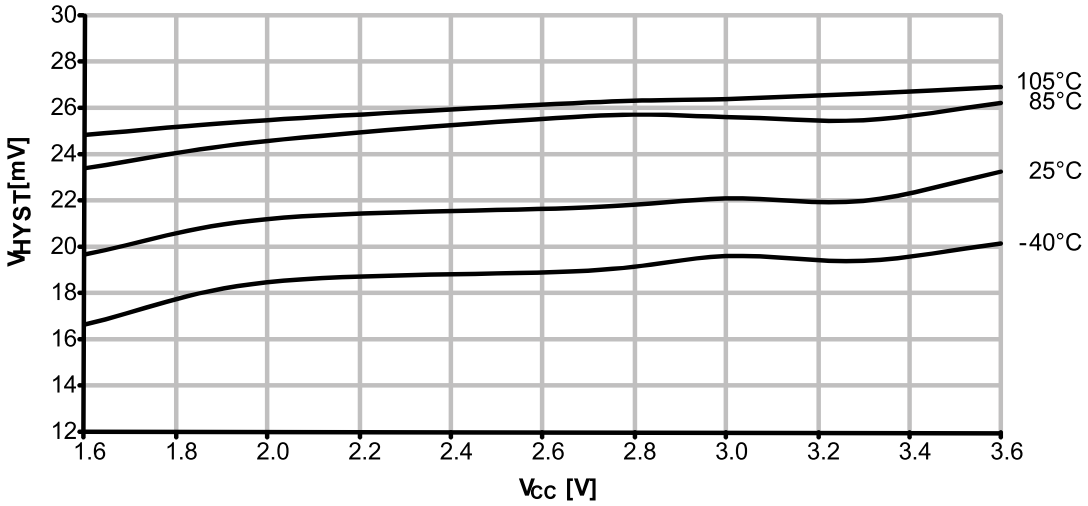


Figure 37-136. Analog comparator hysteresis vs. V_{CC}

High-speed mode, large hysteresis.

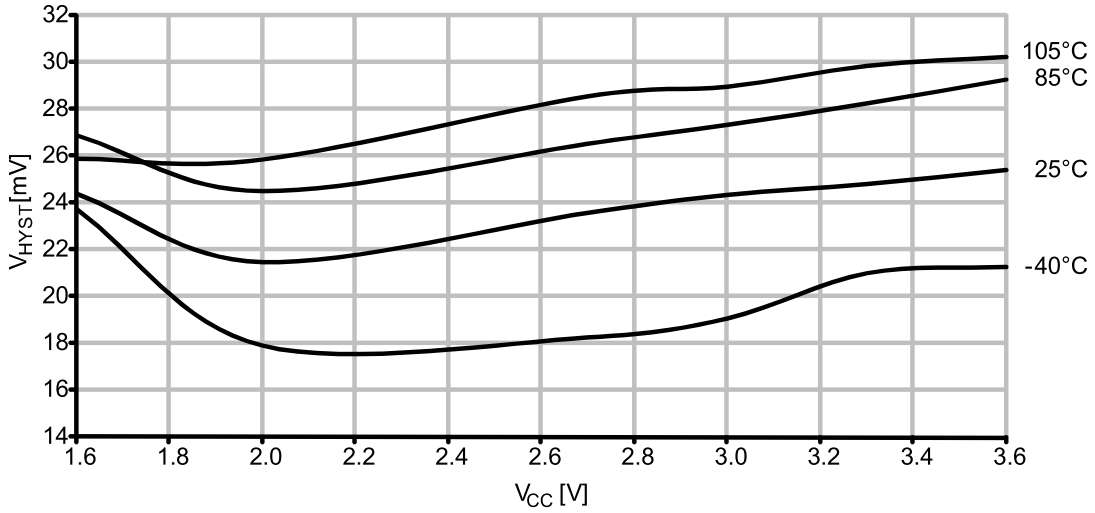


Figure 37-137. Analog comparator hysteresis vs. V_{CC}.

Low power, large hysteresis.

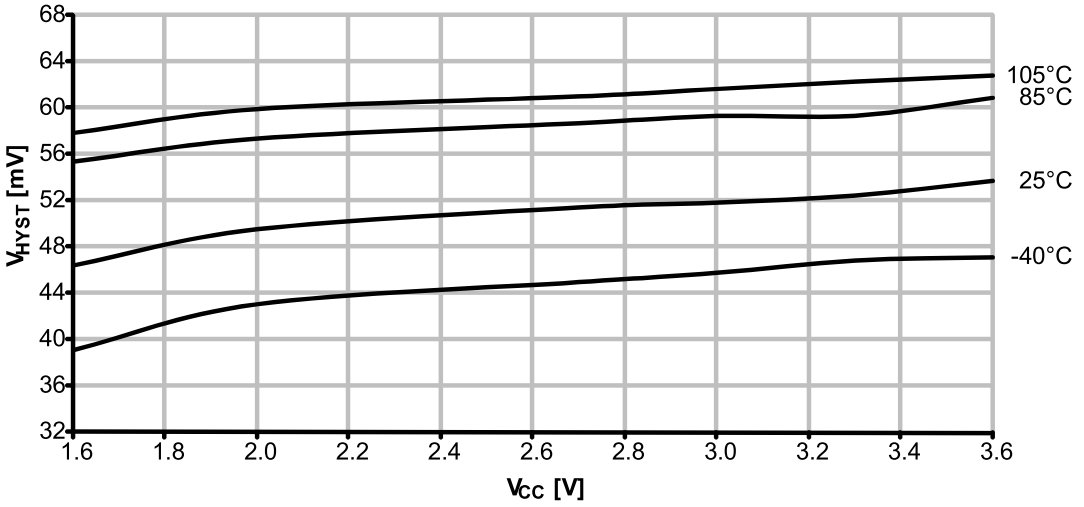


Figure 37-138. Analog comparator current source vs. calibration value.

Temperature = 25°C.

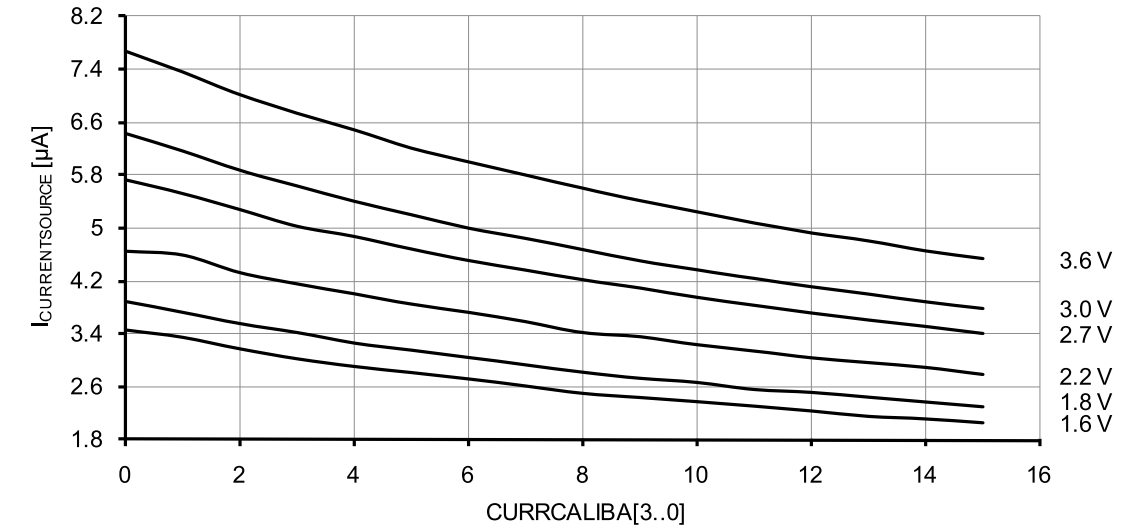


Figure 37-139. Analog comparator current source vs. calibration value.

V_{CC} = 3.0V.

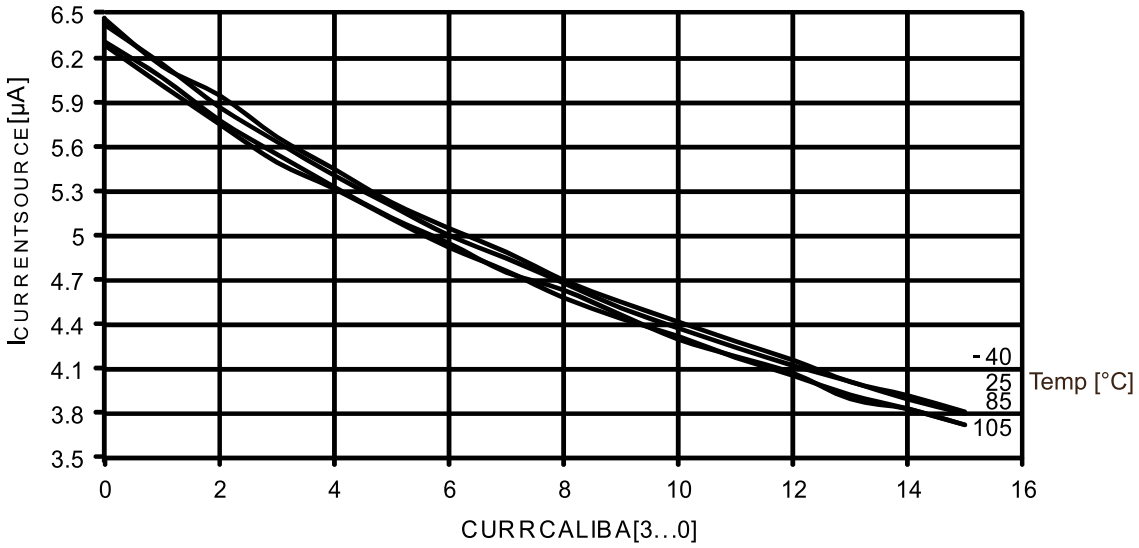
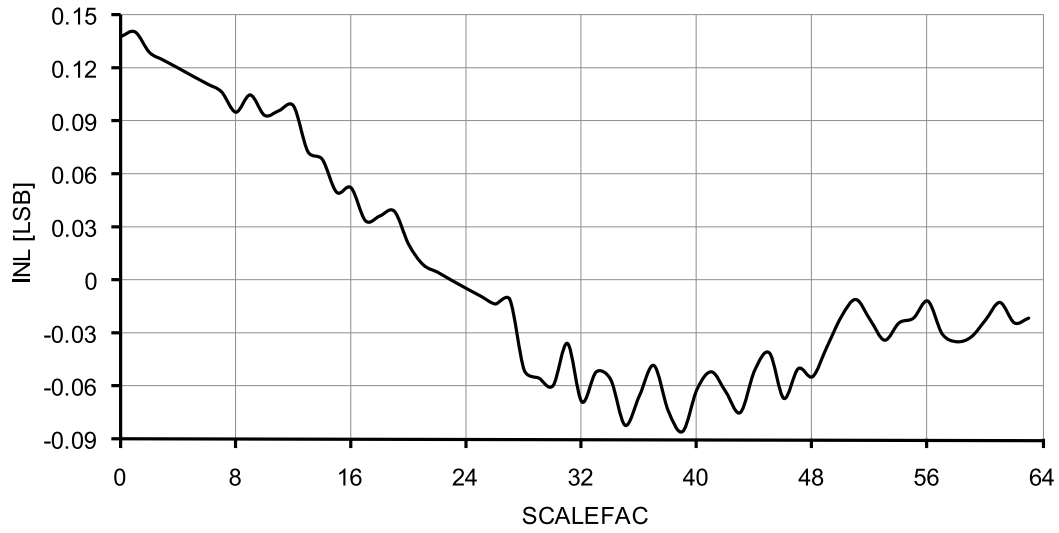


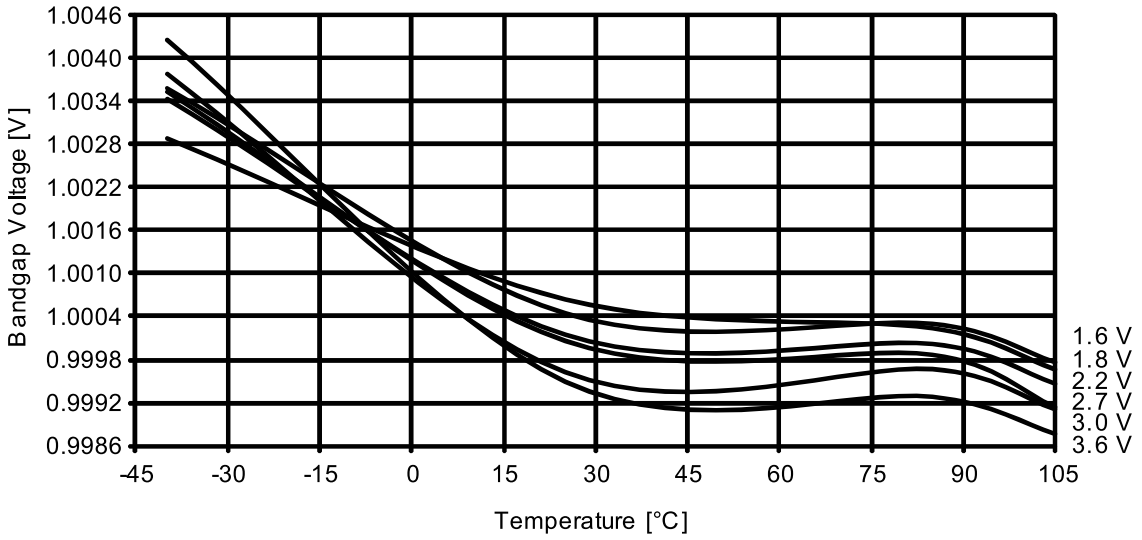
Figure 37-140. Voltage scaler INL vs. SCALEFAC.

T = 25°C, V_{CC} = 3.0V.



37.2.6 Internal 1.0V reference Characteristics

Figure 37-141. ADC/DAC Internal 1.0V reference vs. temperature.



37.2.7 BOD Characteristics

Figure 37-142. BOD thresholds vs. temperature.

BOD level = 1.6V.

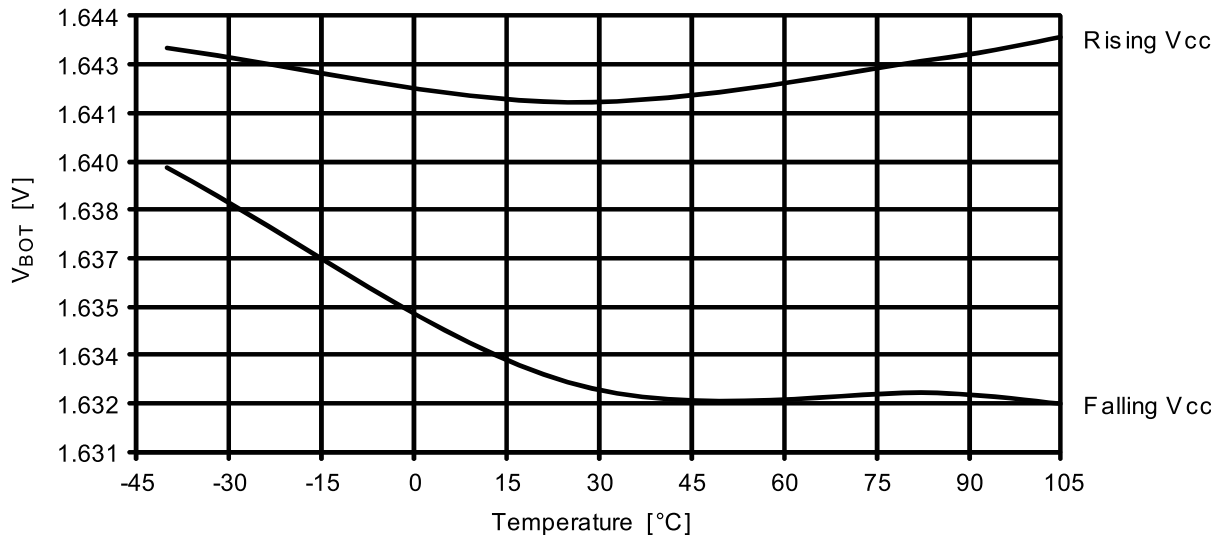
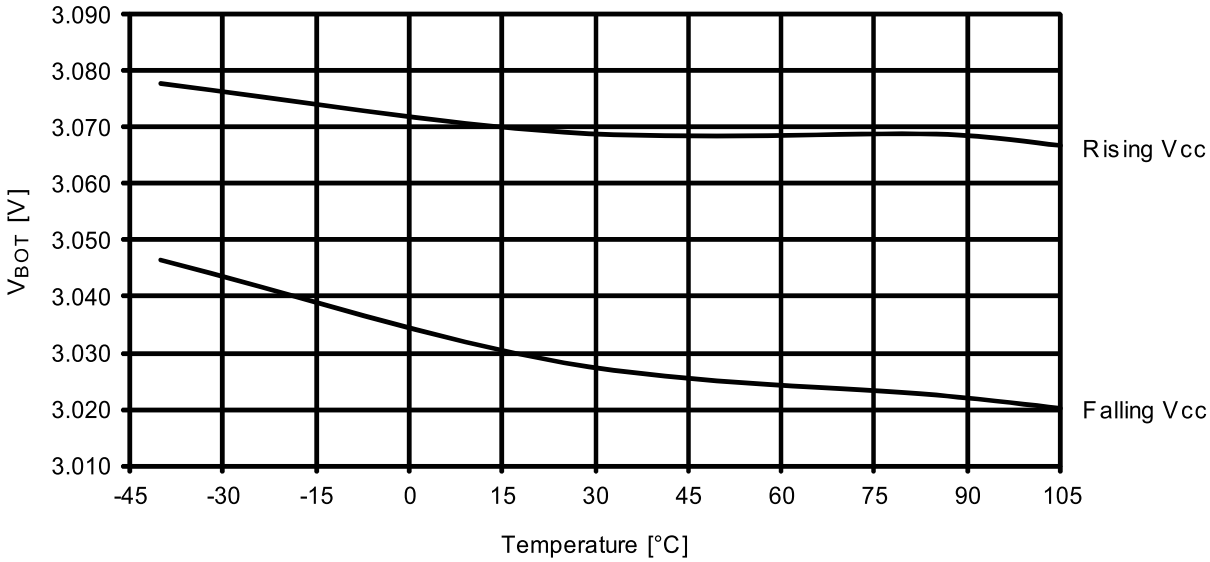


Figure 37-143. BOD thresholds vs. temperature.

BOD level = 3.0V.



37.2.8 External Reset Characteristics

Figure 37-144. Minimum Reset pin pulse width vs. V_{CC}.

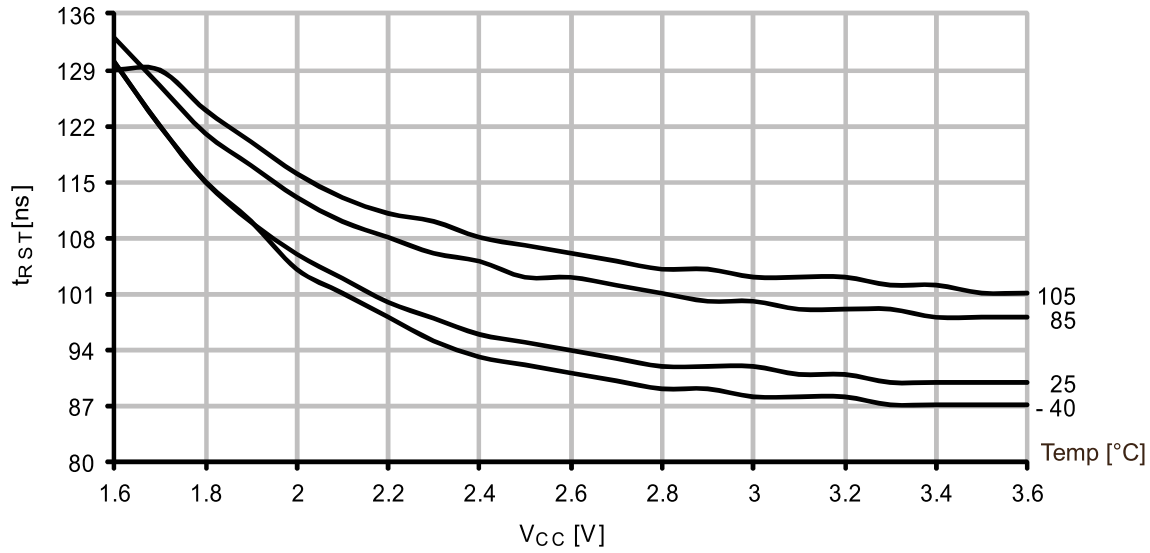


Figure 37-145. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 1.8V.

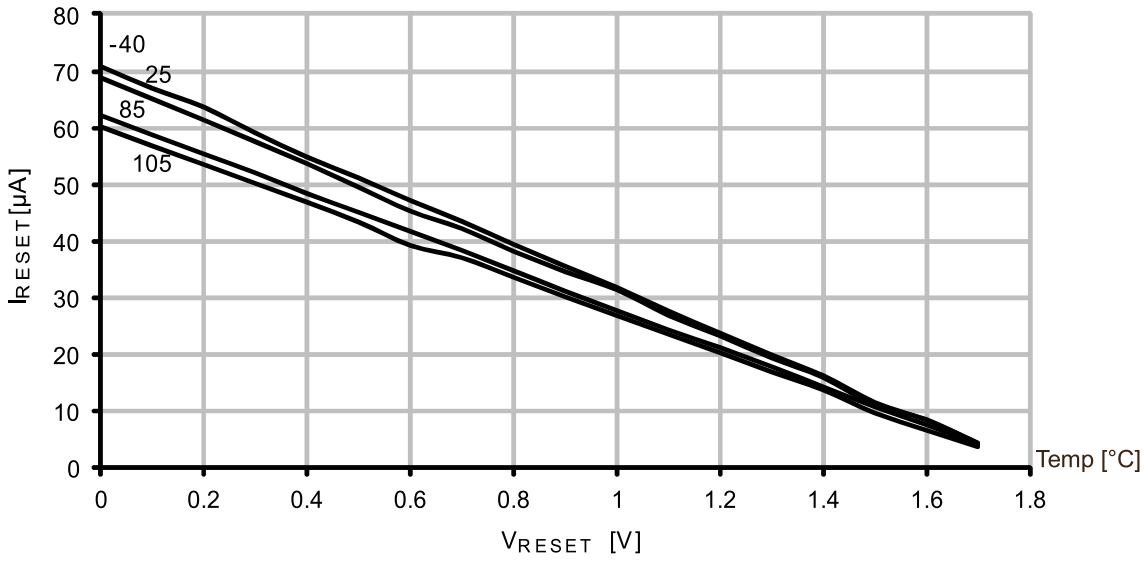


Figure 37-146. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.0V.

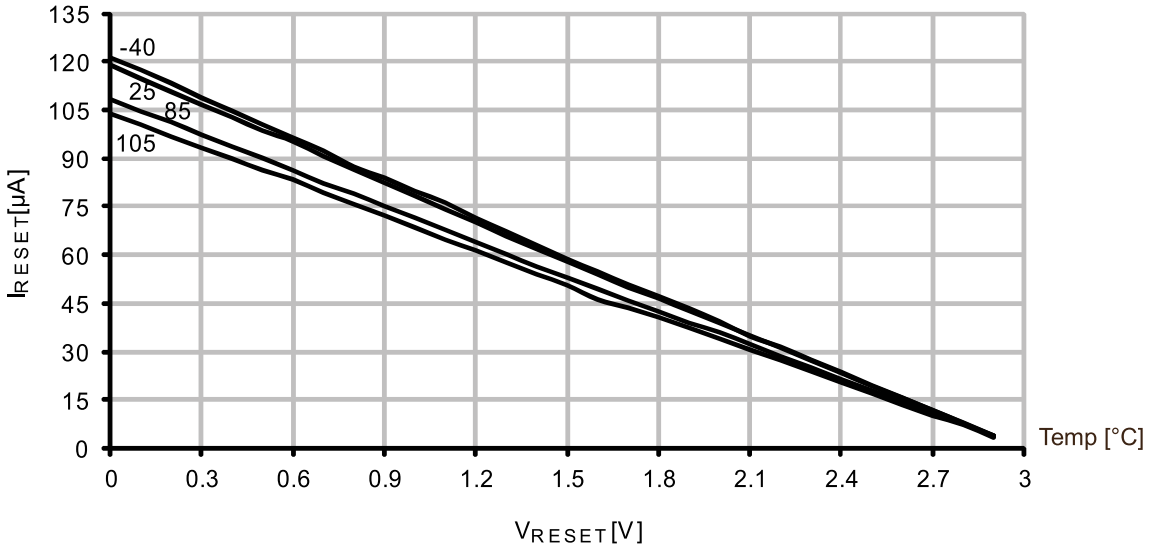


Figure 37-147. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.3V.

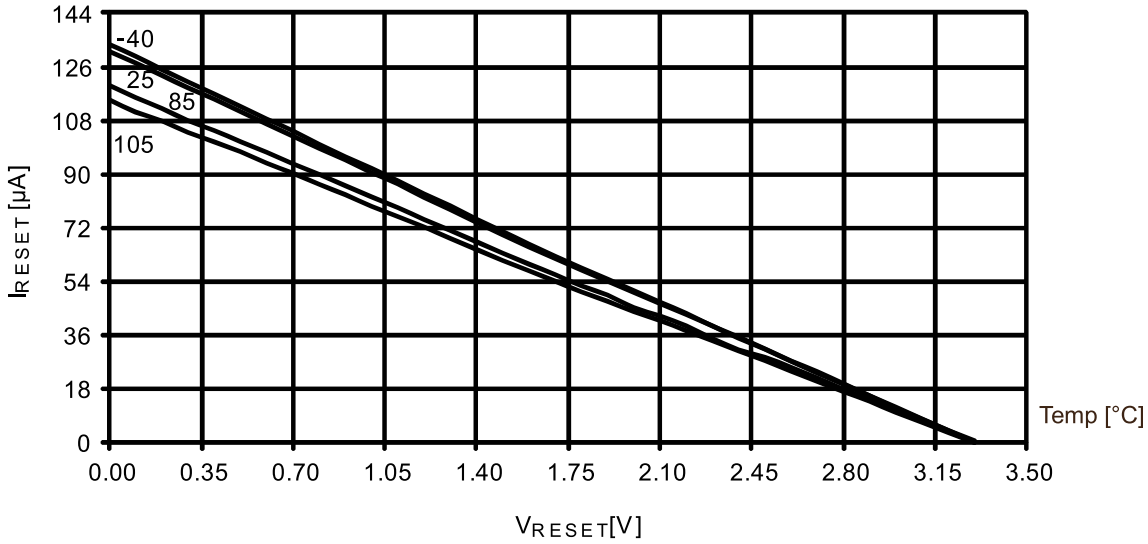


Figure 37-148. Reset pin input threshold voltage vs. V_{CC}.

V_{IH} - Reset pin read as "1".

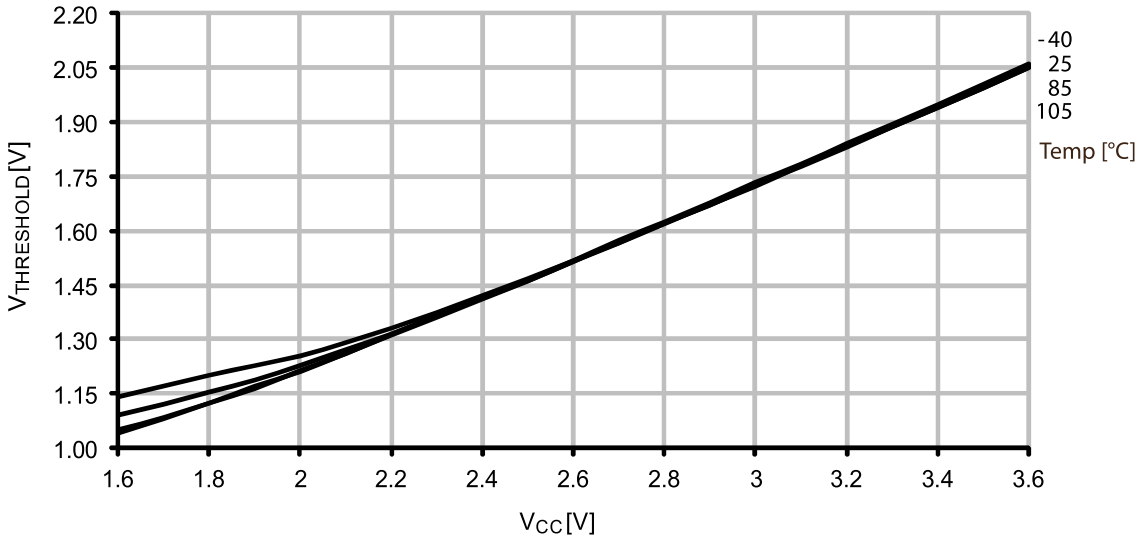
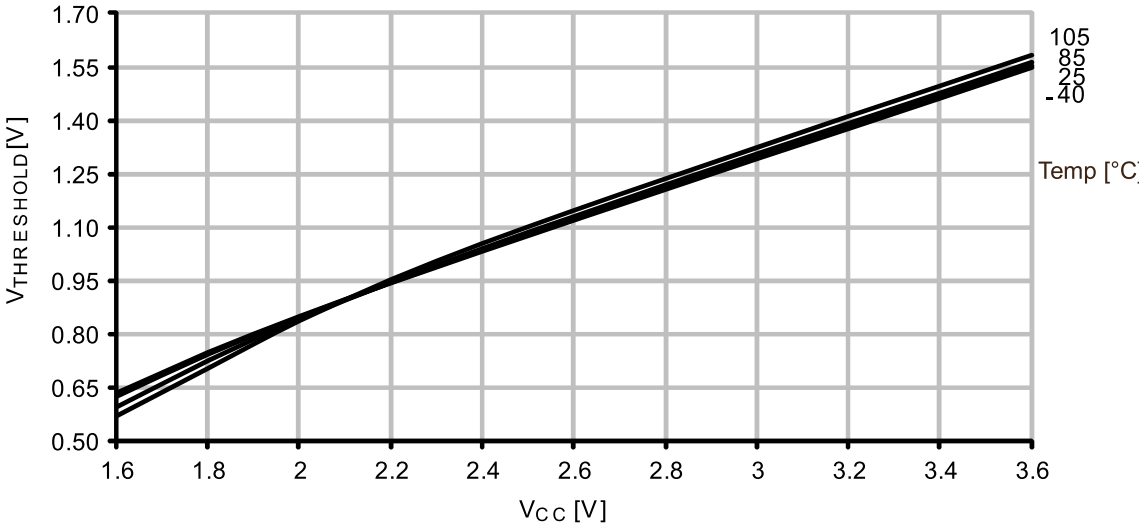


Figure 37-149. Reset pin input threshold voltage vs. V_{CC}.

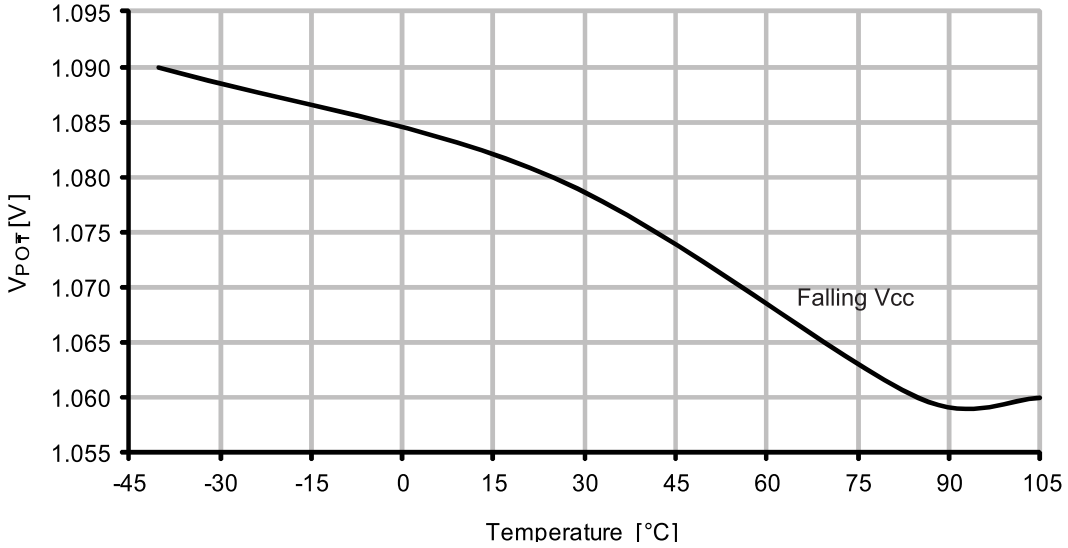
V_{IL} - Reset pin read as "0".



37.2.9 Power-on Reset Characteristics

Figure 37-150. Power-on reset current consumption vs. V_{CC}.

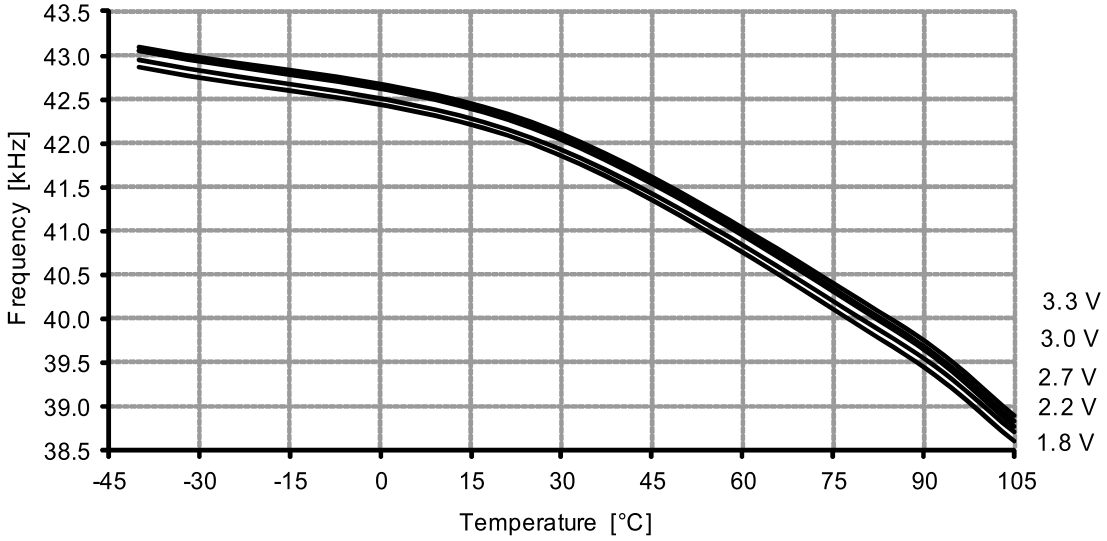
BOD level = 3.0V, enabled in continuous mode.



37.2.10 Oscillator Characteristics

37.2.10.1 Ultra Low-Power internal oscillator

Figure 37-151. Ultra Low-Power internal oscillator frequency vs. temperature.



37.2.10.2 32.768kHz Internal Oscillator

Figure 37-152. 32.768kHz internal oscillator frequency vs. temperature.

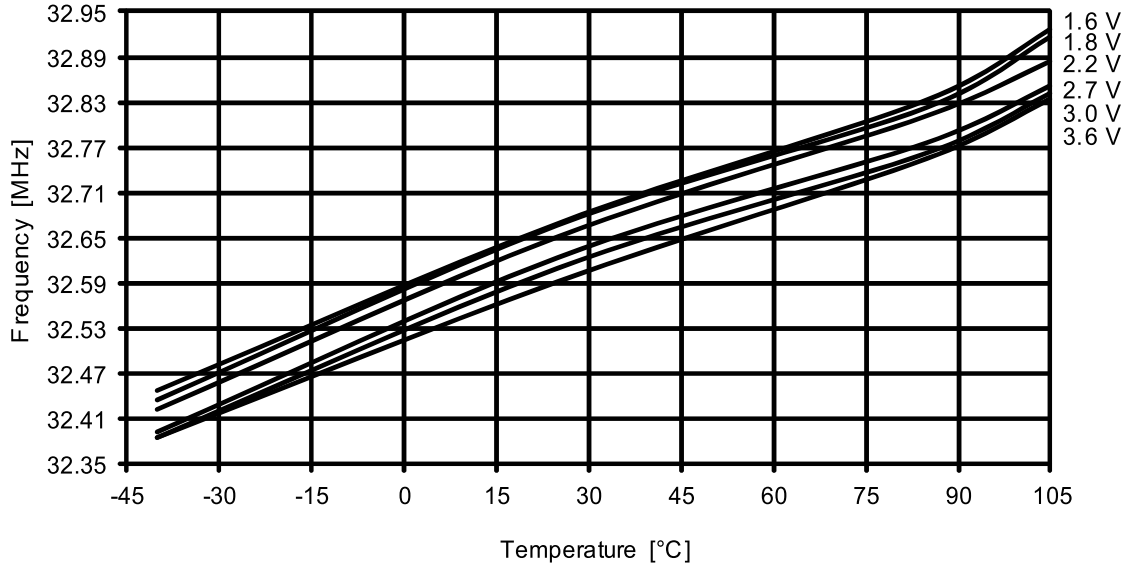
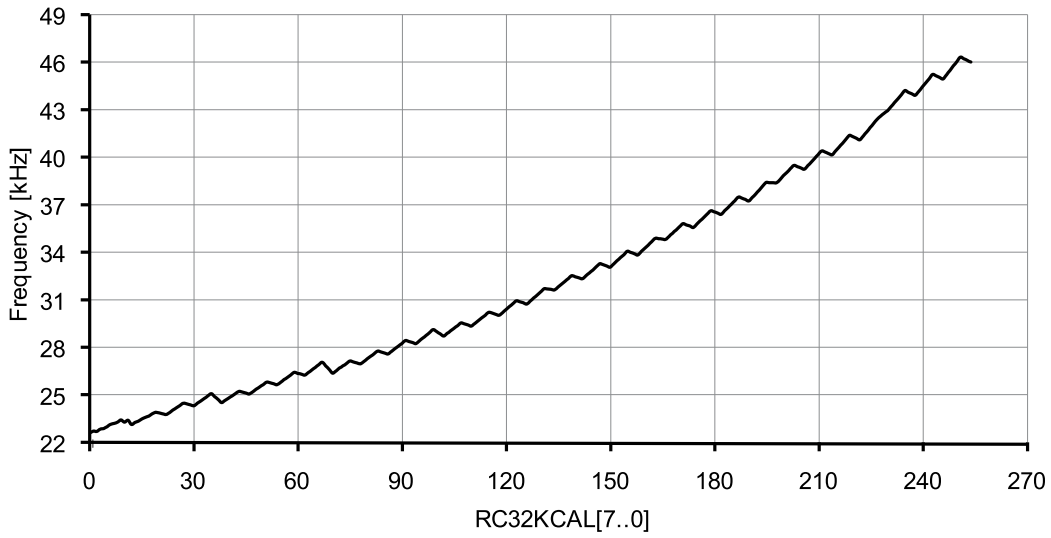


Figure 37-153. 32.768kHz internal oscillator frequency vs. calibration value.

V_{CC} = 3.0V, T = 25°C.



37.2.10.3 2MHz Internal Oscillator

Figure 37-154. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

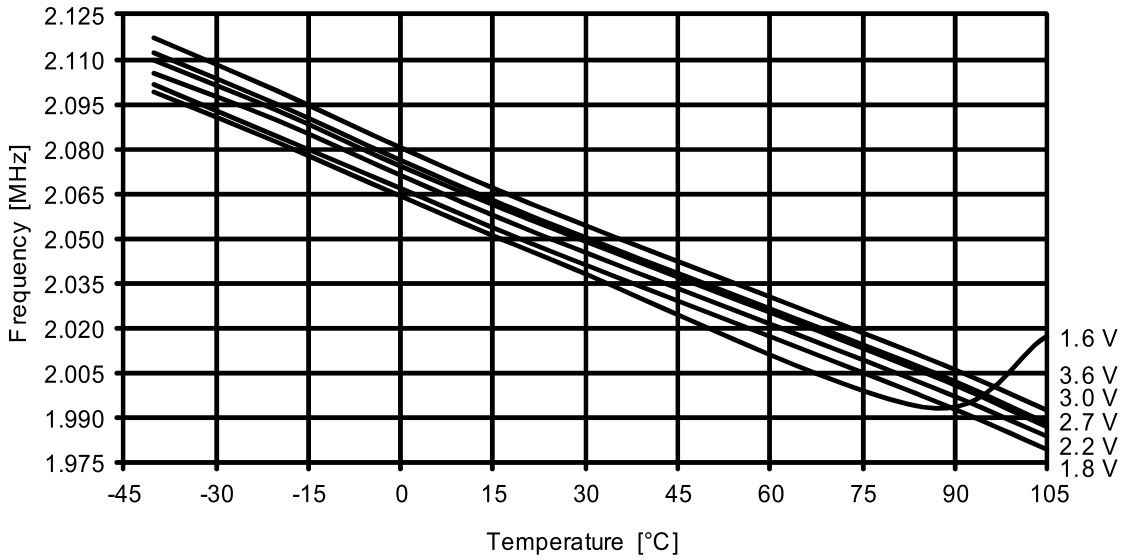


Figure 37-155. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.

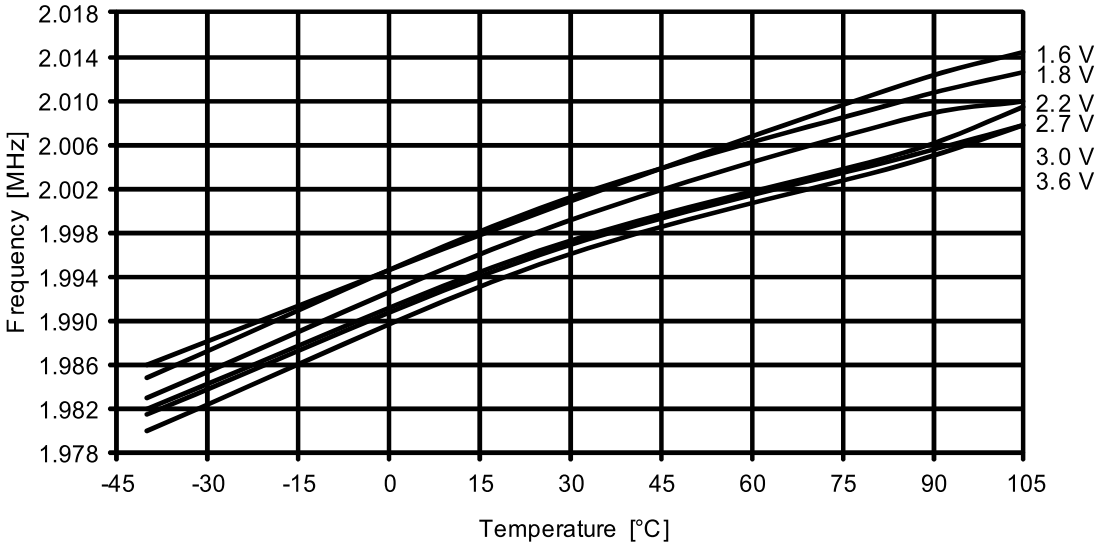
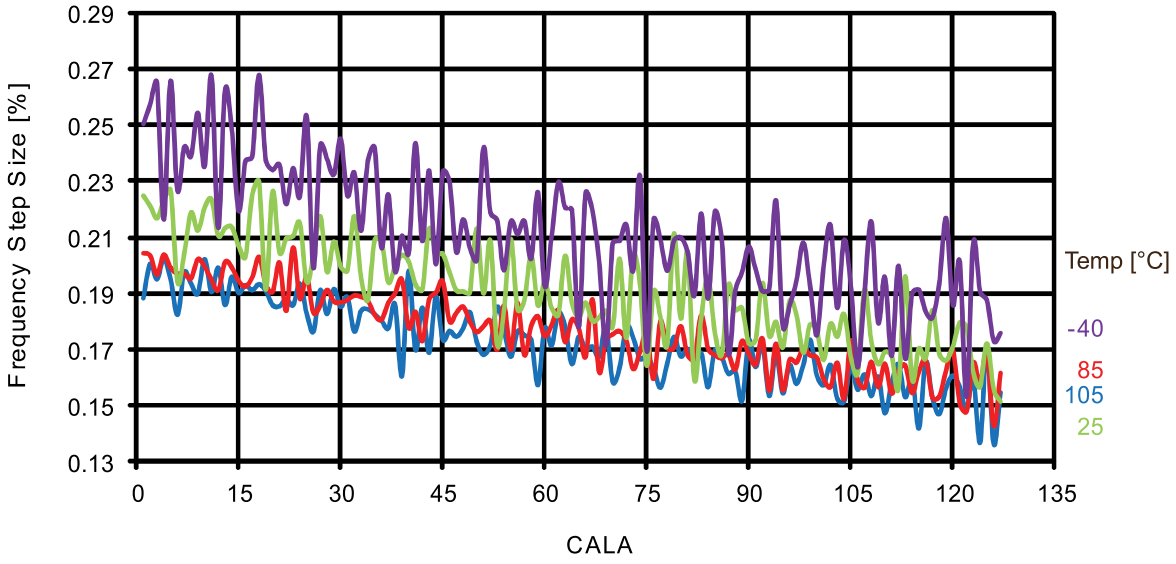


Figure 37-156. 2MHz internal oscillator CALA calibration step size.

V_{CC} = 3V.



37.2.10.4 32MHz Internal Oscillator

Figure 37-157. 32MHz internal oscillator frequency vs. temperature.
DFLL disabled.

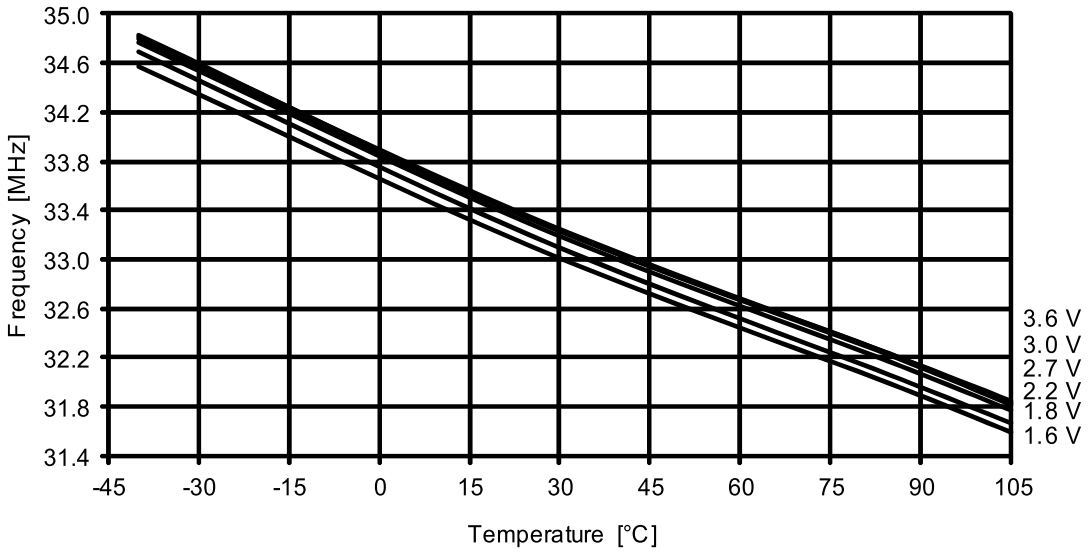


Figure 37-158. 32MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.

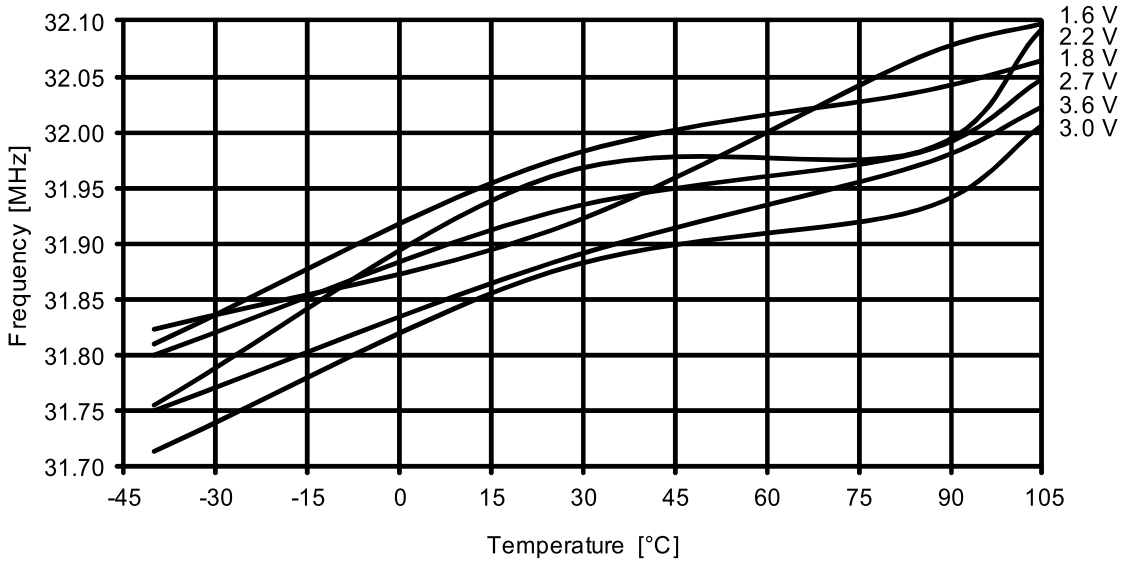


Figure 37-159. 32MHz internal oscillator CALA calibration step size.

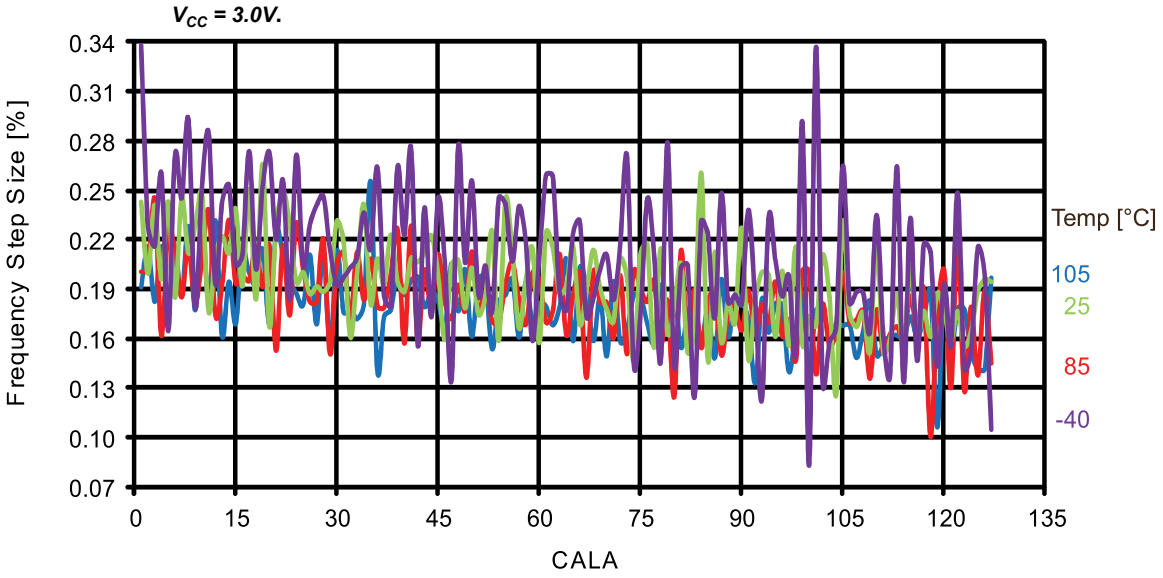
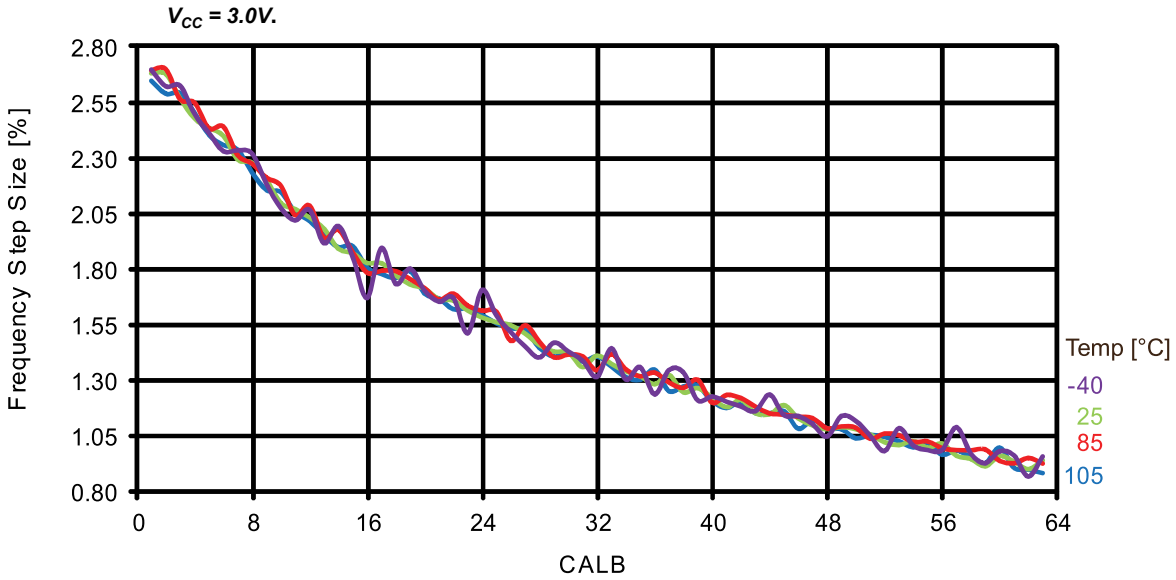


Figure 37-160. 32MHz internal oscillator frequency vs. CALB calibration value.



37.2.10.5 32MHz internal oscillator calibrated to 48MHz

Figure 37-161. 48MHz internal oscillator frequency vs. temperature.

DFLL disabled.

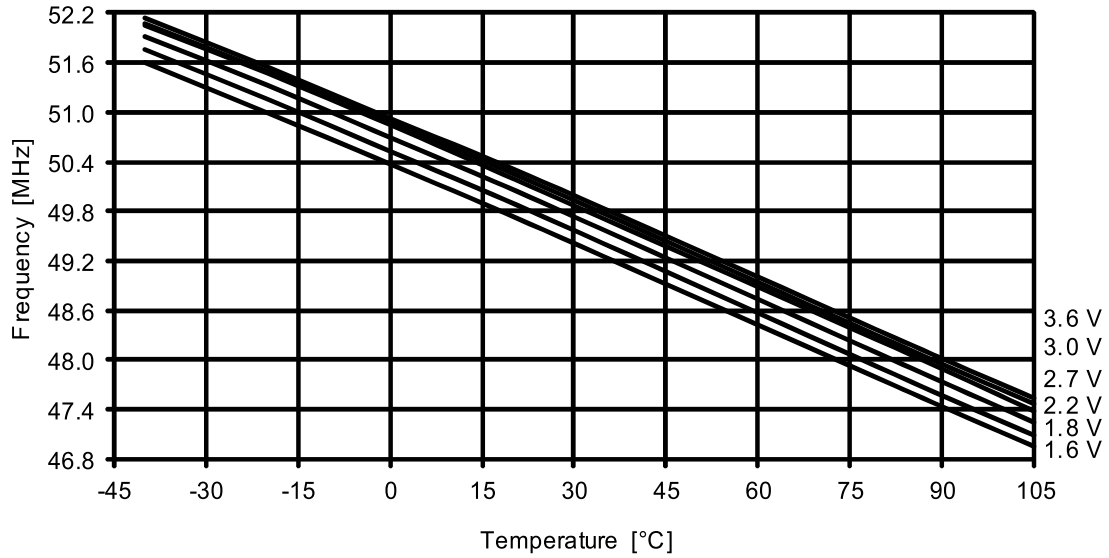


Figure 37-162. 48MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.

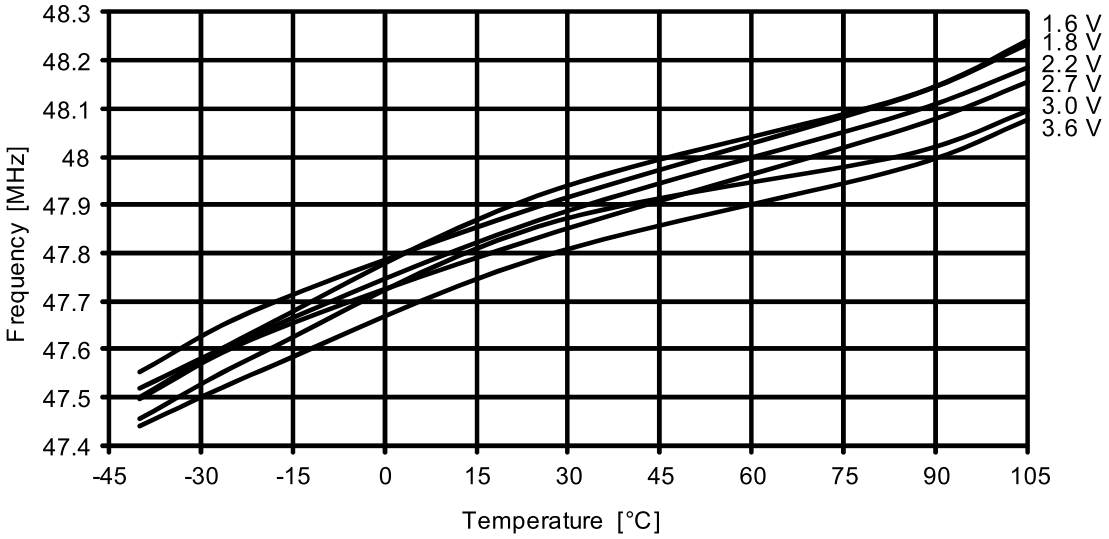
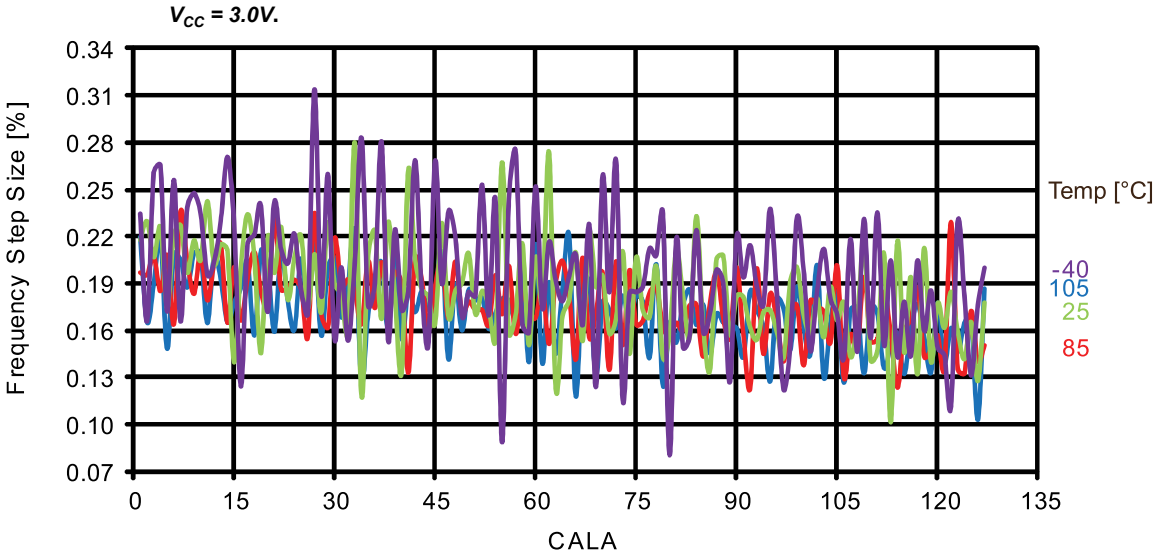


Figure 37-163. 48MHz internal oscillator CALA calibration step size.



37.2.11 Two-Wire Interface characteristics

Figure 37-164. SDA hold time vs. Vcc.

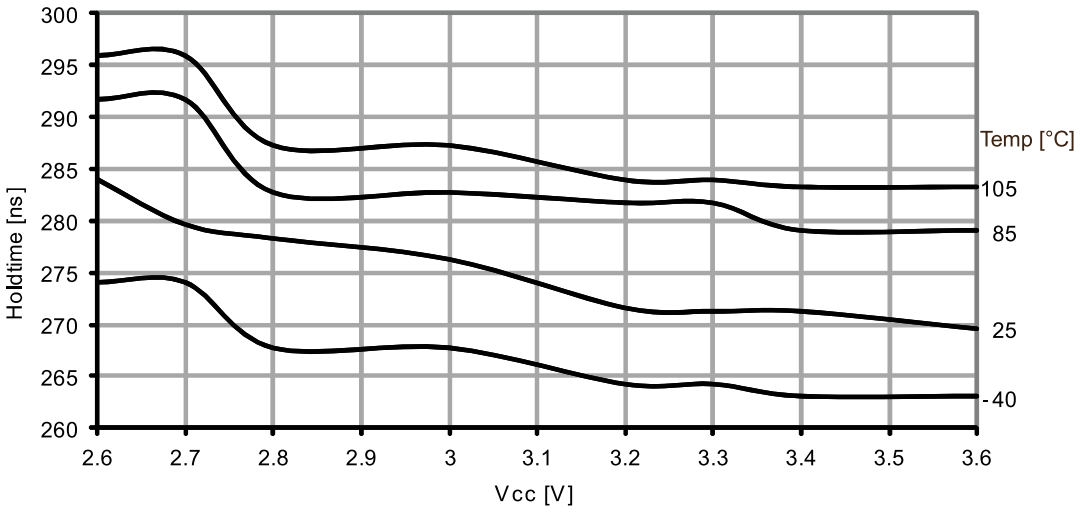
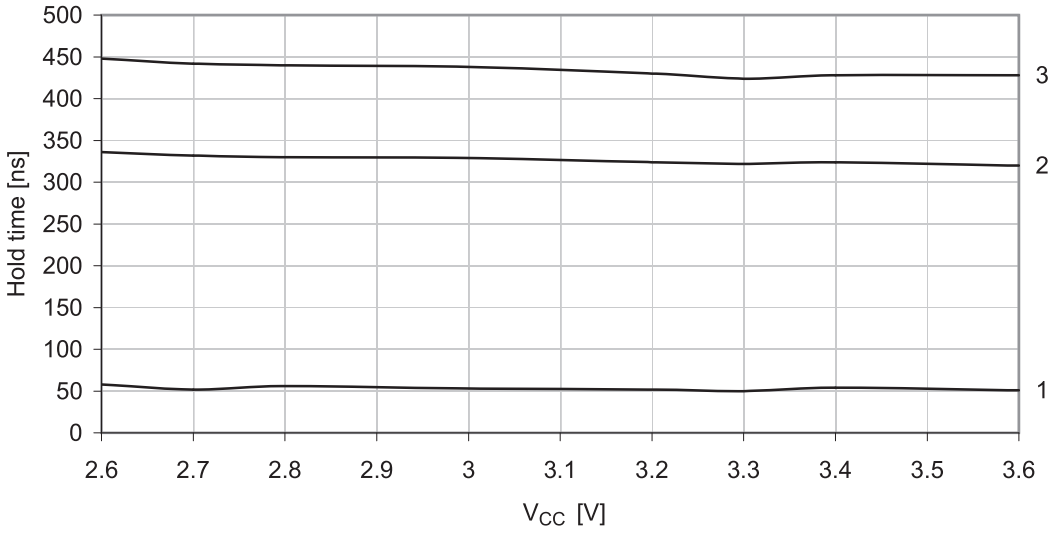
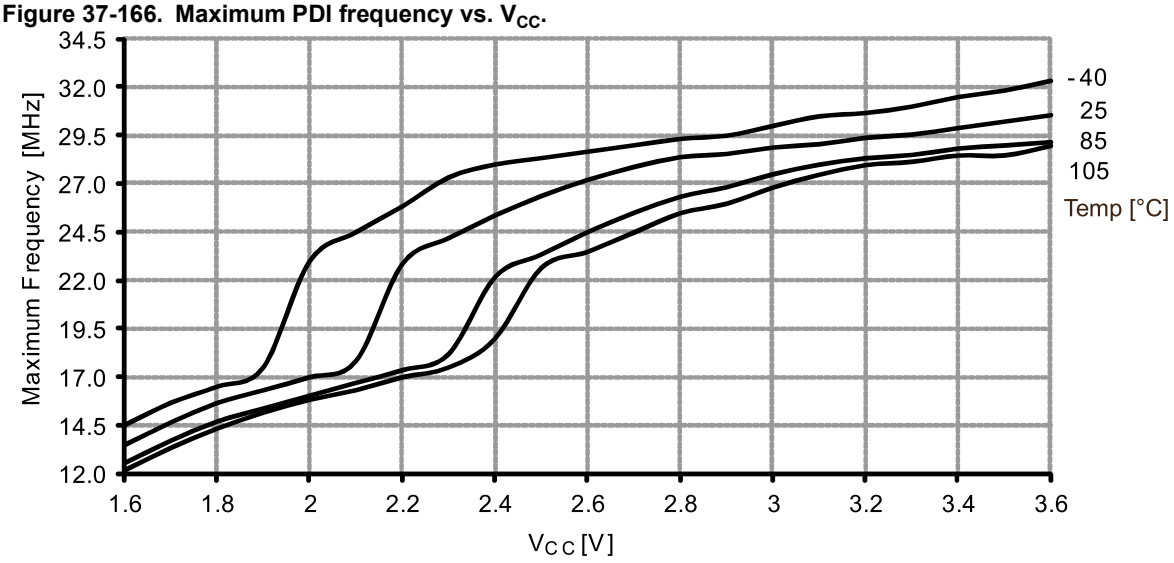


Figure 37-165. SDA hold time vs. supply voltage.



37.2.12 PDI characteristics

Figure 37-166. Maximum PDI frequency vs. V_{CC}.



37.3 ATxmega192A3U

37.3.1 Current consumption

37.3.1.1 Active mode supply current

Figure 37-167. Active supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

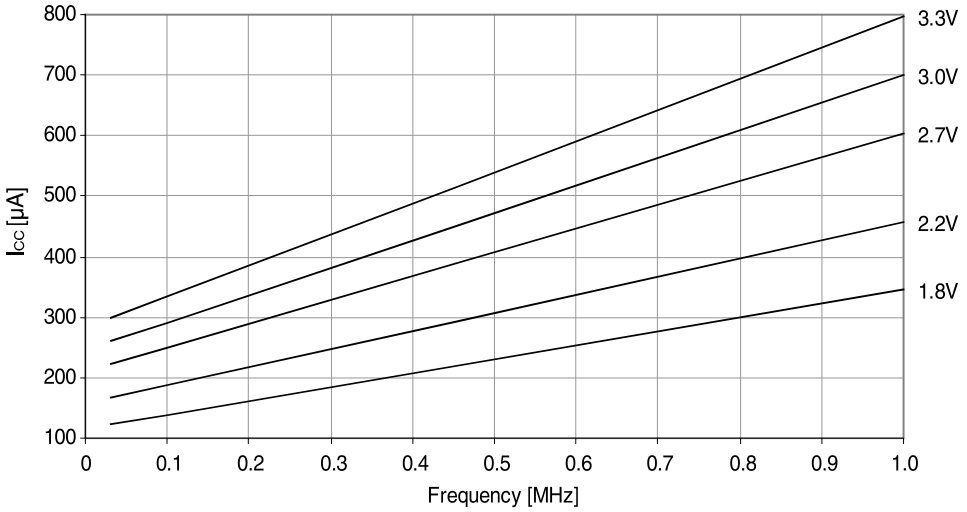


Figure 37-168. Active supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

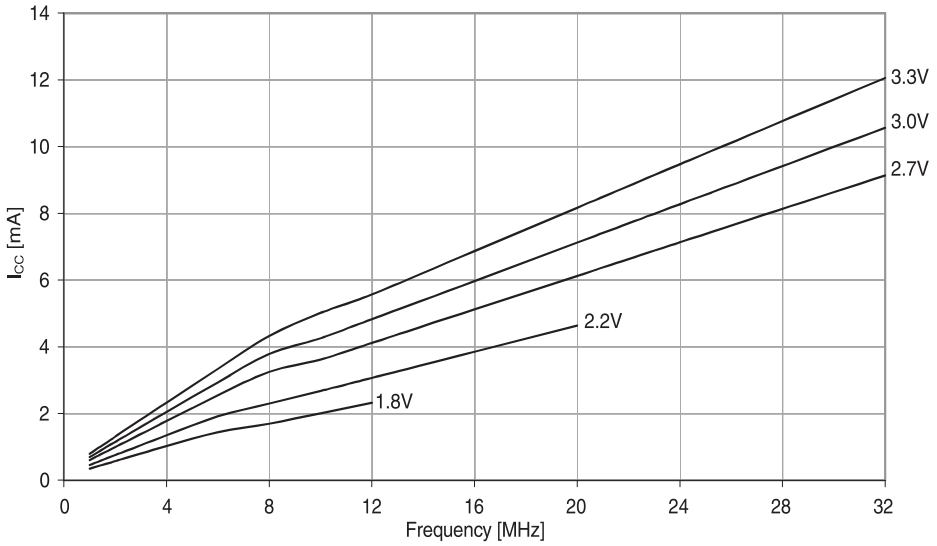


Figure 37-169. Active mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

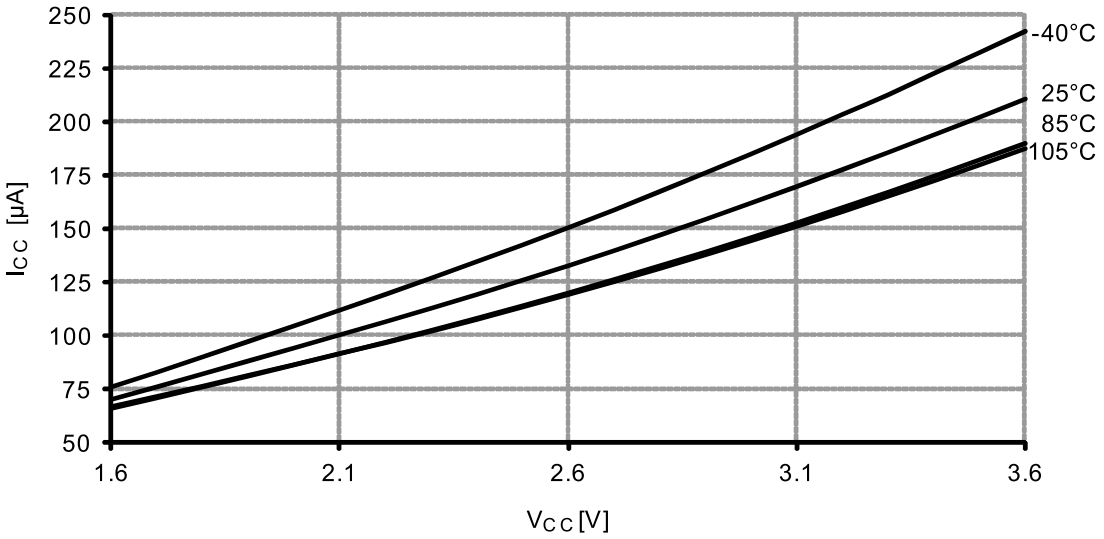


Figure 37-170. Active mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

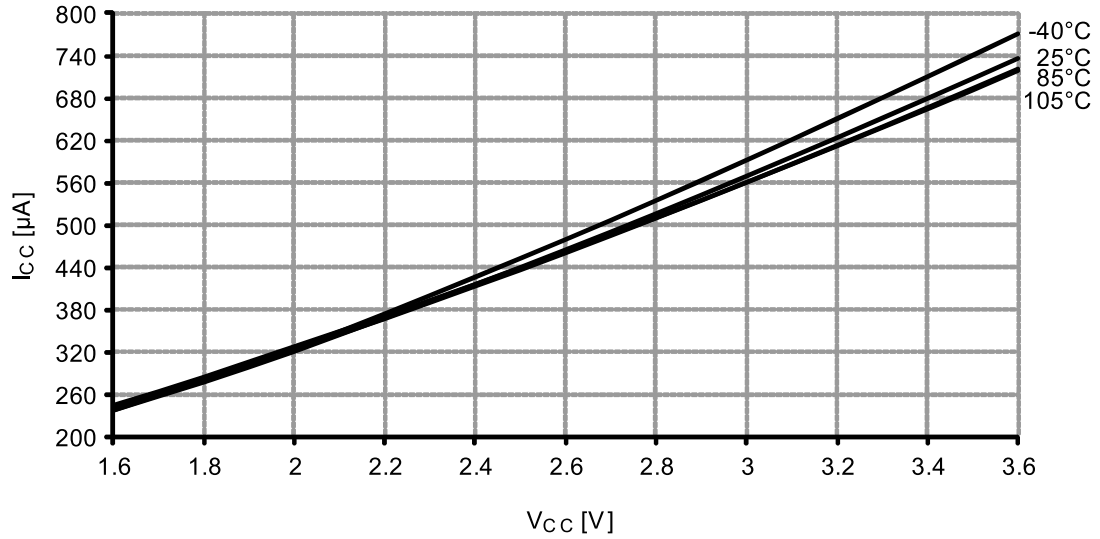


Figure 37-171. Active mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

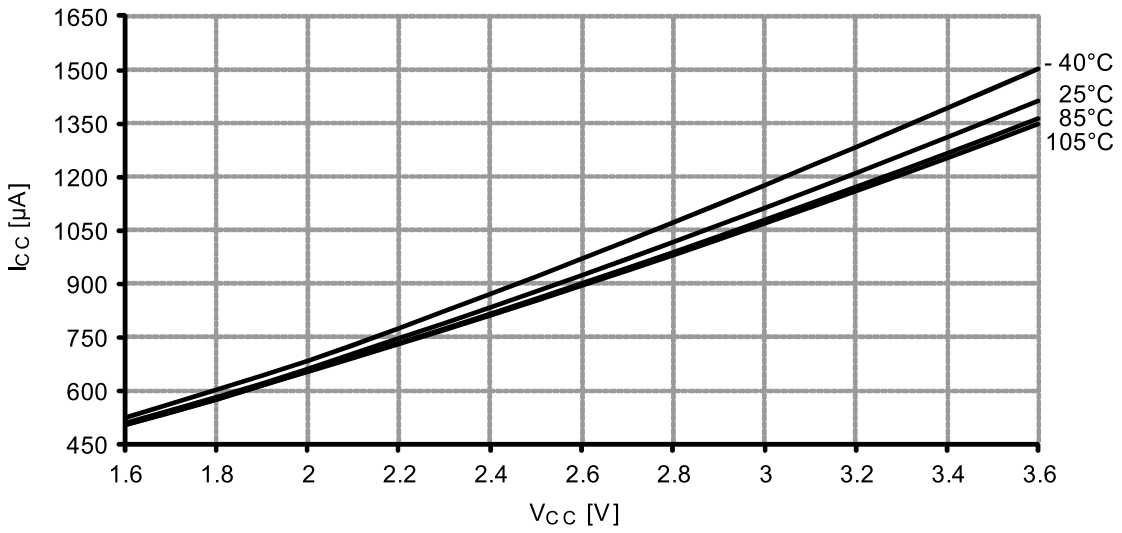


Figure 37-172. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

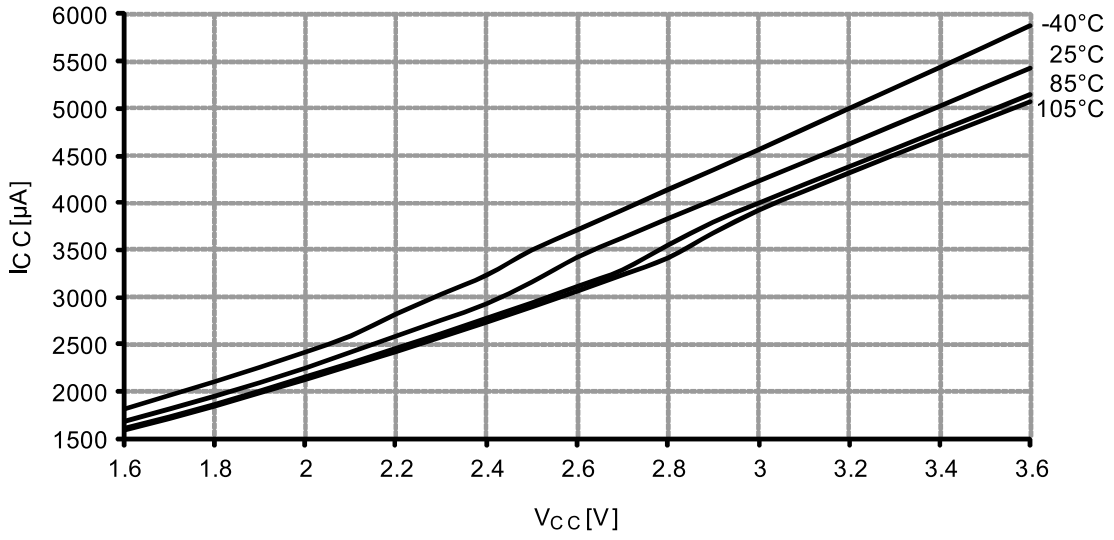
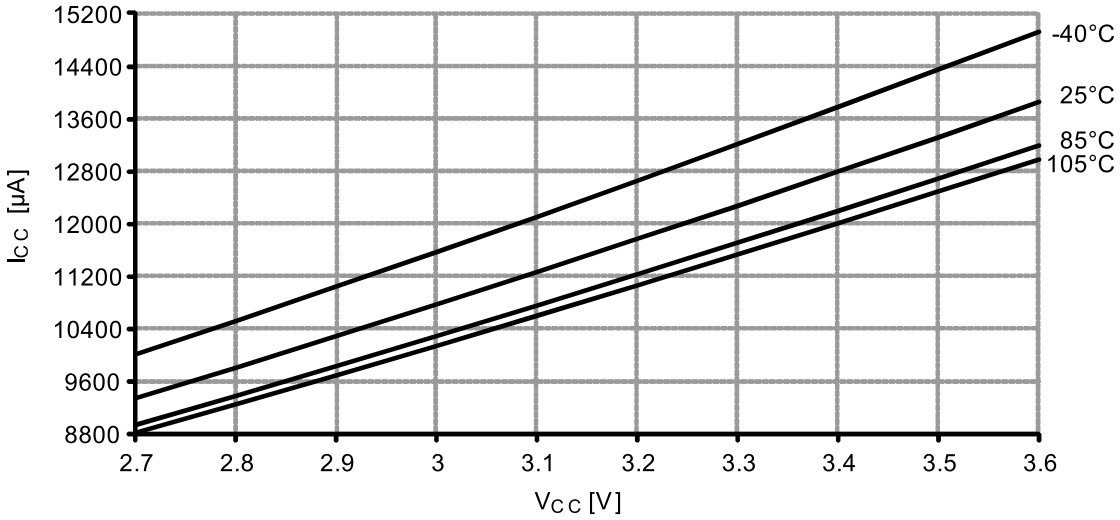


Figure 37-173. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



37.3.1.2 Idle mode supply current

Figure 37-174. Idle mode supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C.

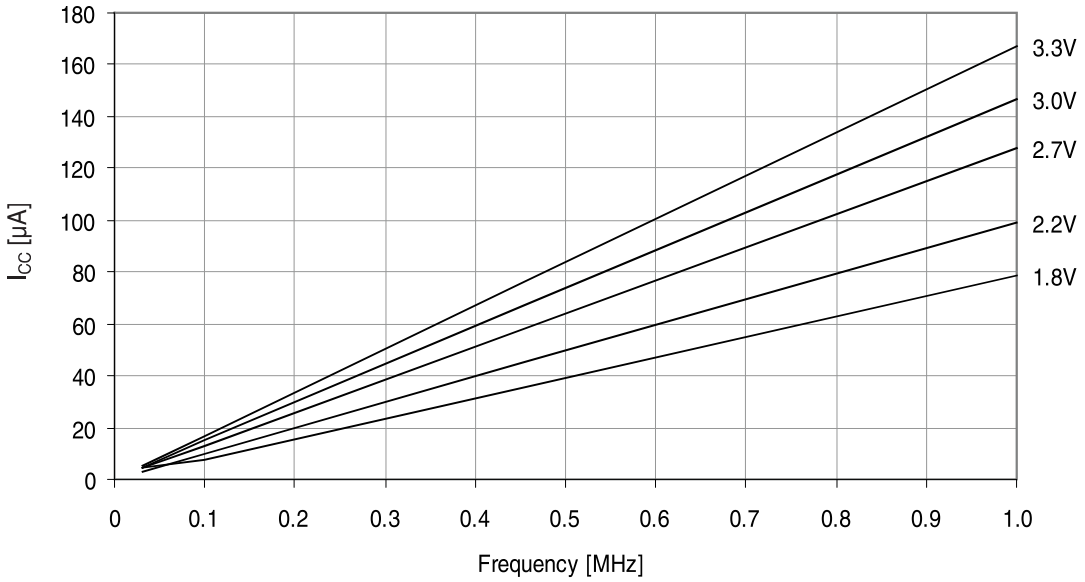


Figure 37-175. Idle mode supply current vs. frequency.

f_{SYS} = 1 - 32MHz external clock, T = 25°C.

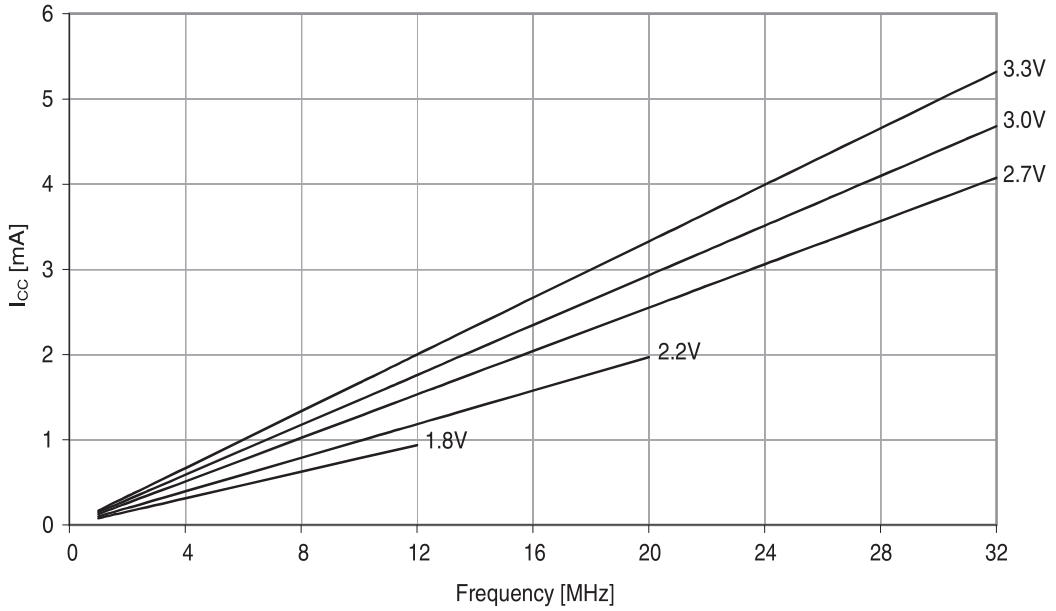


Figure 37-176. Idle mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

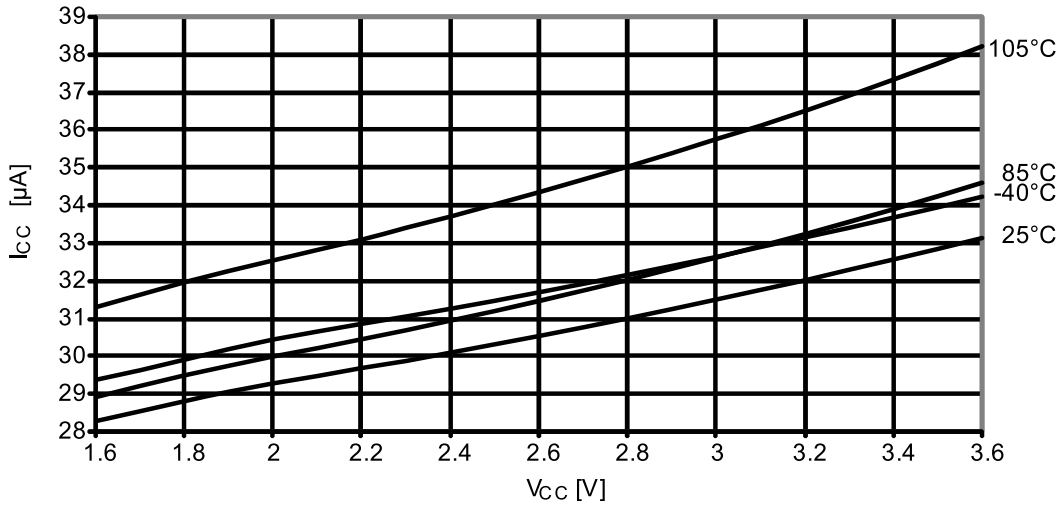


Figure 37-177. Idle mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

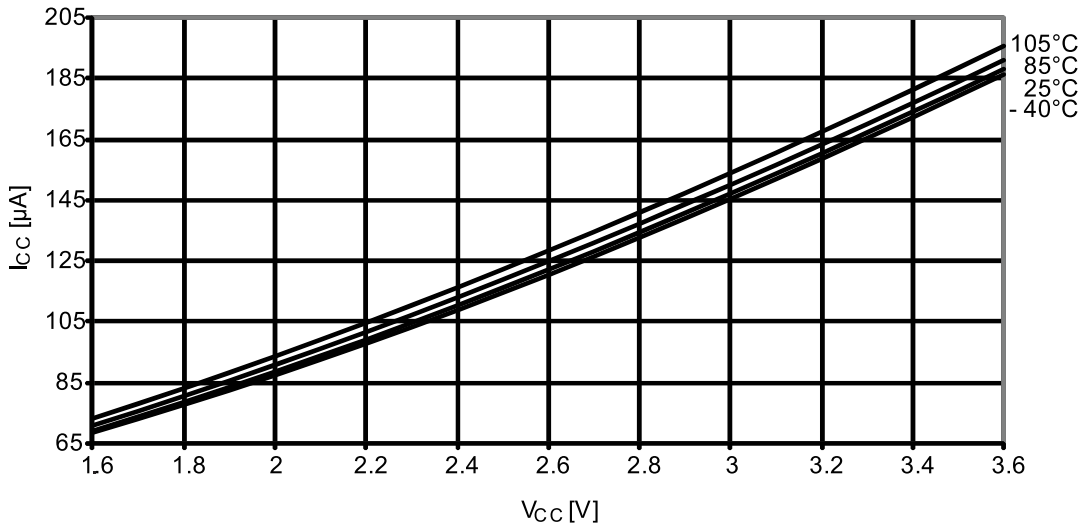


Figure 37-178. Idle mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

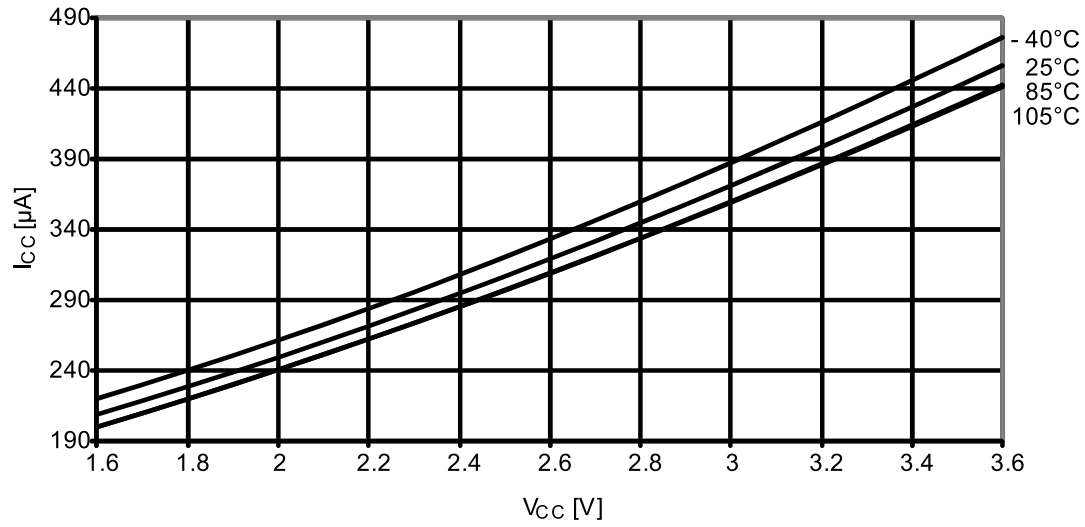


Figure 37-179. Idle mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

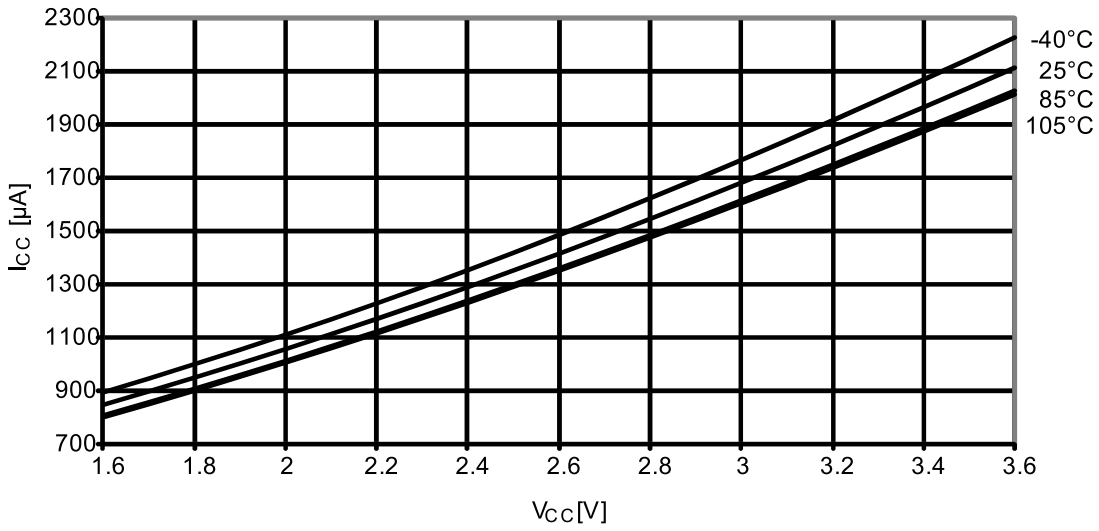
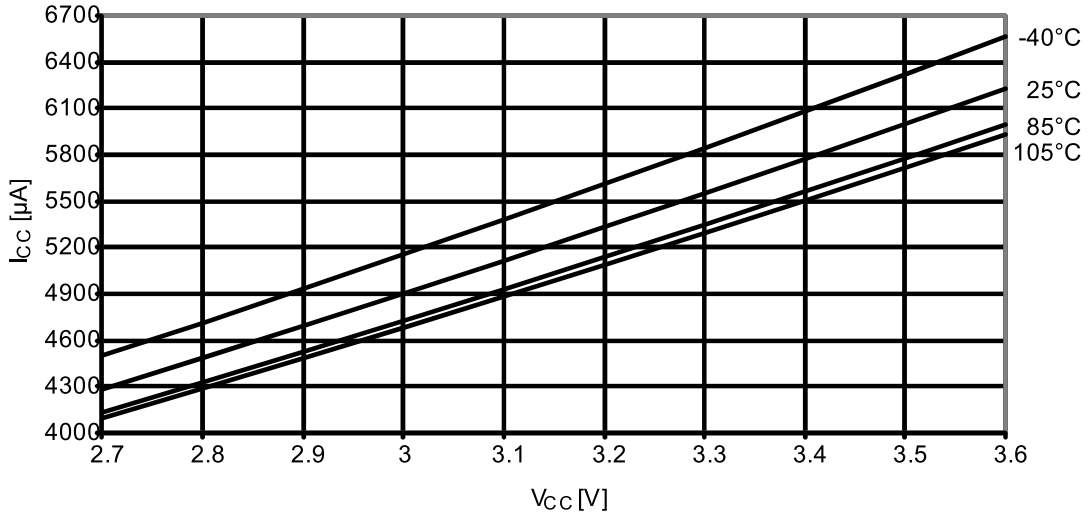


Figure 37-180. Idle mode current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



37.3.1.3 Power-down mode supply current

Figure 37-181. Power-down mode supply current vs. V_{CC}.
All functions disabled.

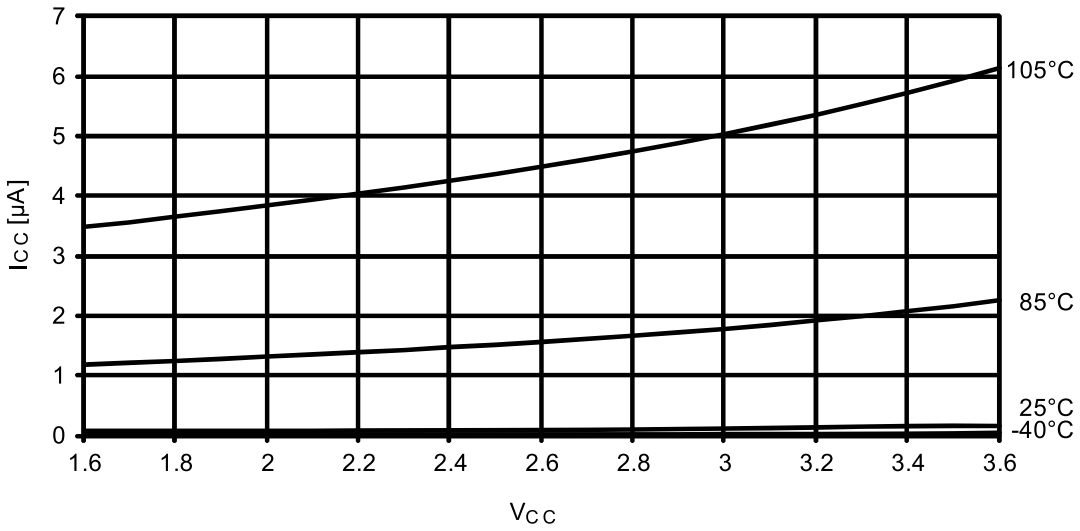
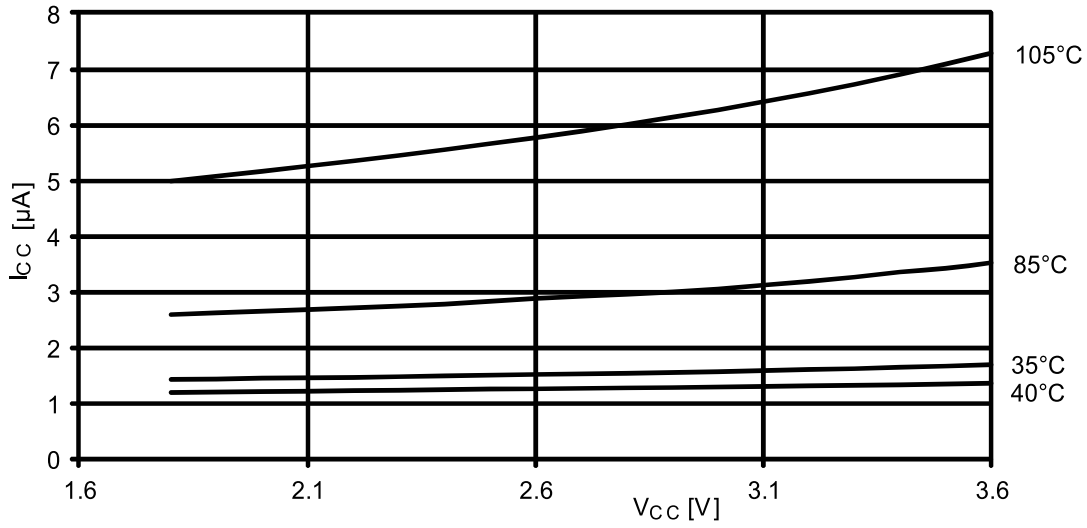


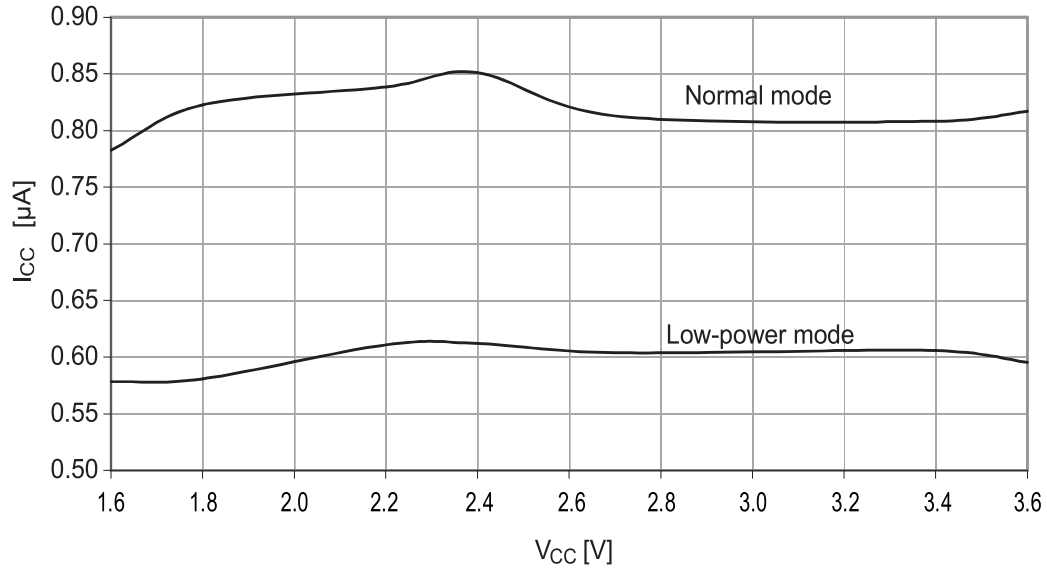
Figure 37-182. Power-down mode supply current vs. V_{CC}.
Watchdog and sampled BOD enabled.



37.3.1.4 Power-save mode supply current

Figure 37-183. Power-save mode supply current vs. V_{CC}.

Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC.



37.3.1.5 Standby mode supply current

Figure 37-184. Standby supply current vs. V_{CC}.

Standby, f_{SYS} = 1MHz.

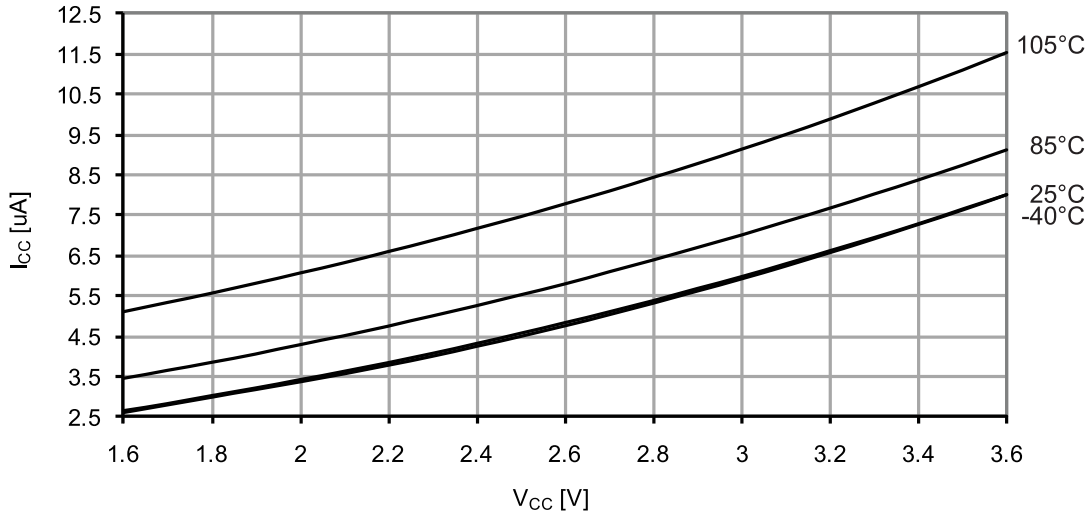
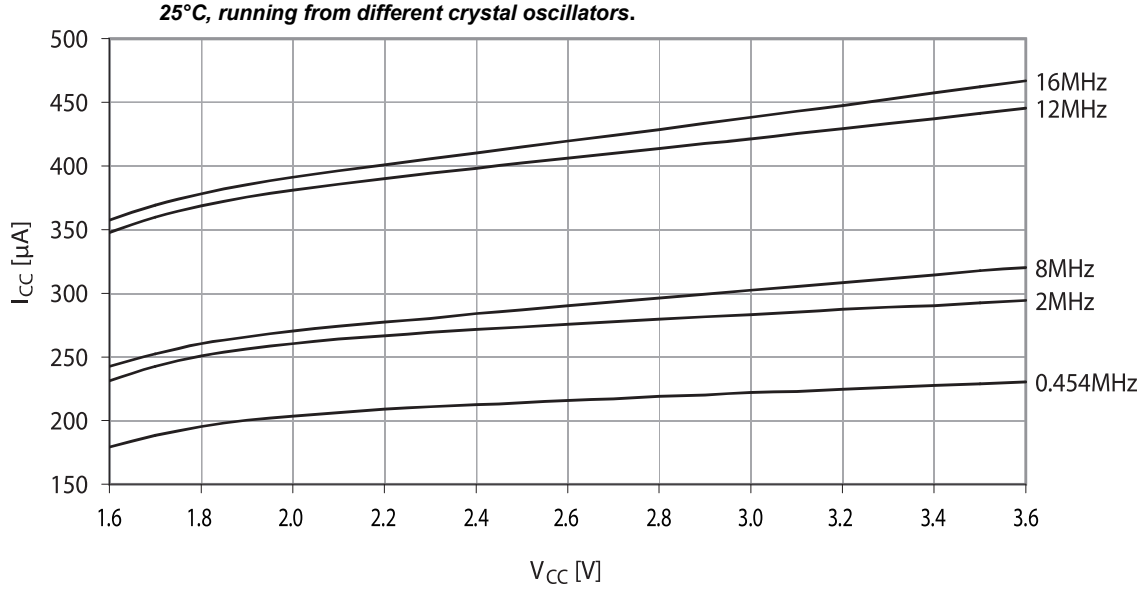


Figure 37-185. Standby supply current vs. V_{CC}.

25°C, running from different crystal oscillators.



37.3.2 I/O Pin Characteristics

37.3.2.1 Pull-up

Figure 37-186. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 1.8V.

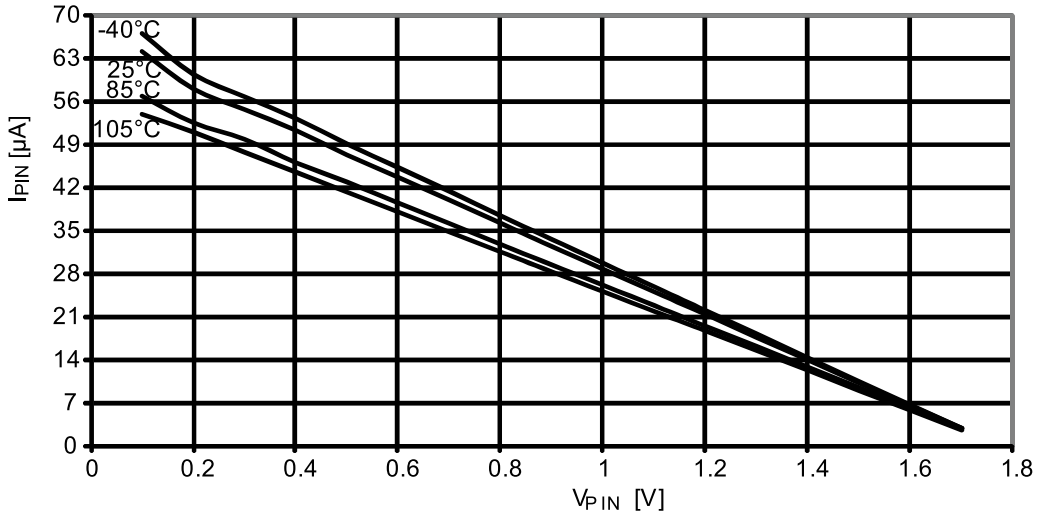


Figure 37-187. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.0V.

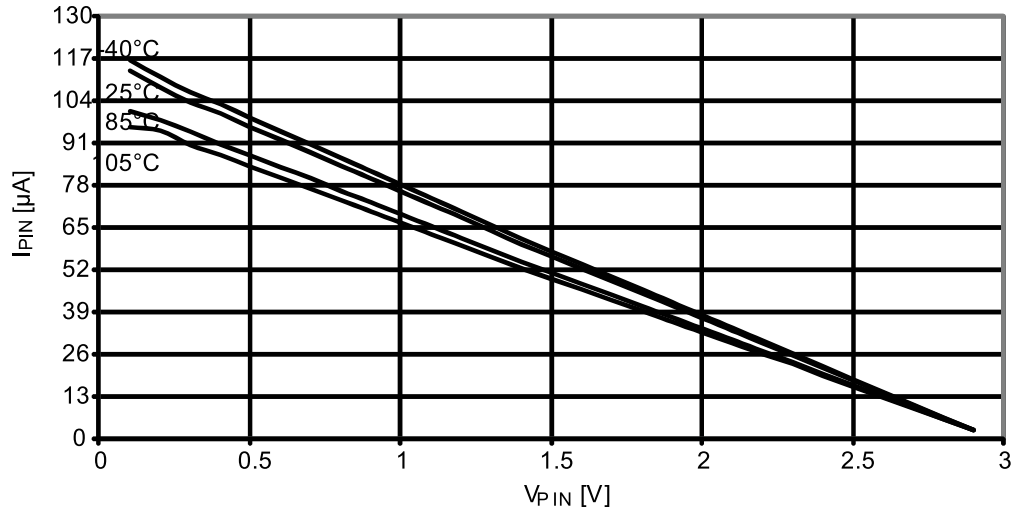
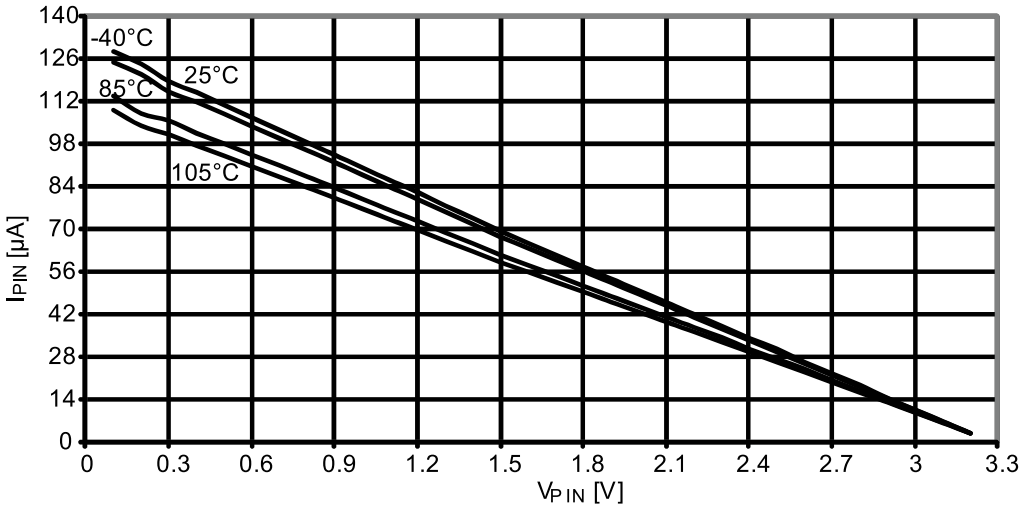


Figure 37-188. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.3V.



37.3.2.2 Output Voltage vs. Sink/Source Current

Figure 37-189. I/O pin output voltage vs. source current.
V_{CC} = 1.8V.

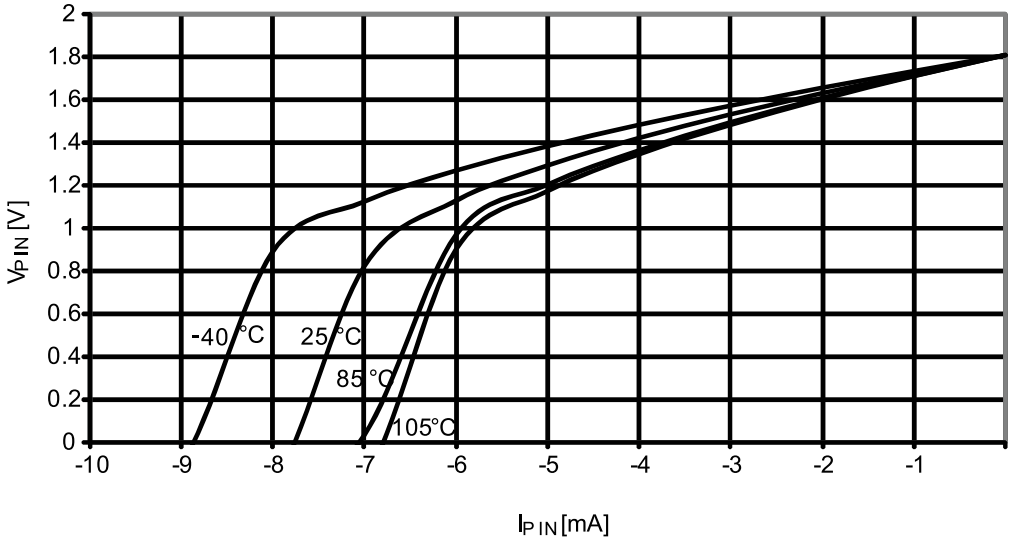


Figure 37-190. I/O pin output voltage vs. source current.
V_{CC} = 3.0V.

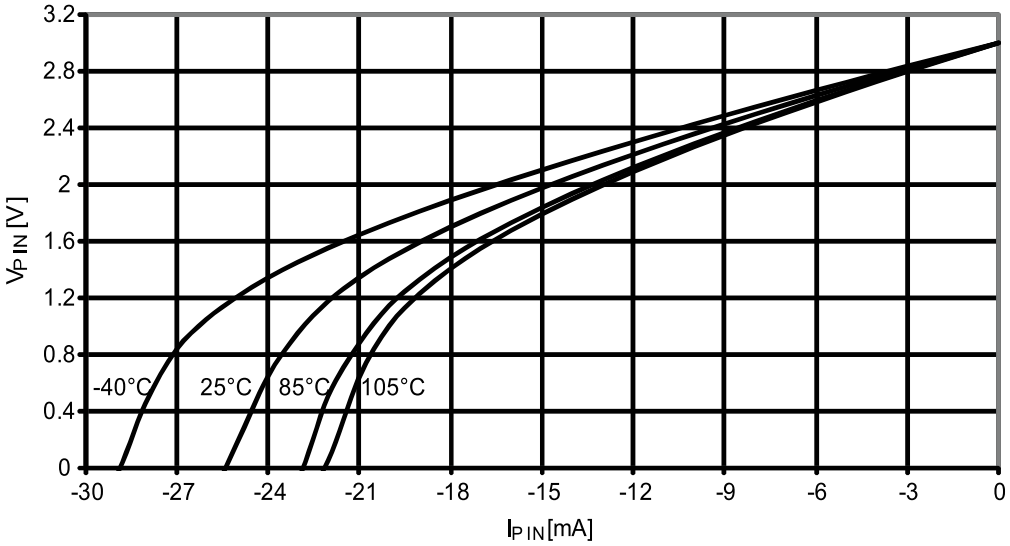


Figure 37-191. I/O pin output voltage vs. source current.

V_{CC} = 3.3V.

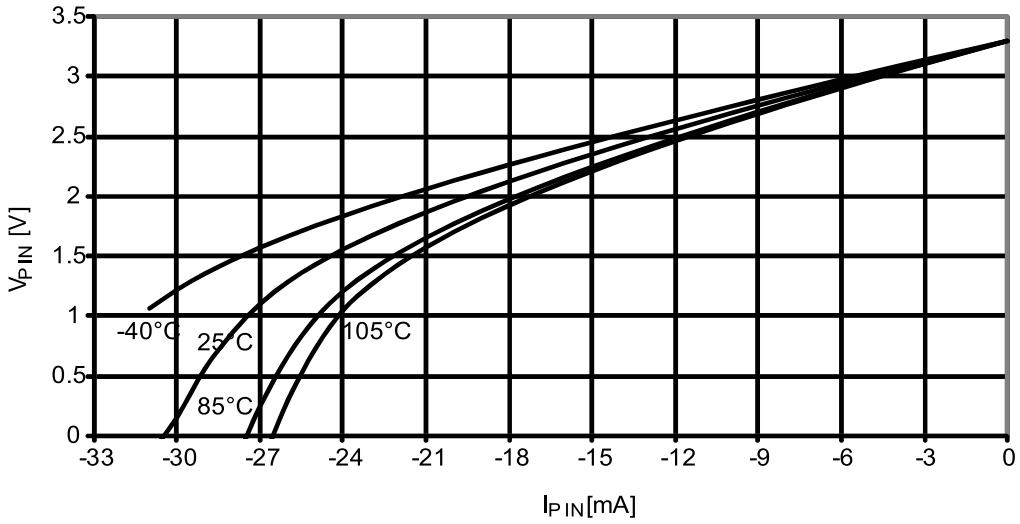


Figure 37-192. I/O pin output voltage vs. source current.

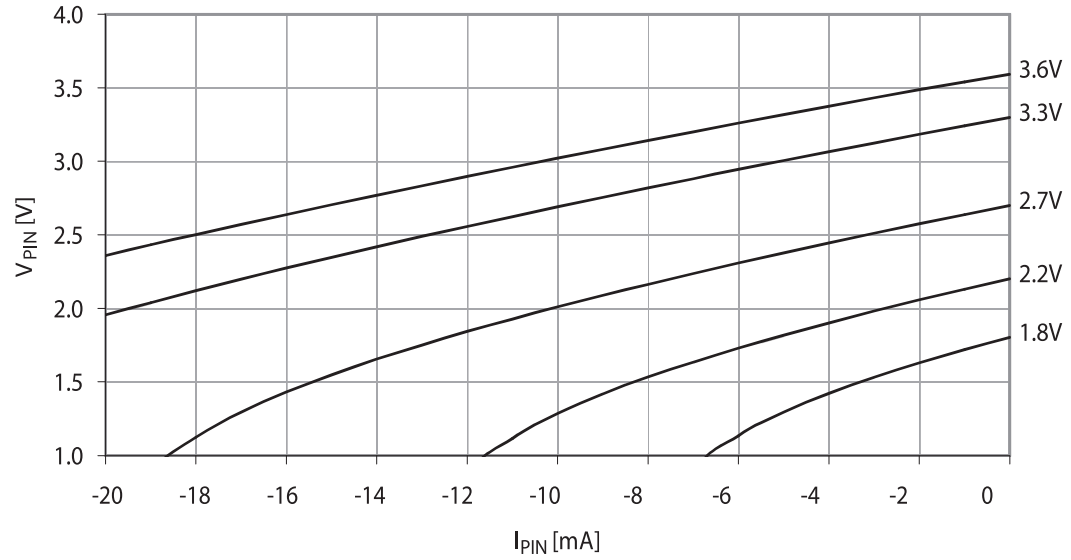


Figure 37-193. I/O pin output voltage vs. sink current.

V_{CC} = 1.8V.

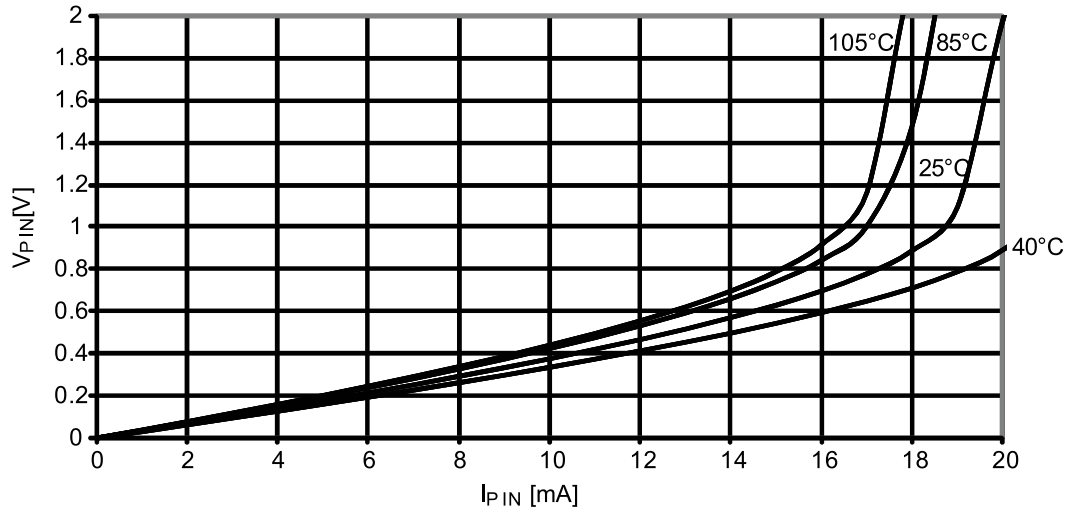


Figure 37-194. I/O pin output voltage vs. sink current.

V_{CC} = 3.0V.

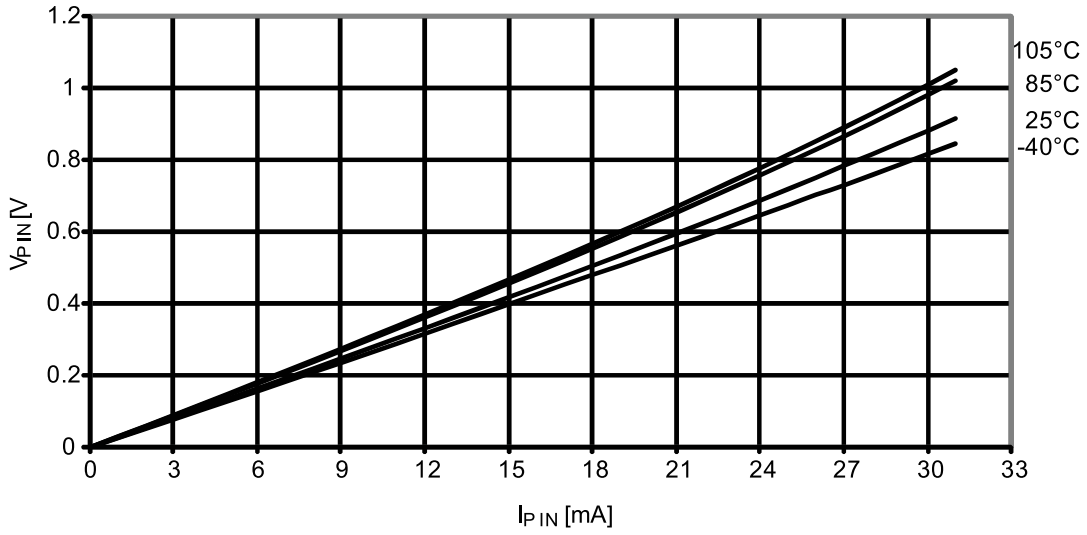


Figure 37-195. I/O pin output voltage vs. sink current.

V_{CC} = 3.3V.

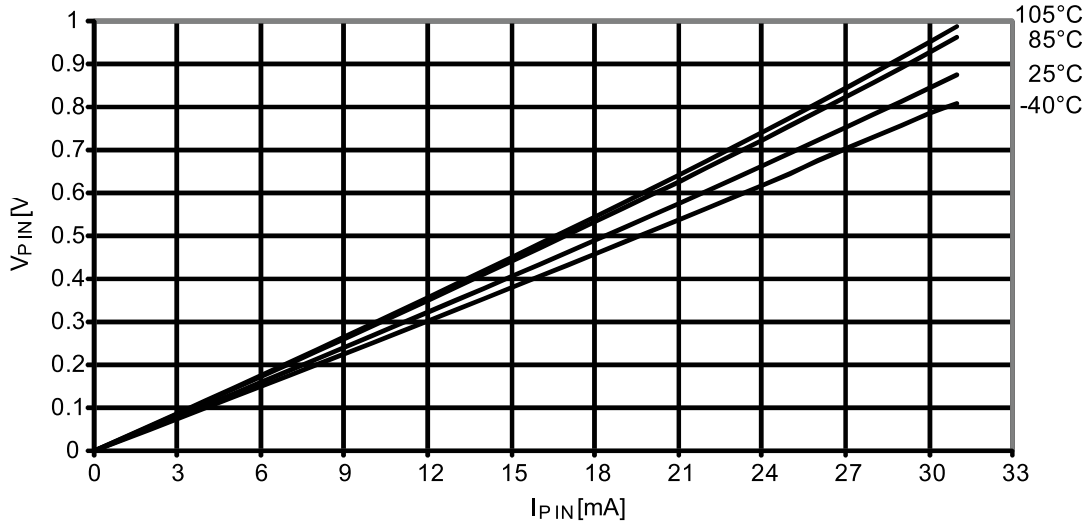
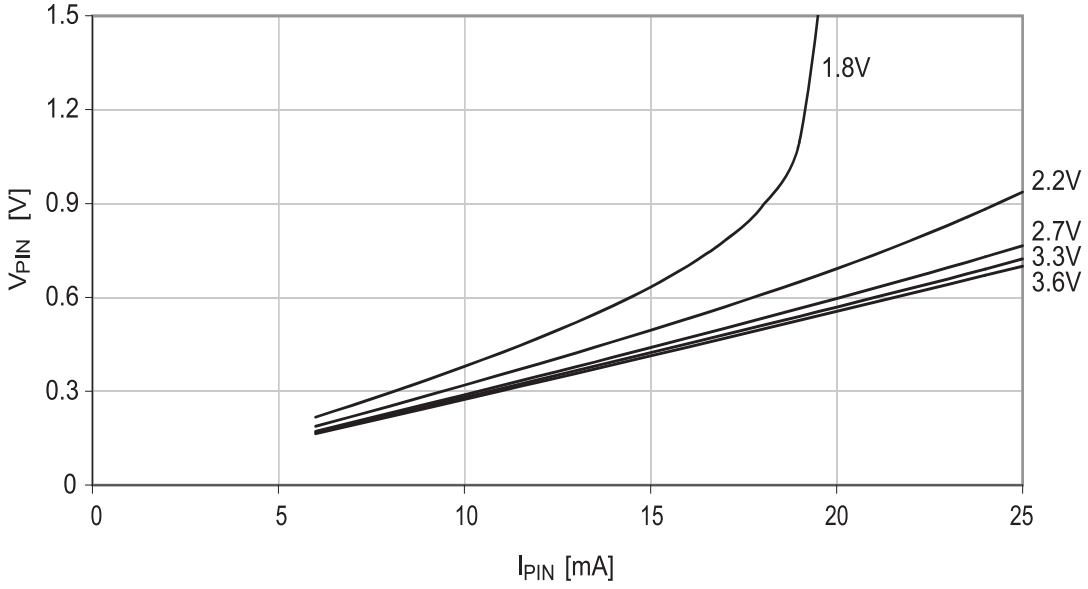


Figure 37-196. I/O pin output voltage vs. sink current.



37.3.2.3 Thresholds and Hysteresis

Figure 37-197. I/O pin input threshold voltage vs. V_{CC}.
T = 25°C.

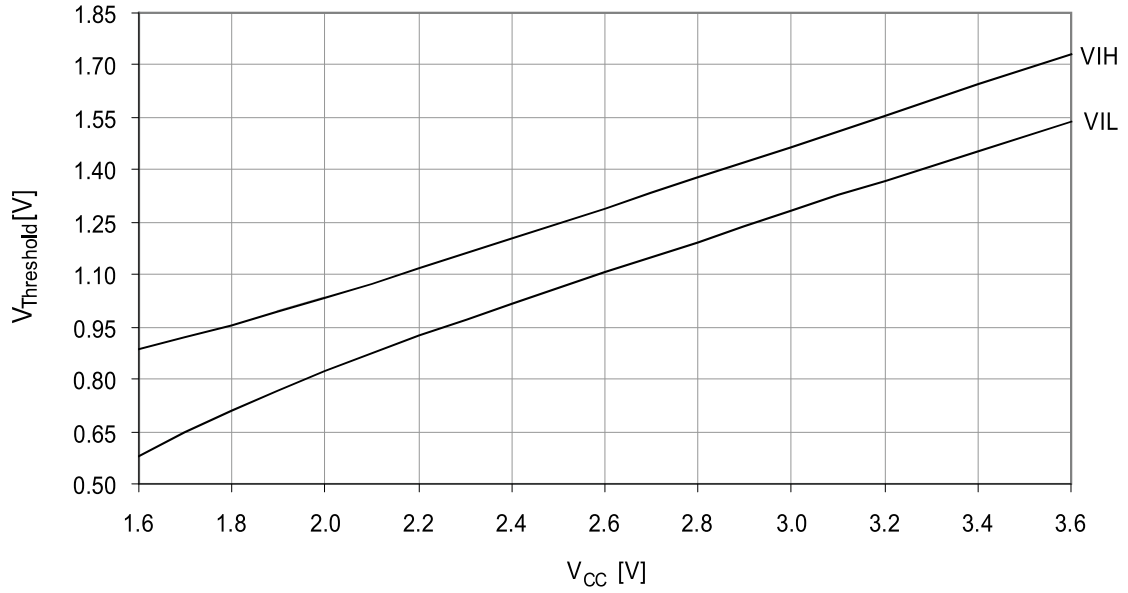


Figure 37-198. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} I/O pin read as "1".

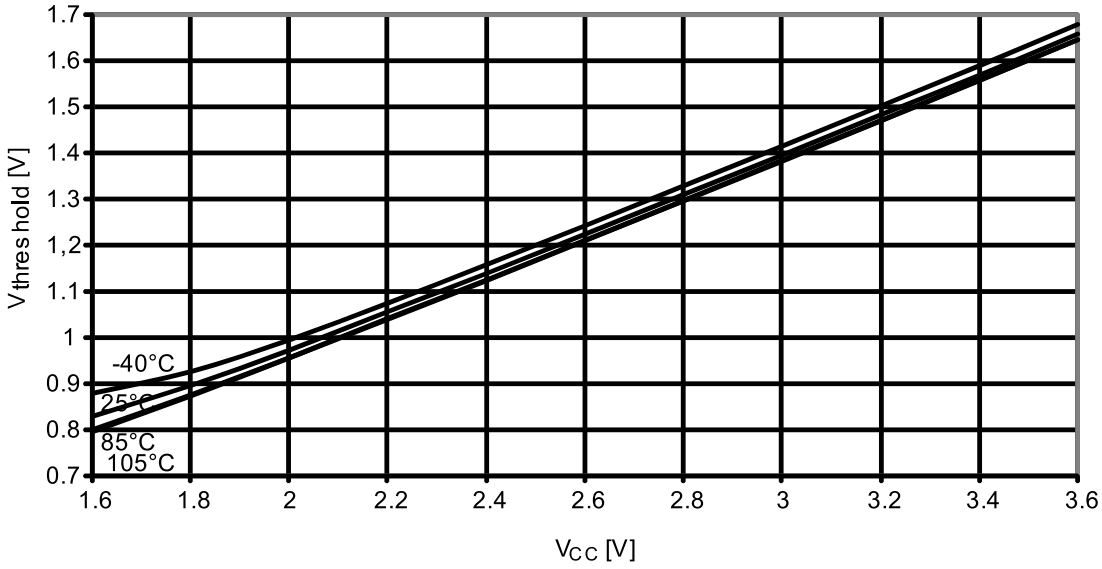


Figure 37-199. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

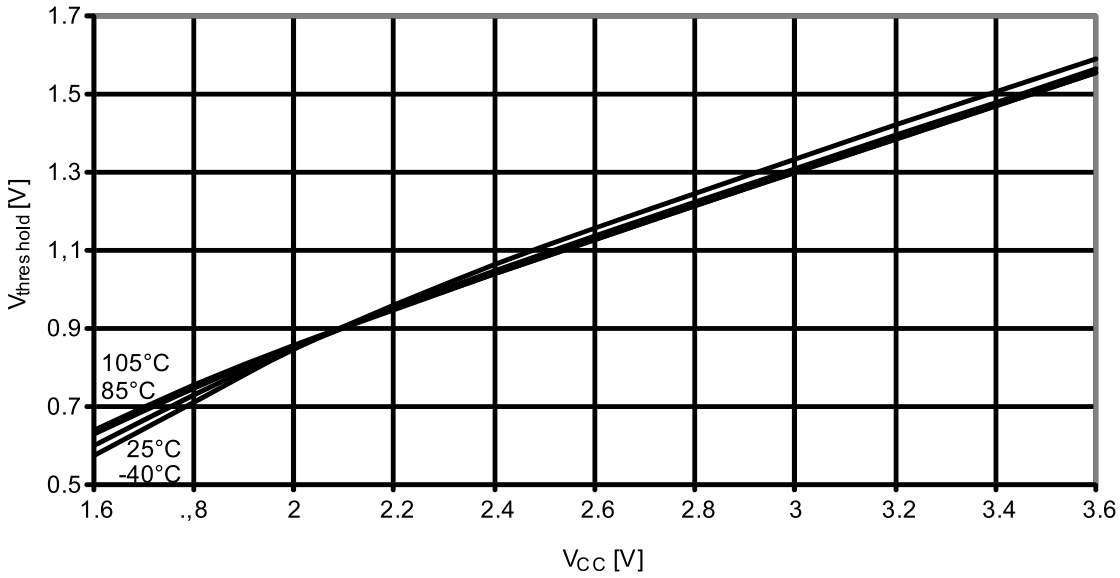
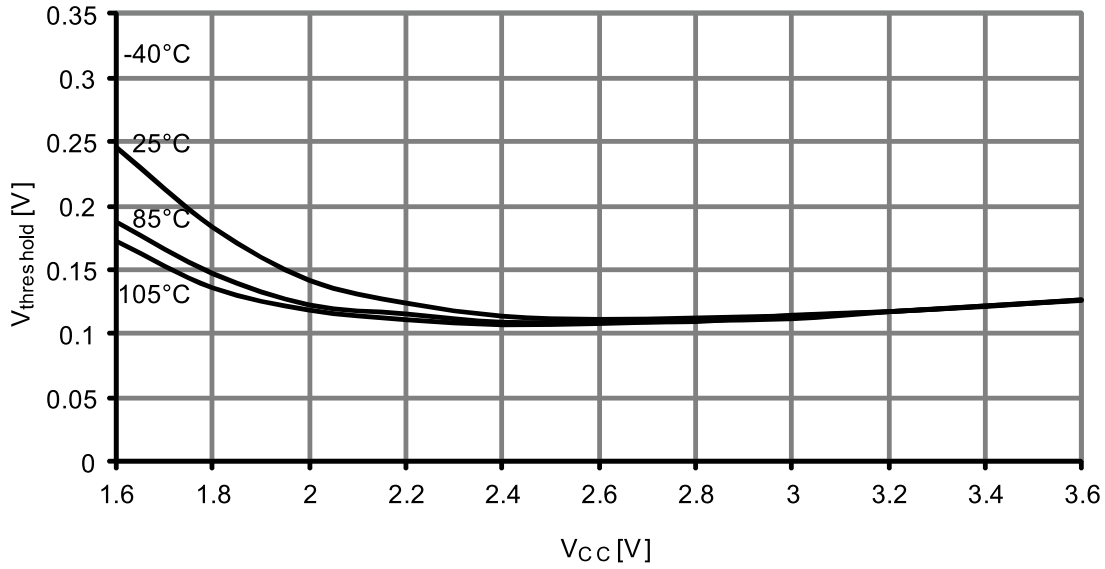


Figure 37-200. I/O pin input hysteresis vs. V_{CC} .



37.3.3 ADC Characteristics

Figure 37-201. INL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

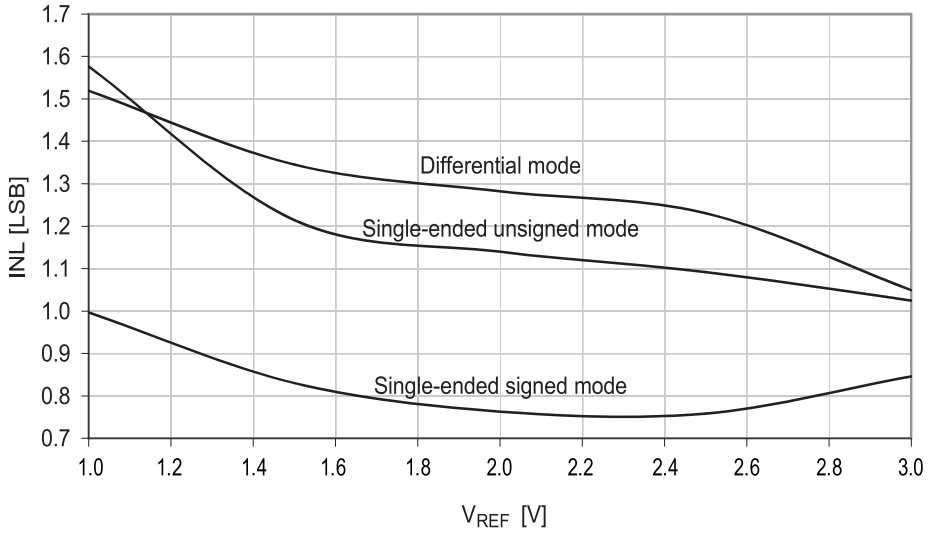


Figure 37-202. INL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

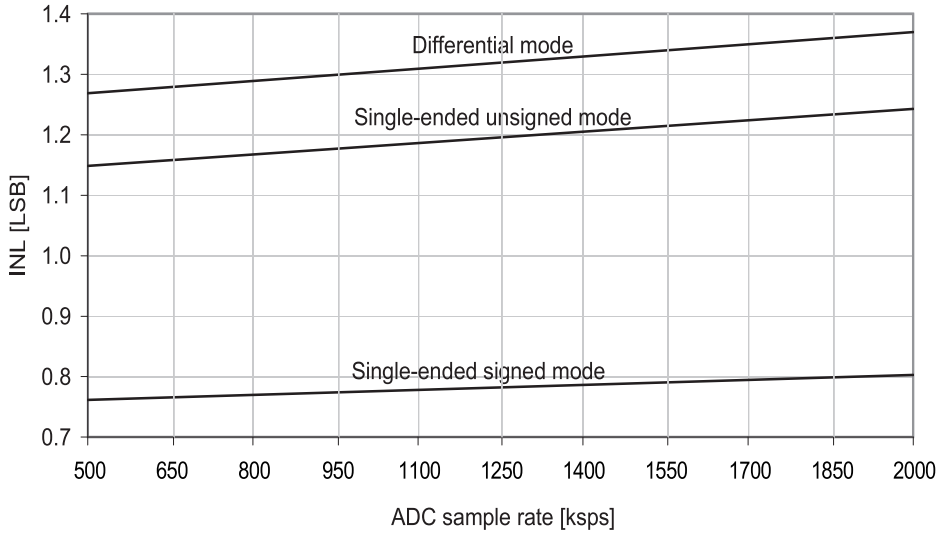


Figure 37-203. INL error vs. input code.

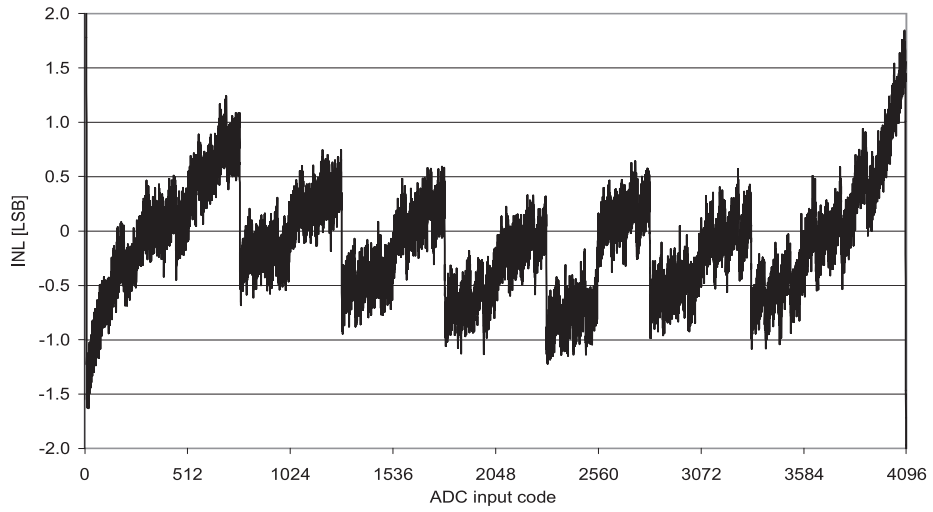


Figure 37-204. DNL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

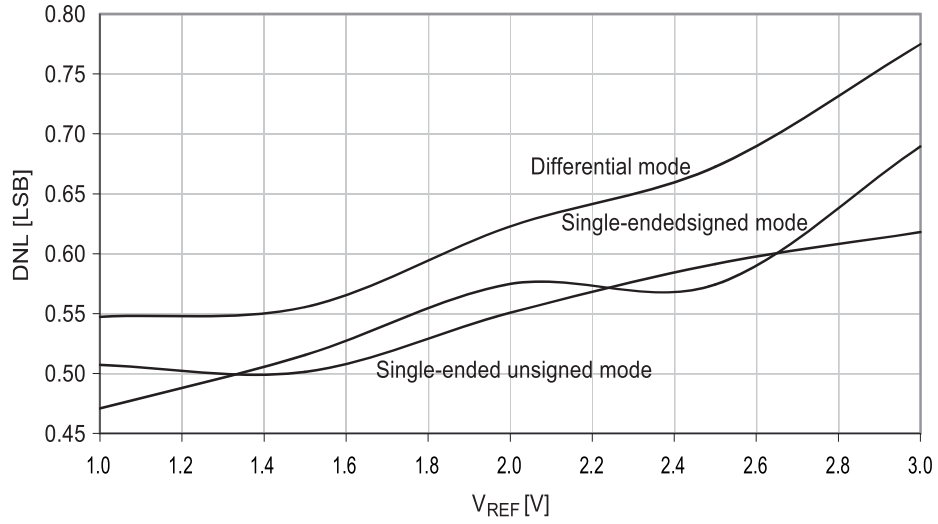


Figure 37-205. DNL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

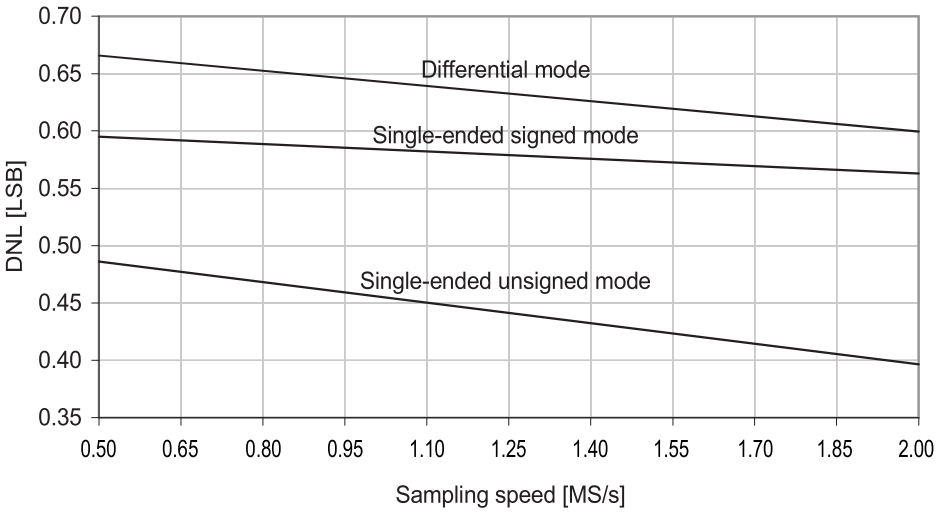


Figure 37-206. DNL error vs. input code.

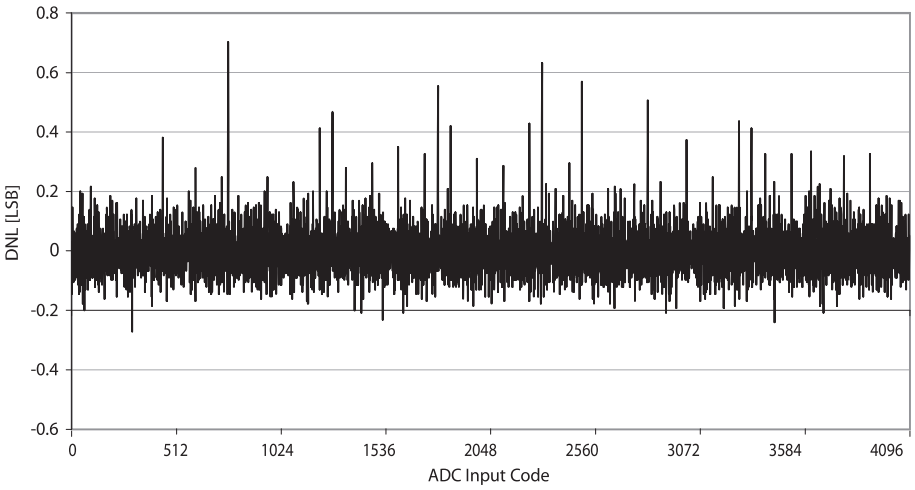


Figure 37-207. Gain error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

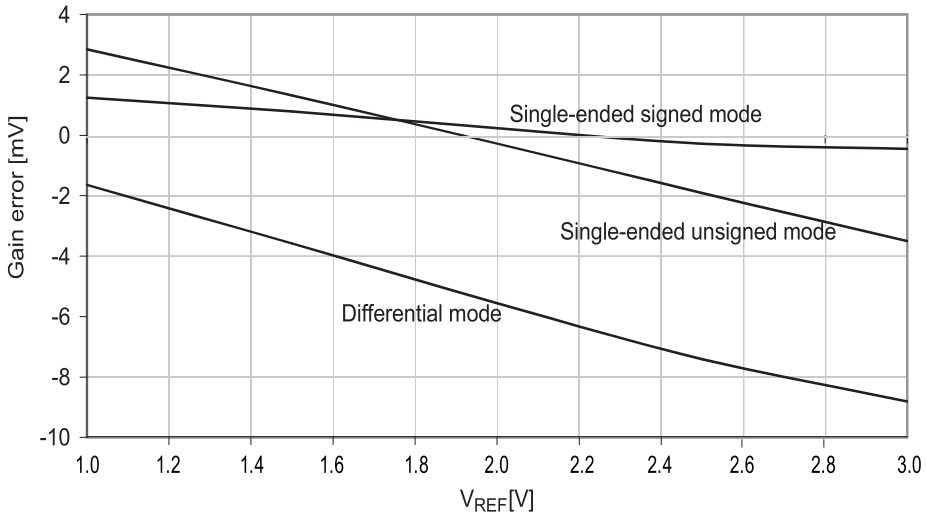


Figure 37-208. Gain error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

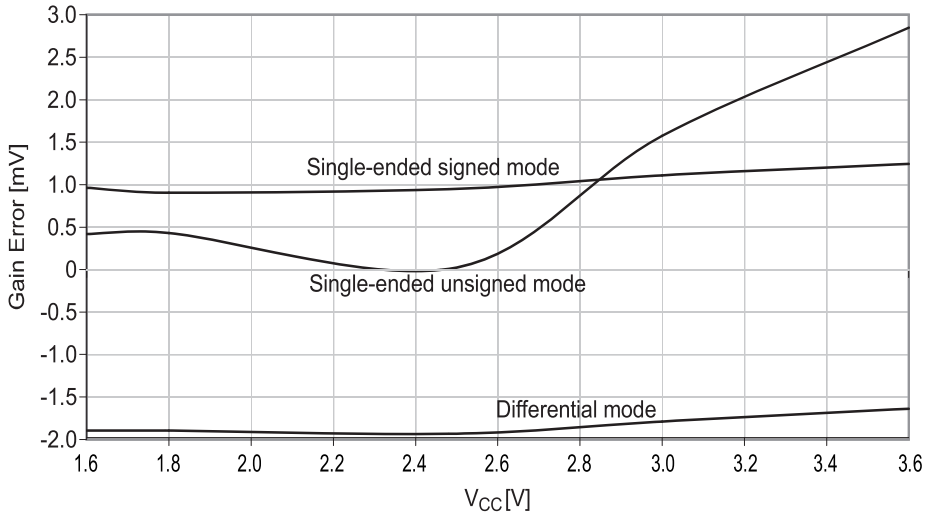


Figure 37-209. Offset error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

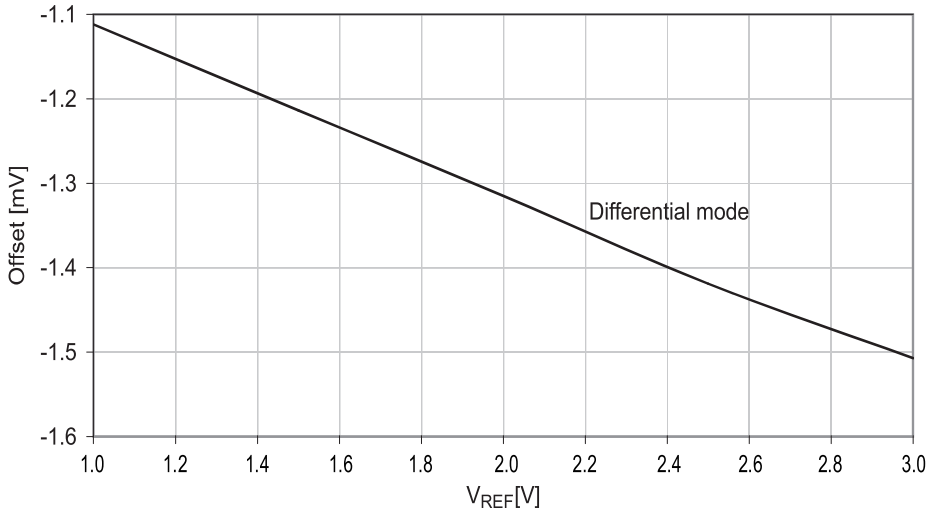


Figure 37-210. Gain error vs. temperature.

V_{CC} = 2.7V, V_{REF} = external 1.0V .

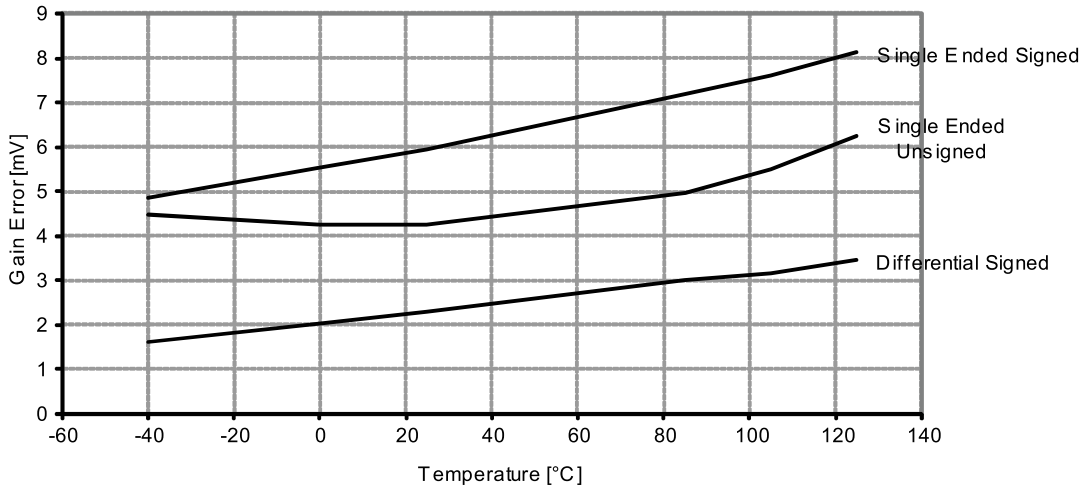


Figure 37-211. Offset error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

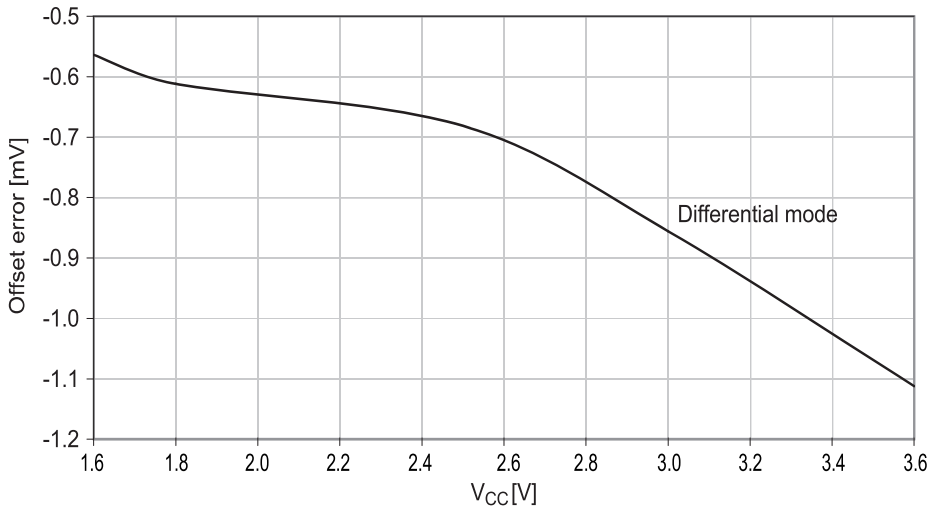


Figure 37-212. Noise vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

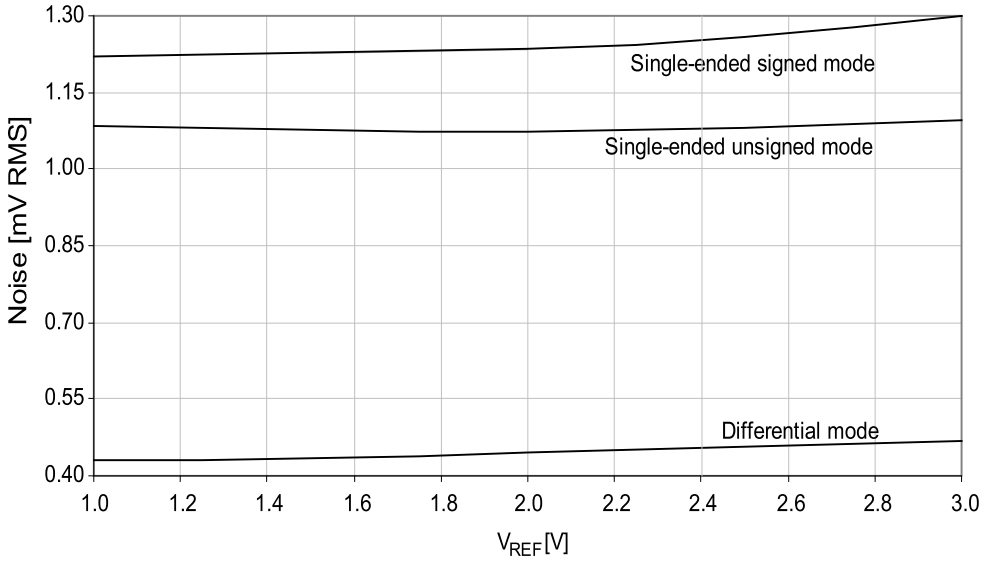
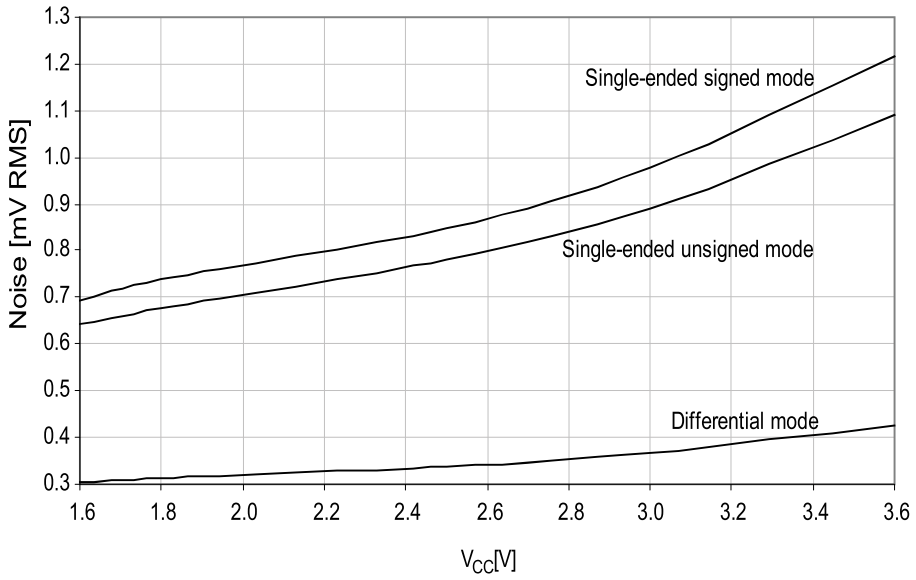


Figure 37-213. Noise vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.



37.3.4 DAC Characteristics

Figure 37-214. DAC INL error vs. V_{REF}.

V_{CC} = 3.6V.

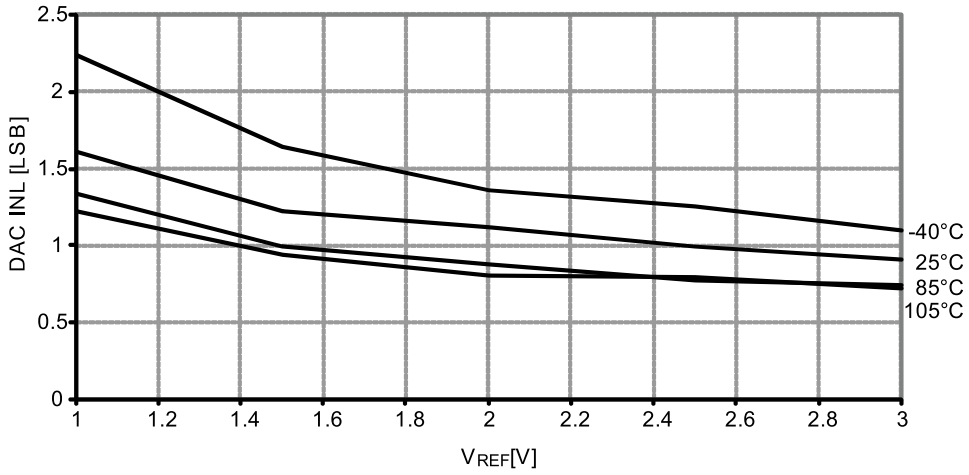


Figure 37-215. DNL error vs. V_{REF}.

$T = 25°C$, $V_{CC} = 3.6V$.

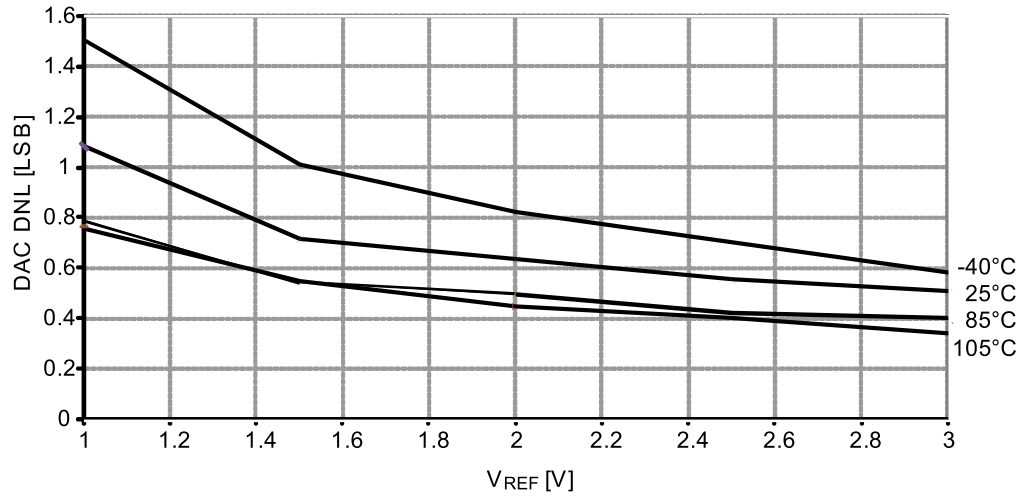
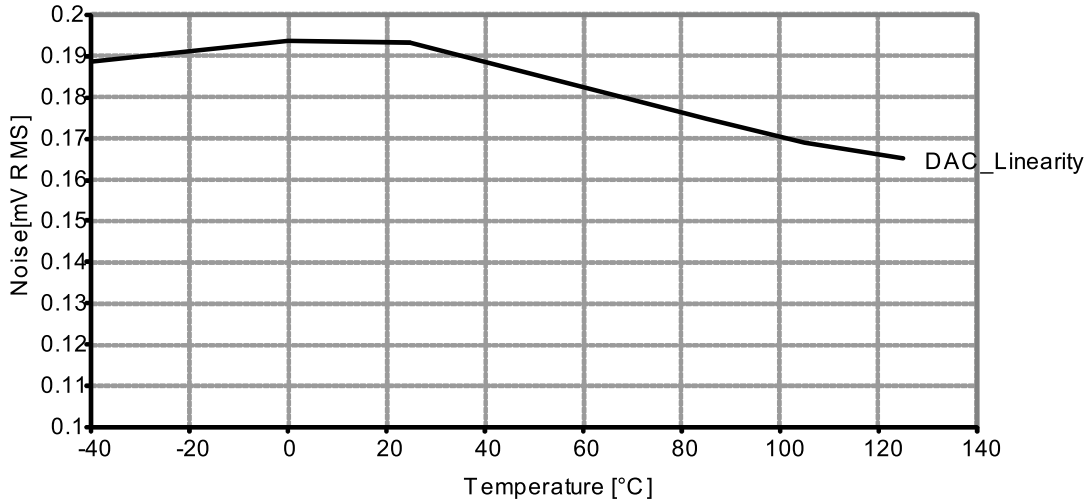


Figure 37-216. DAC noise vs. temperature.

$V_{CC} = 3.3V$, $V_{REF} = 2.0V$.



37.3.5 Analog Comparator Characteristics

Figure 37-217. Analog comparator hysteresis vs. V_{CC}.
High-speed, small hysteresis.

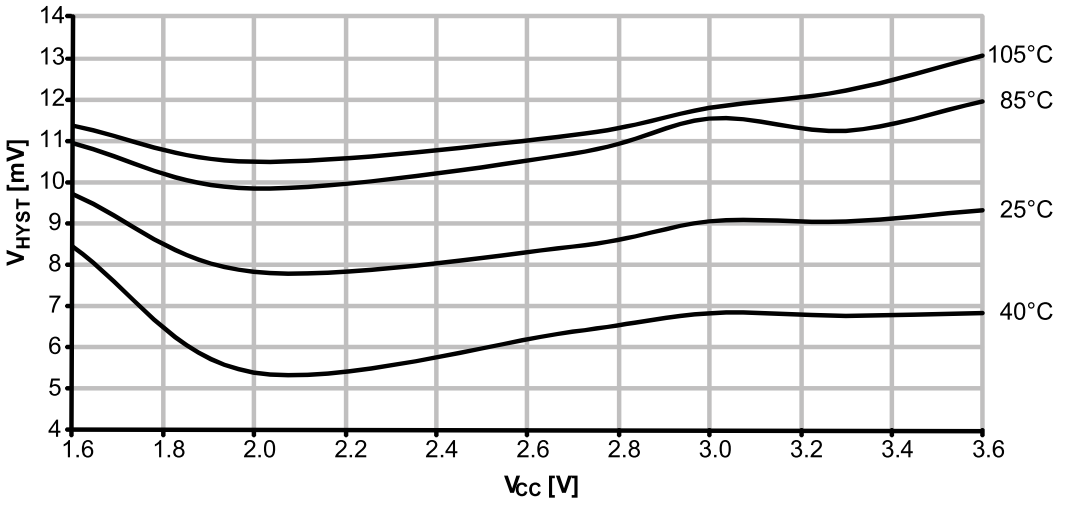


Figure 37-218. Analog comparator hysteresis vs. V_{CC}.
Low power, small hysteresis.

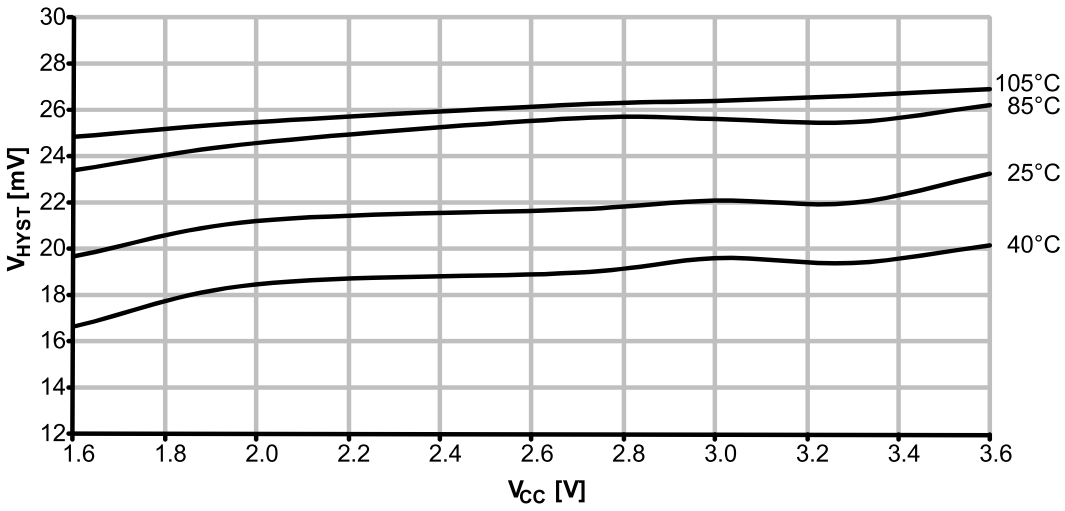


Figure 37-219. Analog comparator hysteresis vs. V_{CC}.

High-speed mode, large hysteresis.

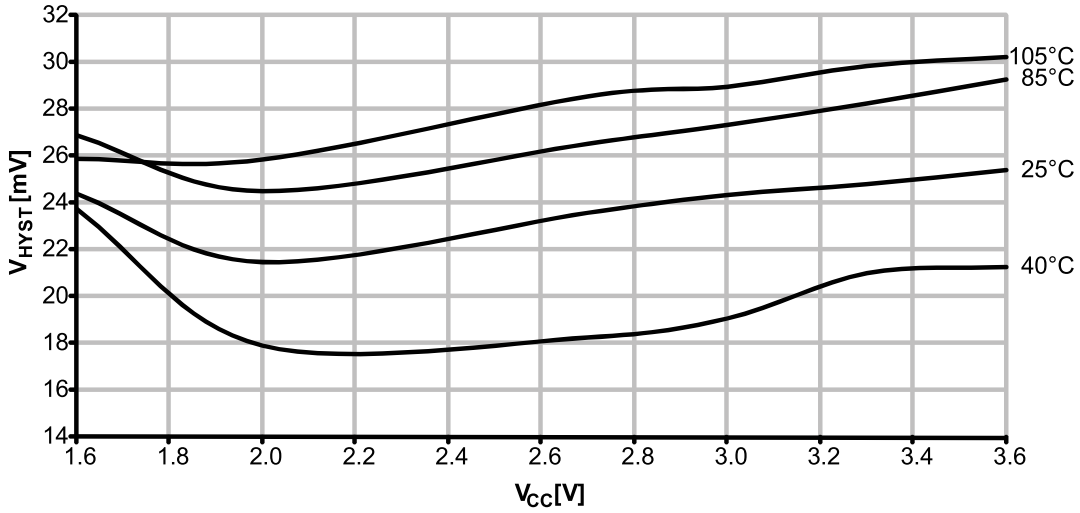


Figure 37-220. Analog comparator hysteresis vs. V_{CC}.

Low power, large hysteresis.

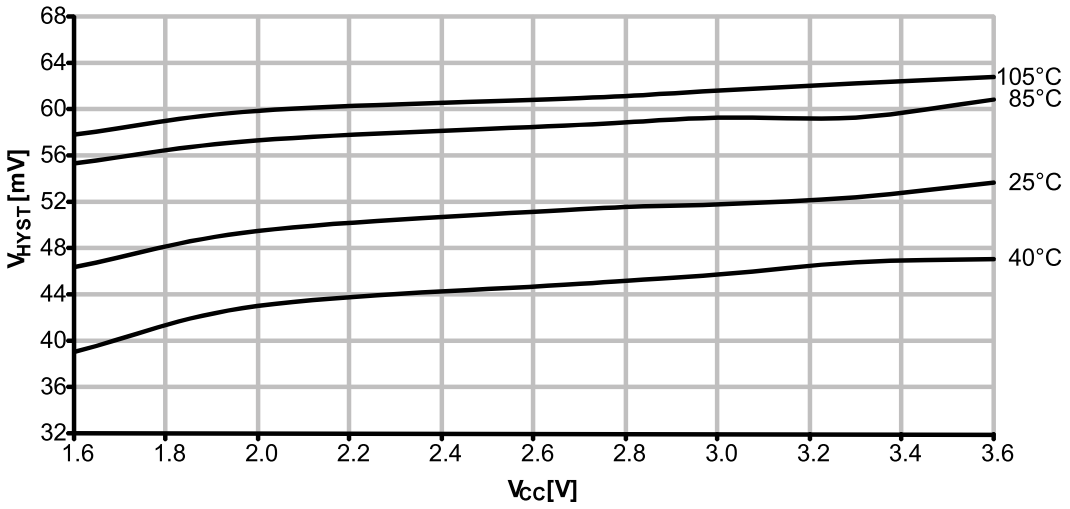


Figure 37-221. Analog comparator current source vs. calibration value.

Temperature = 25°C.

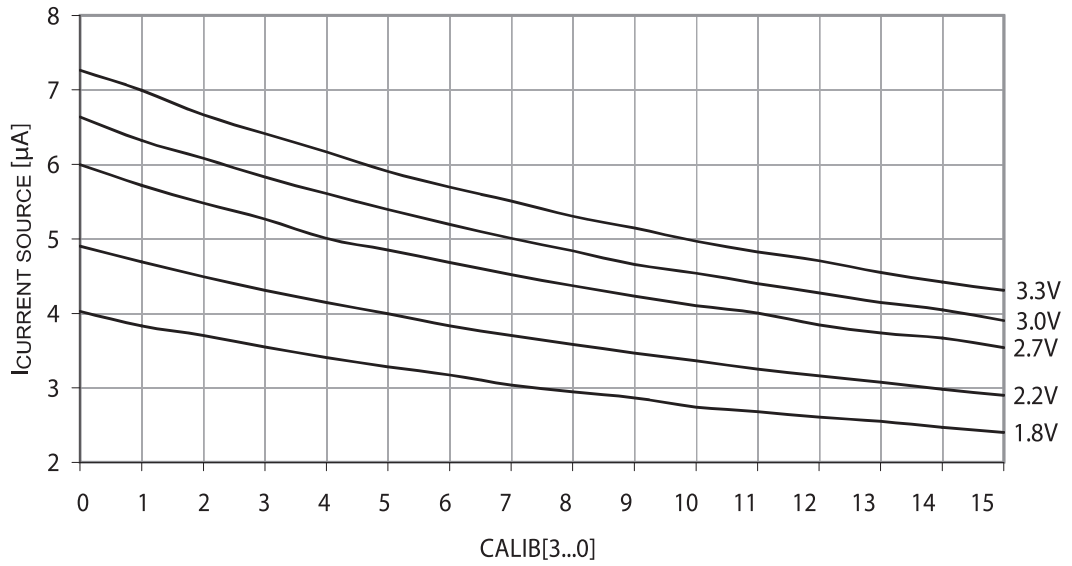


Figure 37-222. Analog comparator current source vs. calibration value.

V_{CC} = 3.0V.

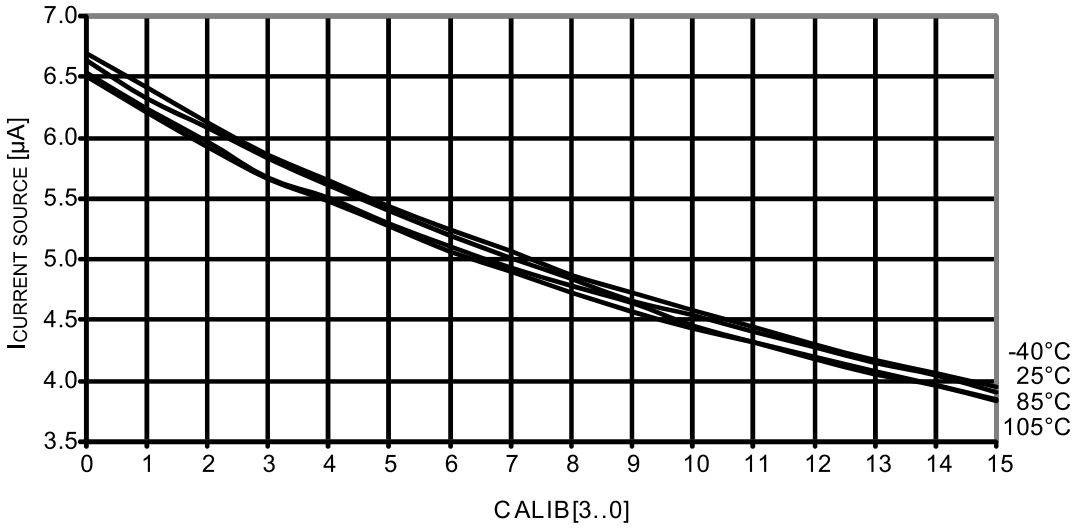
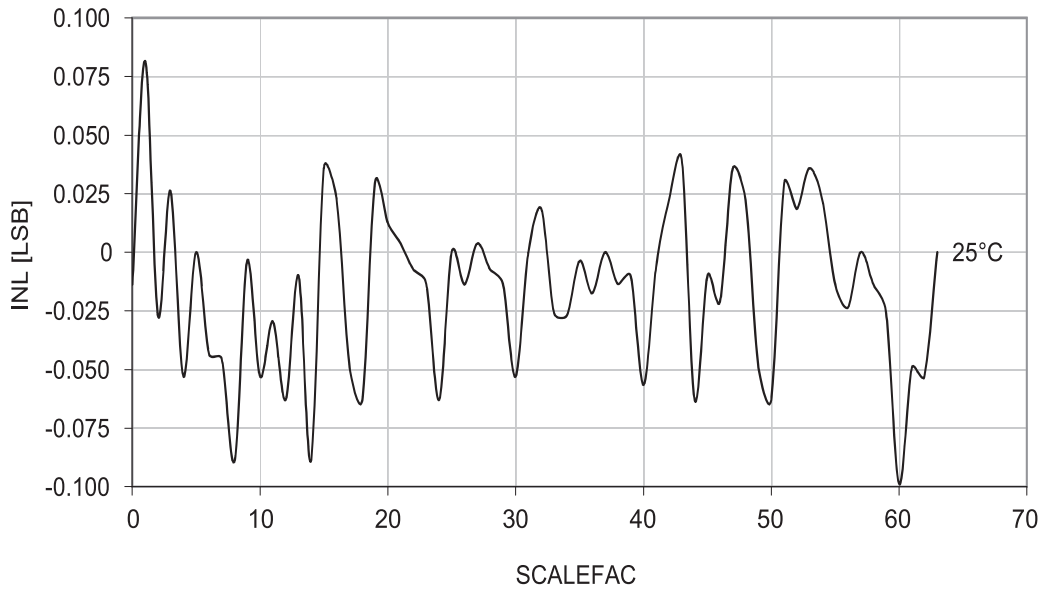


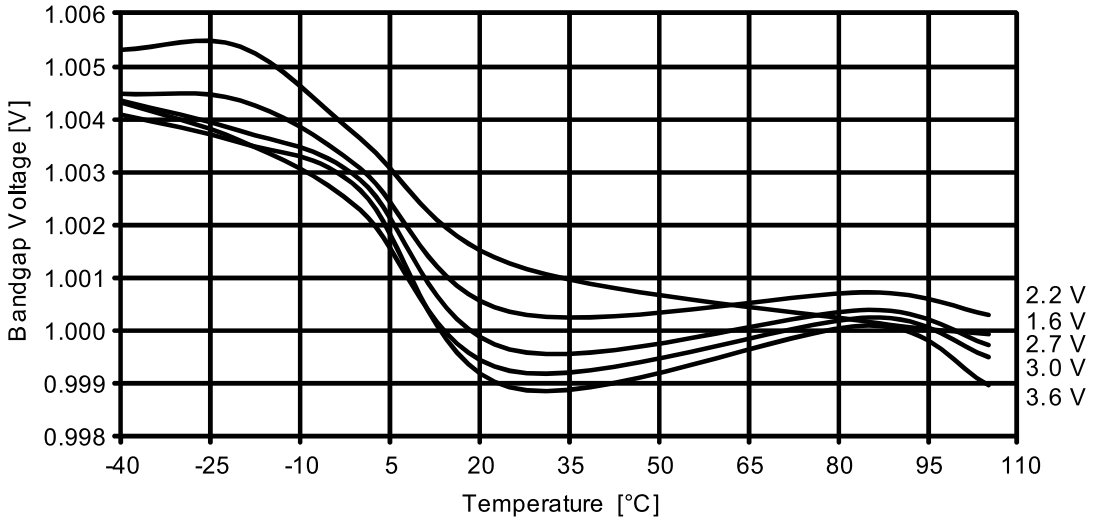
Figure 37-223. Voltage scaler INL vs. SCALEFAC.

T = 25°C, V_{CC} = 3.0V.



37.3.6 Internal 1.0V reference Characteristics

Figure 37-224. ADC/DAC Internal 1.0V reference vs. temperature.



37.3.7 BOD Characteristics

Figure 37-225. BOD thresholds vs. temperature.
BOD level = 1.6V.

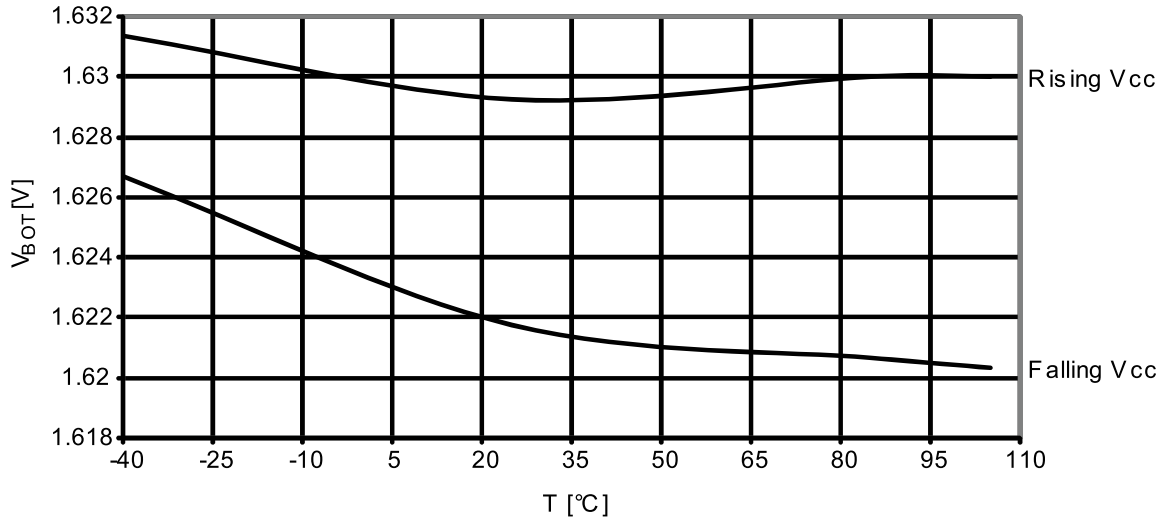
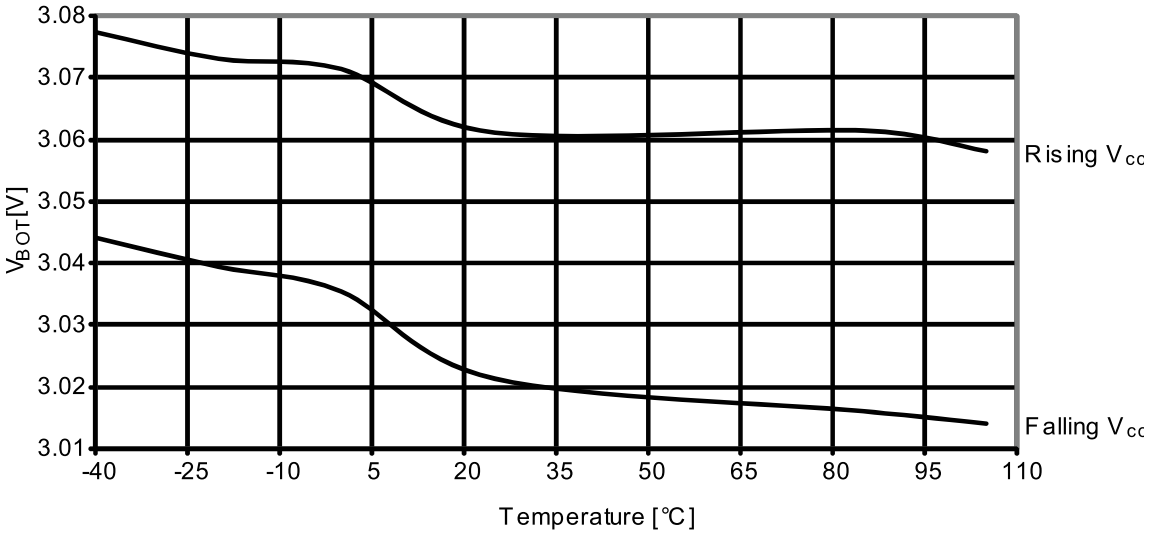


Figure 37-226. BOD thresholds vs. temperature.
BOD level = 3.0V.



37.3.8 External Reset Characteristics

Figure 37-227. Minimum Reset pin pulse width vs. V_{CC}.

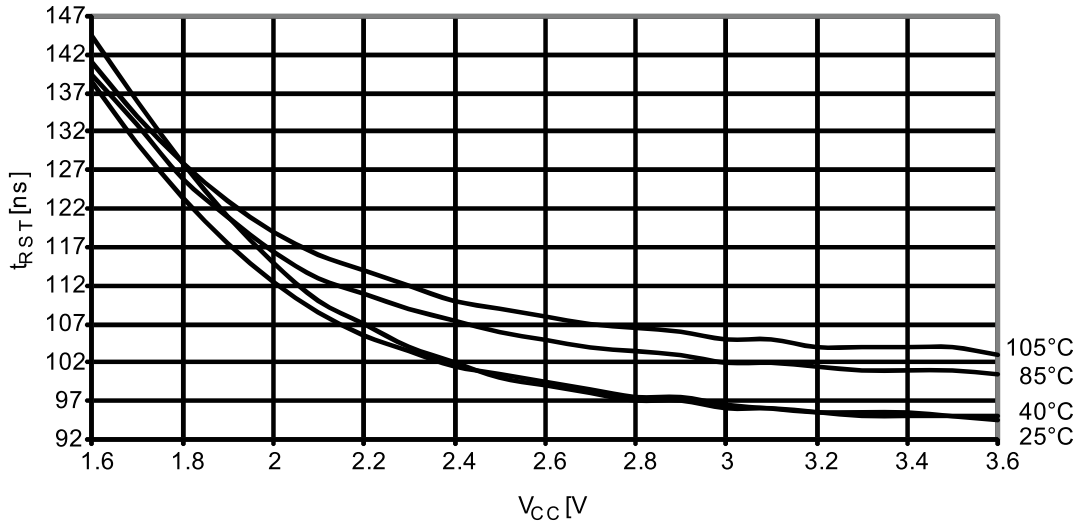


Figure 37-228. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 1.8V.

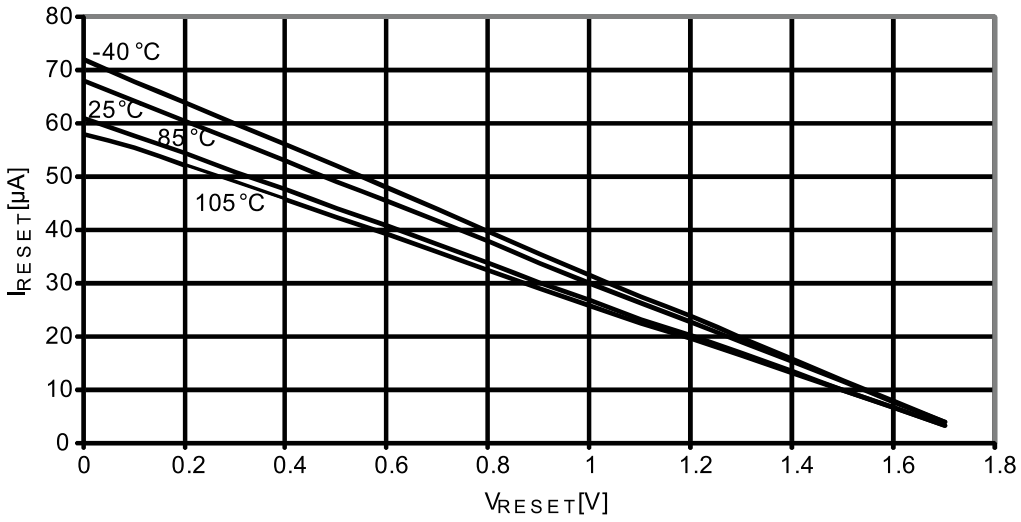


Figure 37-229. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 3.0V.

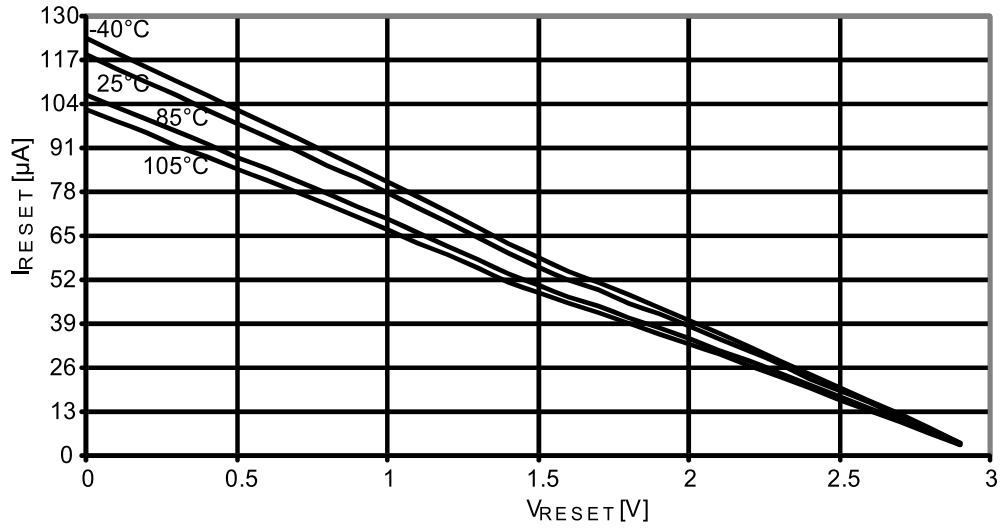


Figure 37-230. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 3.3V.

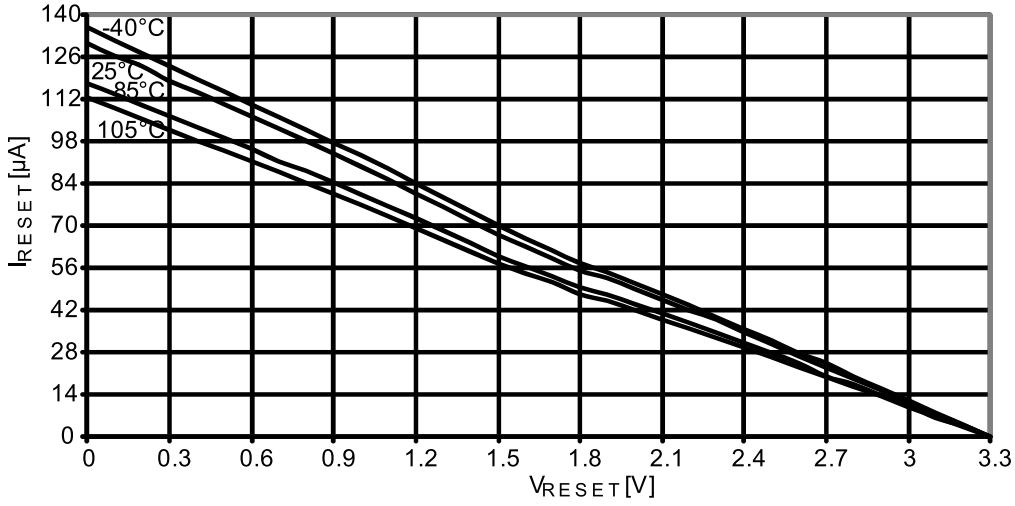


Figure 37-231. Reset pin input threshold voltage vs. V_{CC}

V_{IH} - Reset pin read as "1".

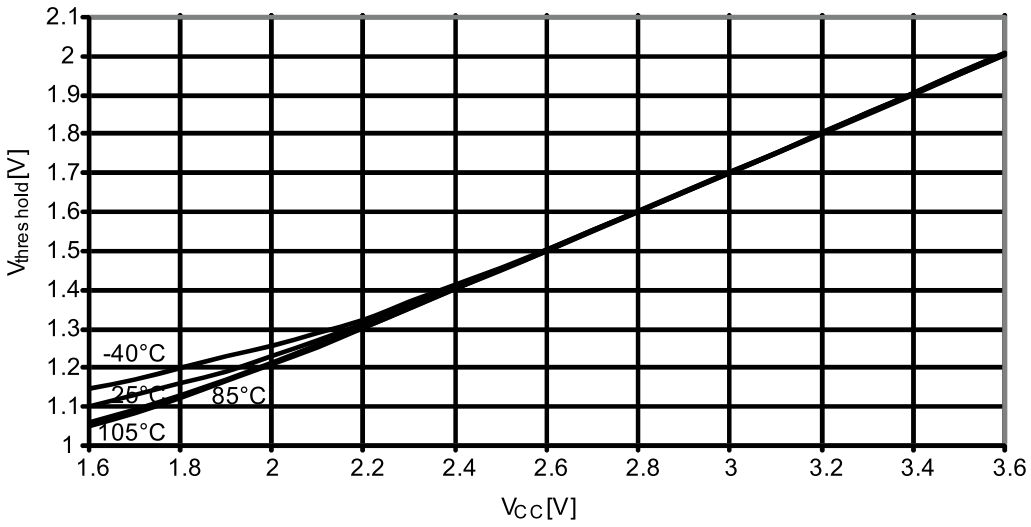
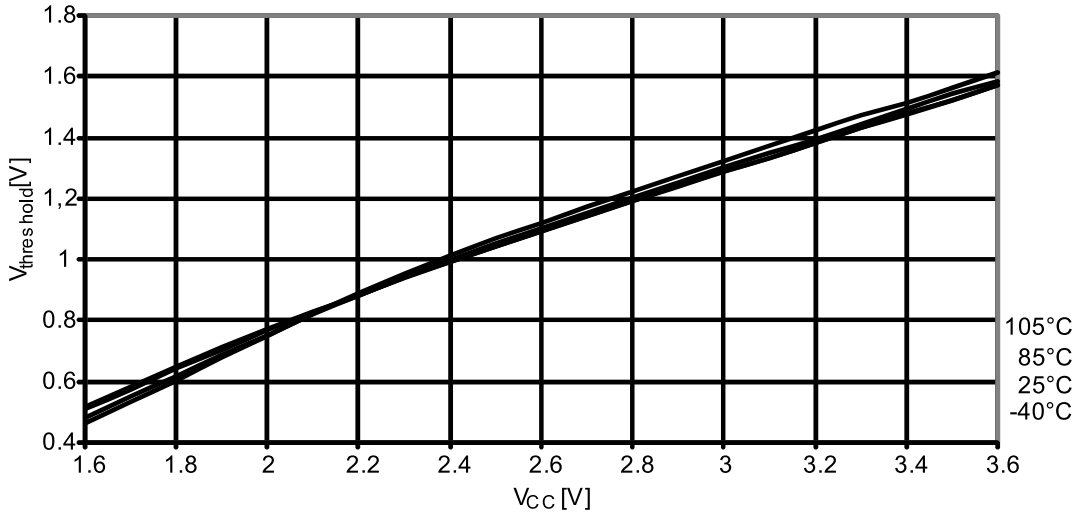


Figure 37-232. Reset pin input threshold voltage vs. V_{CC}.

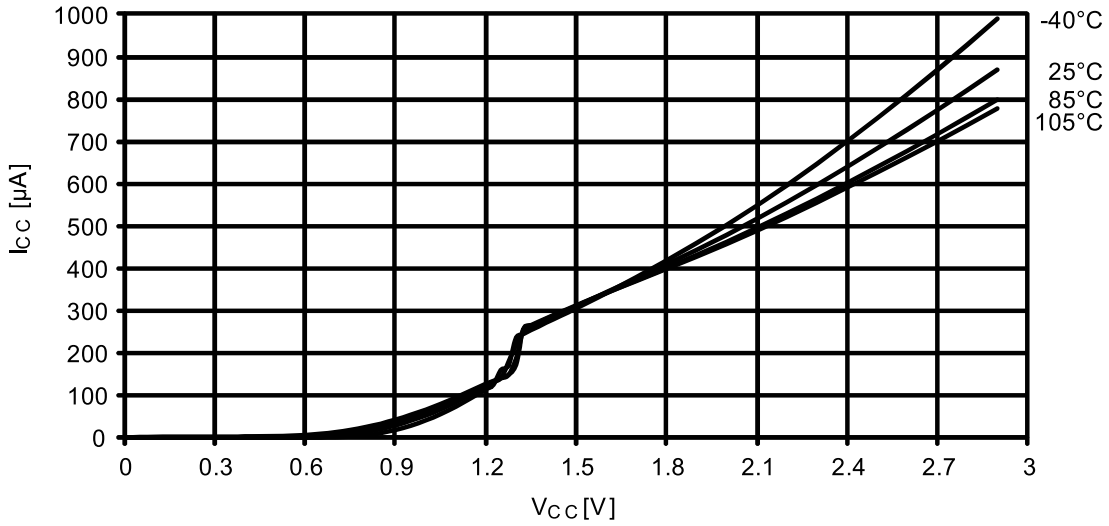
V_{IL} - Reset pin read as "0".



37.3.9 Power-on Reset Characteristics

Figure 37-233. Power-on reset current consumption vs. V_{CC}.

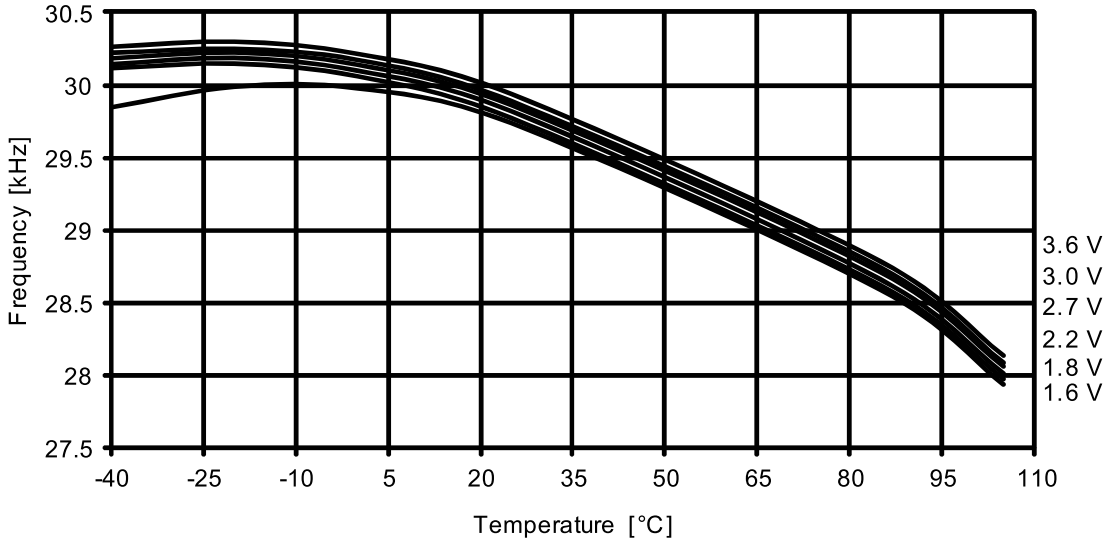
BOD level = 3.0V, enabled in continuous mode.



37.3.10 Oscillator Characteristics

37.3.10.1 Ultra Low-Power internal oscillator

Figure 37-234. Ultra Low-Power internal oscillator frequency vs. temperature.



37.3.10.2 32.768kHz Internal Oscillator

Figure 37-235. 32.768kHz internal oscillator frequency vs. temperature.

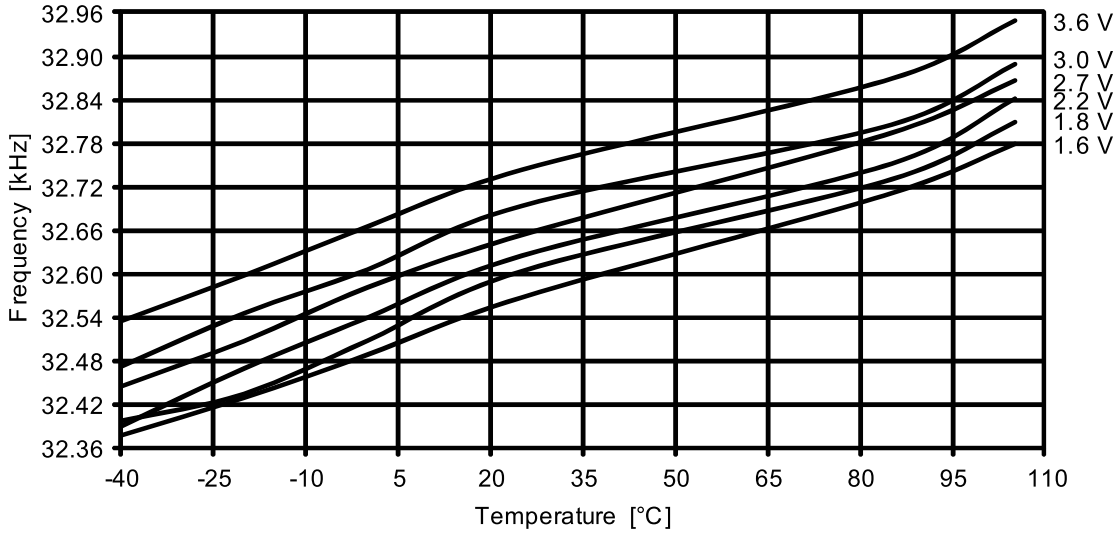
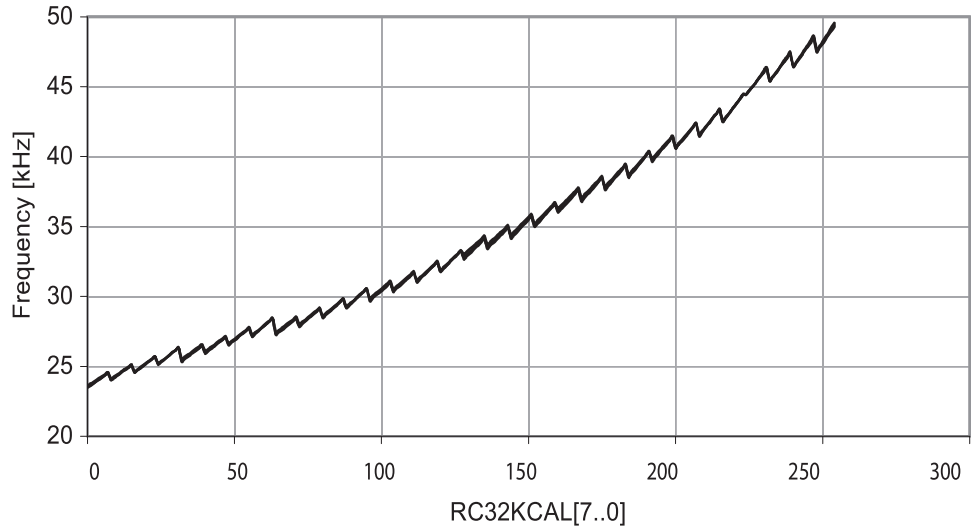


Figure 37-236. 32.768kHz internal oscillator frequency vs. calibration value.

V_{CC} = 3.0V, T = 25°C.



37.3.10.3 2MHz Internal Oscillator

Figure 37-237. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

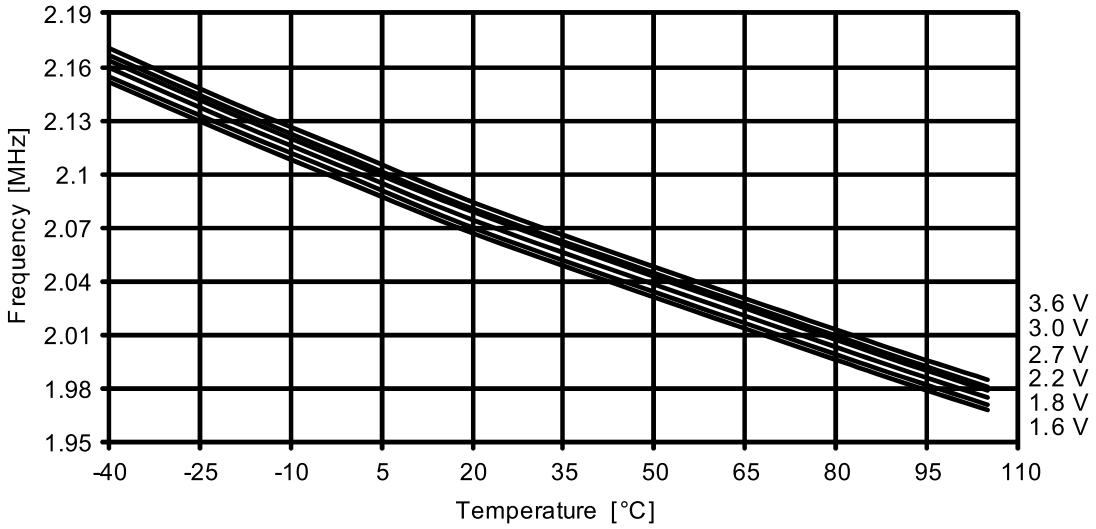


Figure 37-238. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.

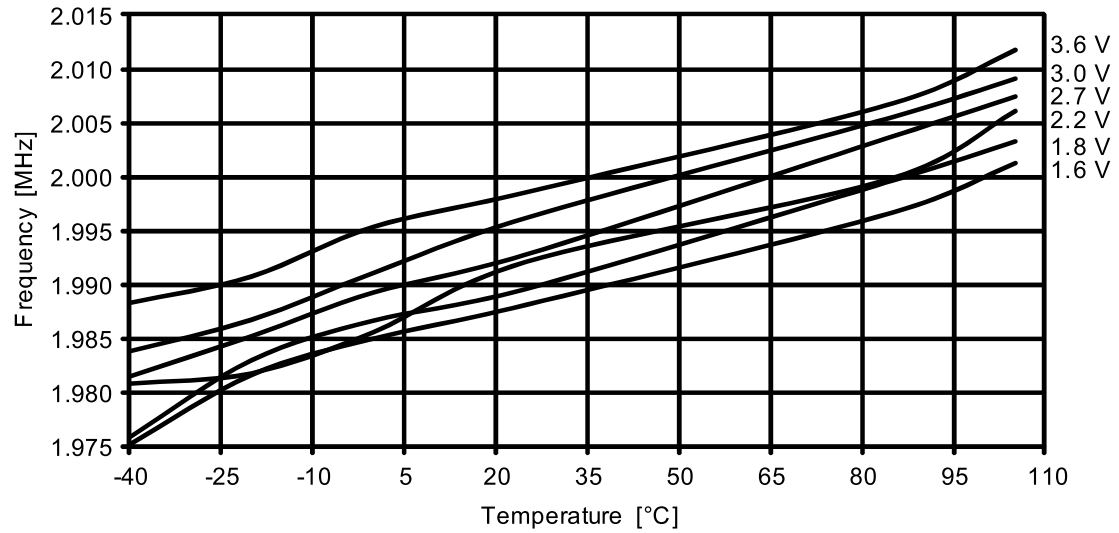
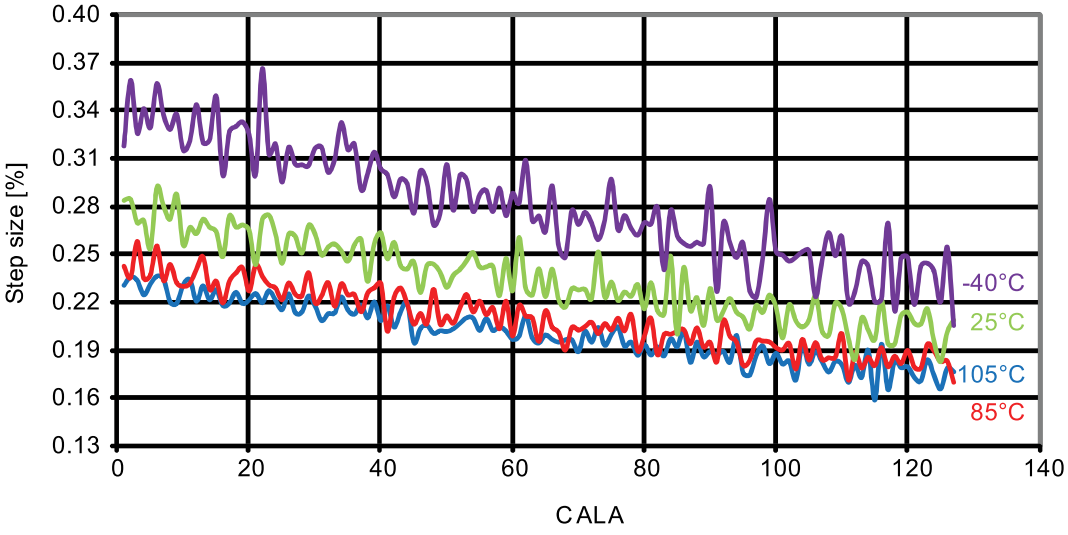


Figure 37-239. 2MHz internal oscillator CALA calibration step size.

V_{CC} = 3V.



37.3.10.4 32MHz Internal Oscillator

Figure 37-240. 32MHz internal oscillator frequency vs. temperature.
DFLL disabled.

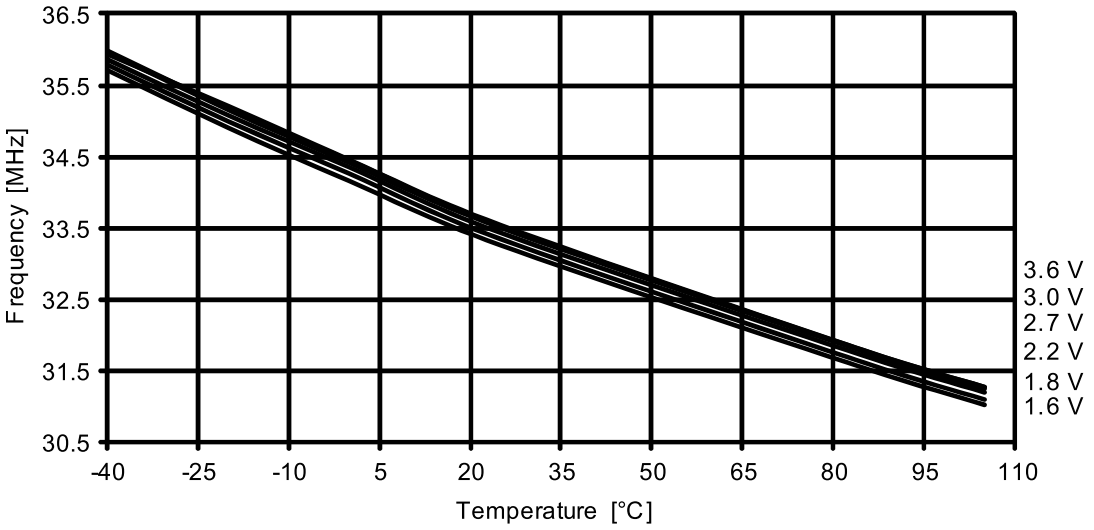


Figure 37-241. 32MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.

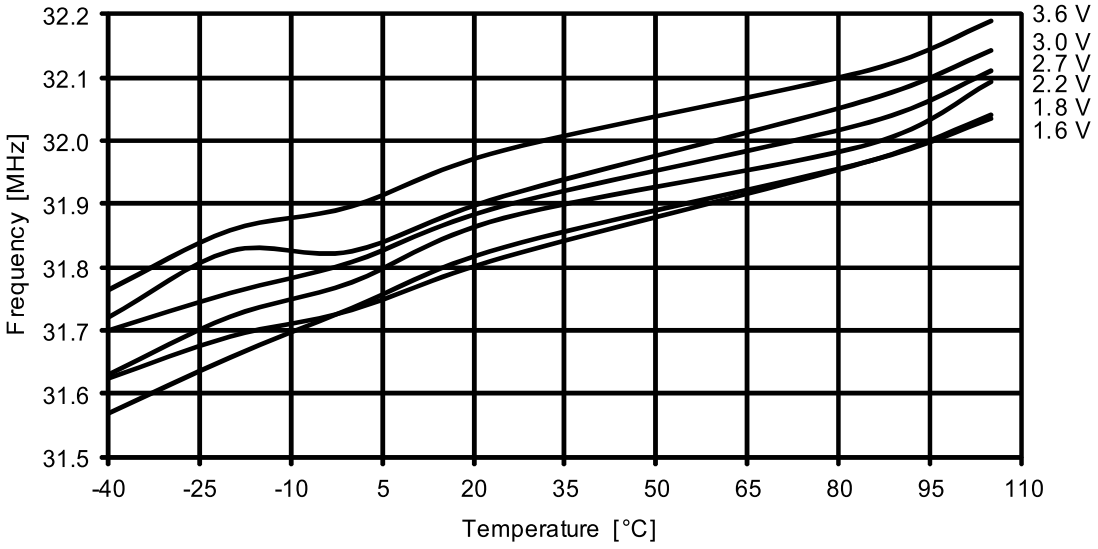


Figure 37-242. 32MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.

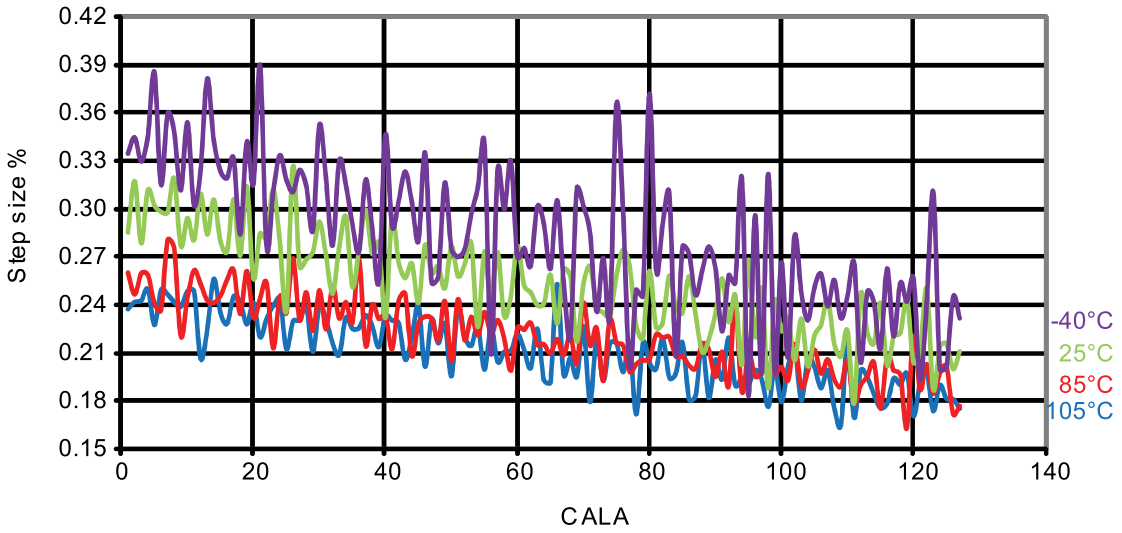
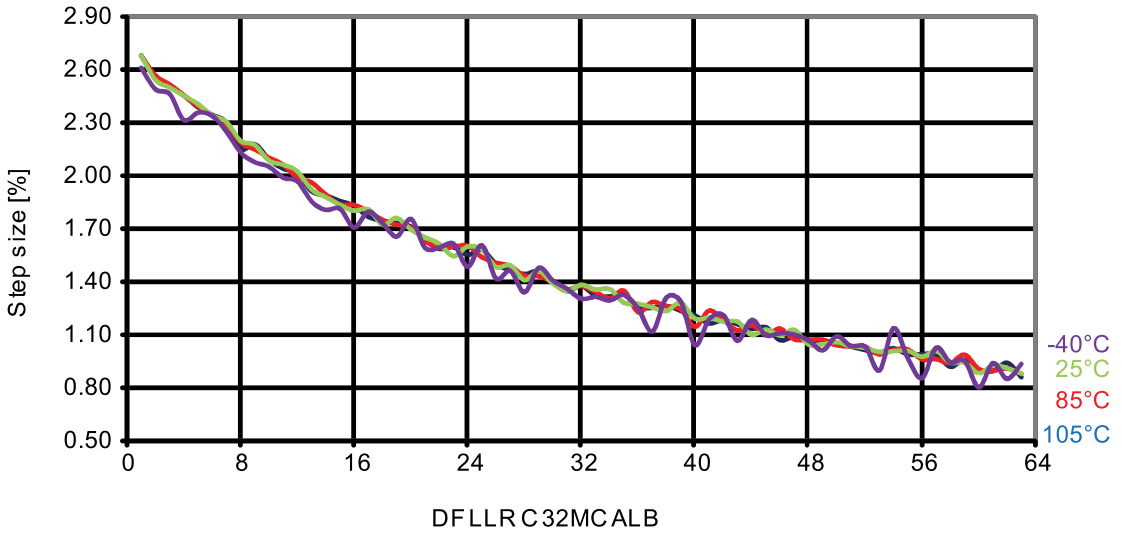


Figure 37-243. 32MHz internal oscillator frequency vs. CALB calibration value.

V_{CC} = 3.0V.



37.3.10.5 32MHz internal oscillator calibrated to 48MHz

Figure 37-244. 48MHz internal oscillator frequency vs. temperature.
DFLL disabled.

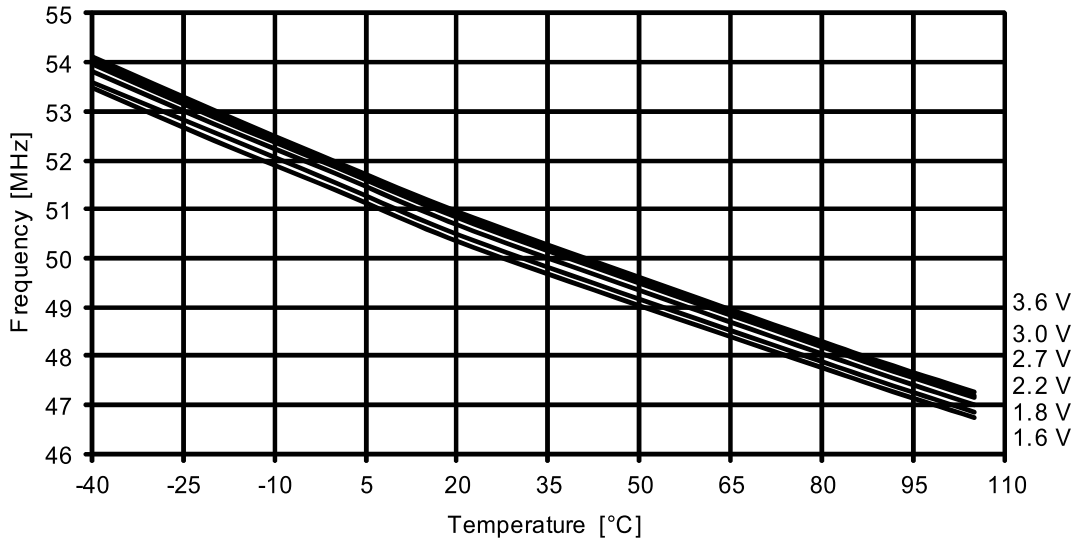


Figure 37-245. 48MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.

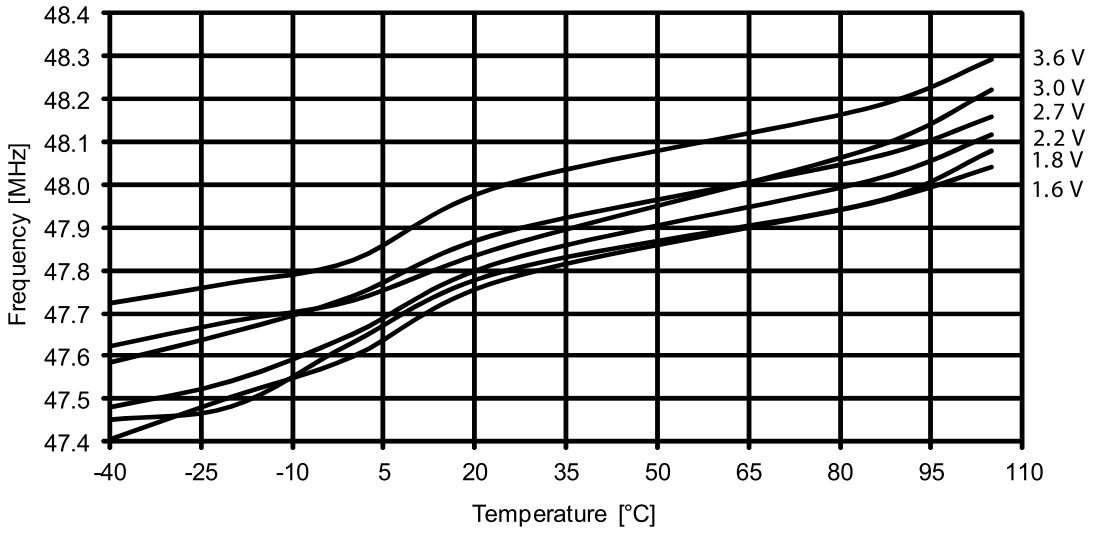
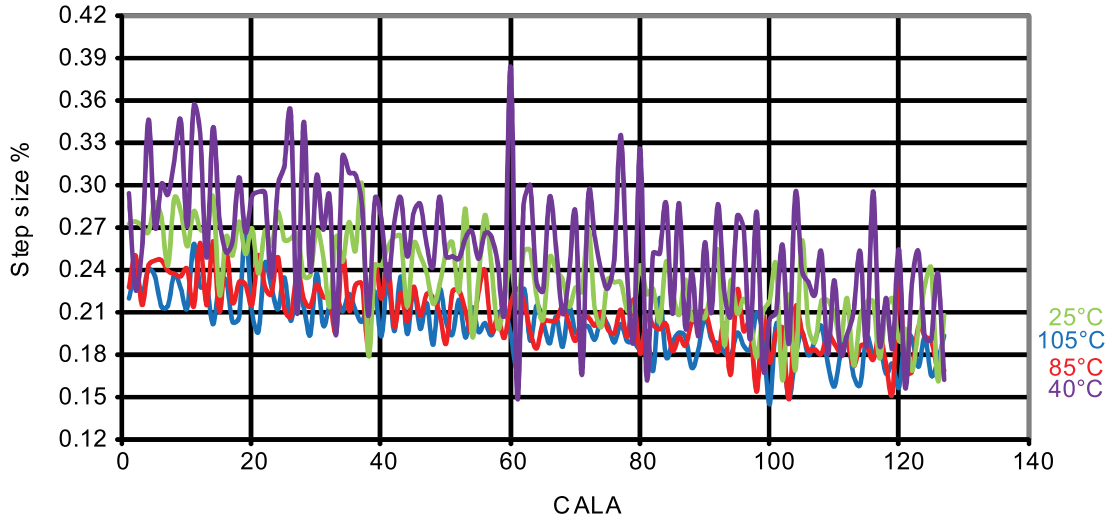


Figure 37-246. 48MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.



37.3.11 Two-Wire Interface characteristics

Figure 37-247. SDA hold time vs. Vcc.

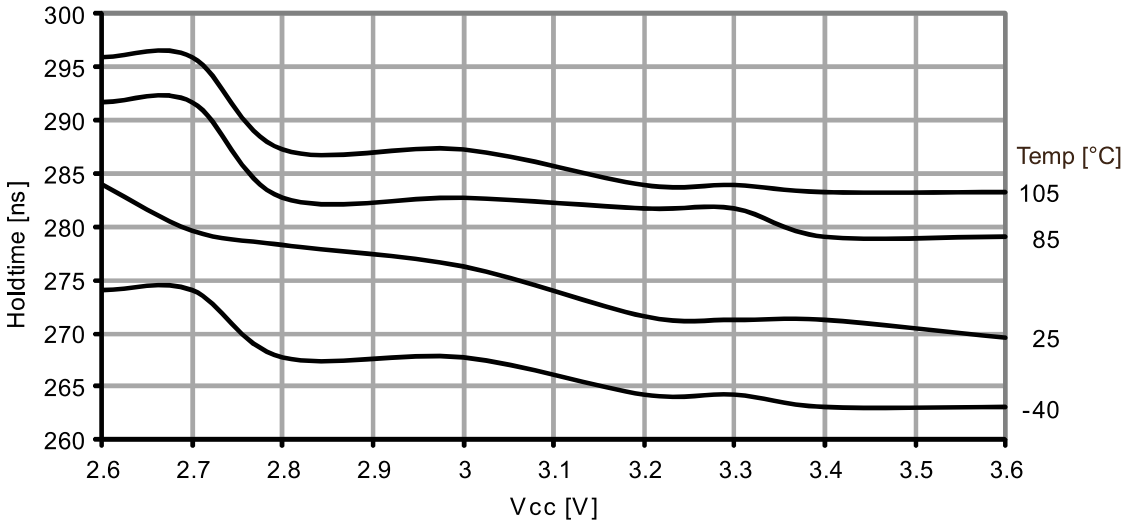
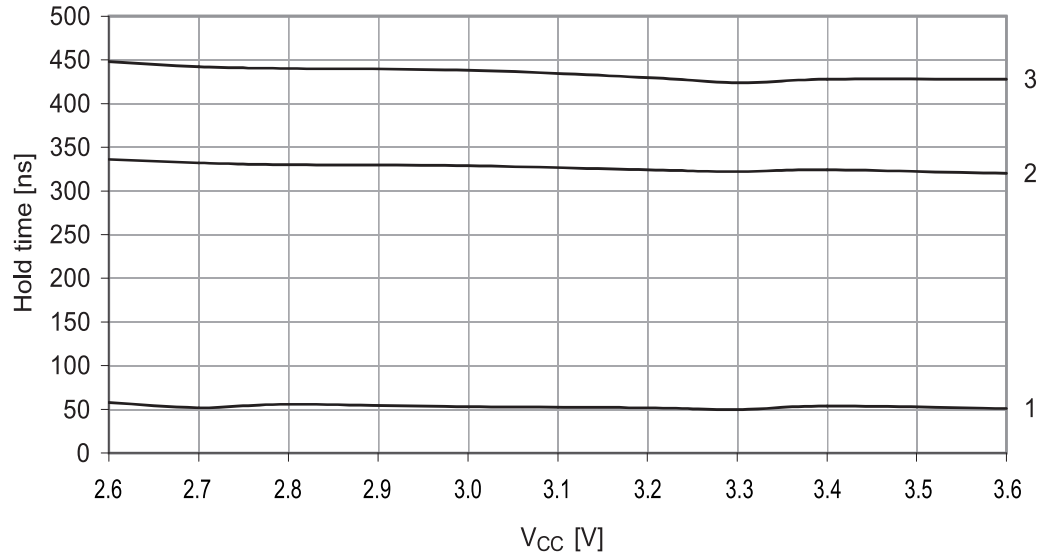
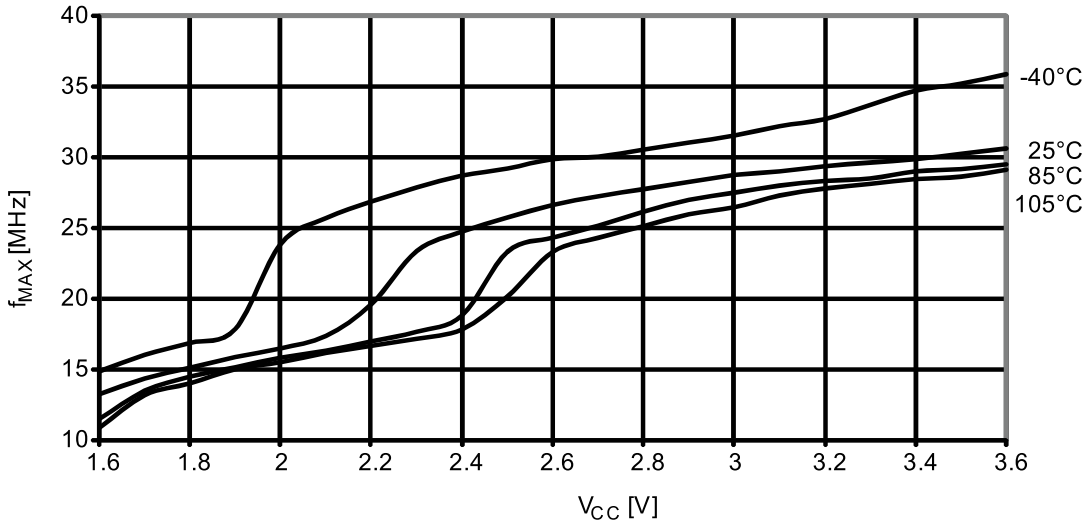


Figure 37-248. SDA hold time vs. supply voltage.



37.3.12 PDI characteristics

Figure 37-249. Maximum PDI frequency vs. V_{CC}.



37.4 ATxmega256A3U

37.4.1 Current consumption

37.4.1.1 Active mode supply current

Figure 37-250. Active supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

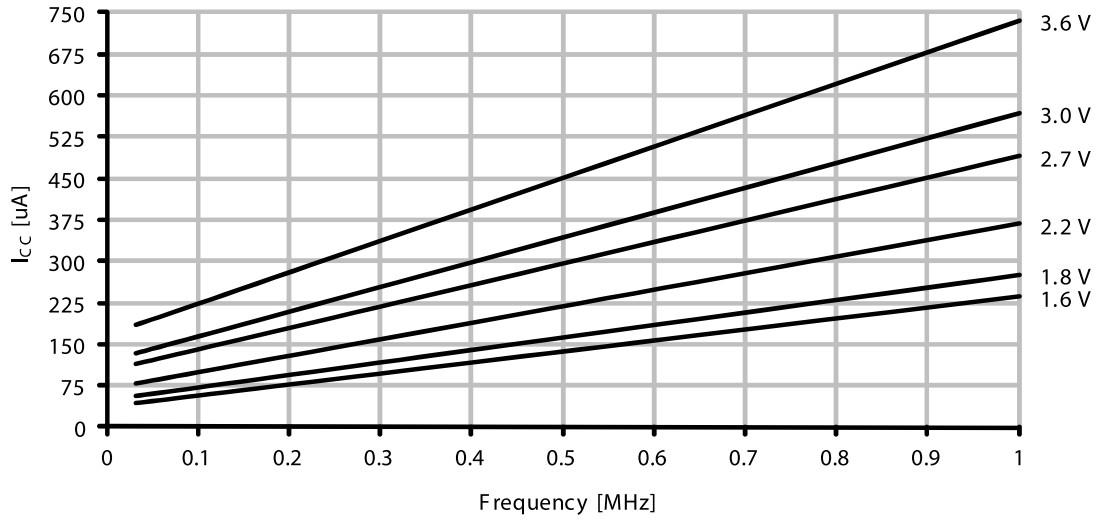


Figure 37-251. Active supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

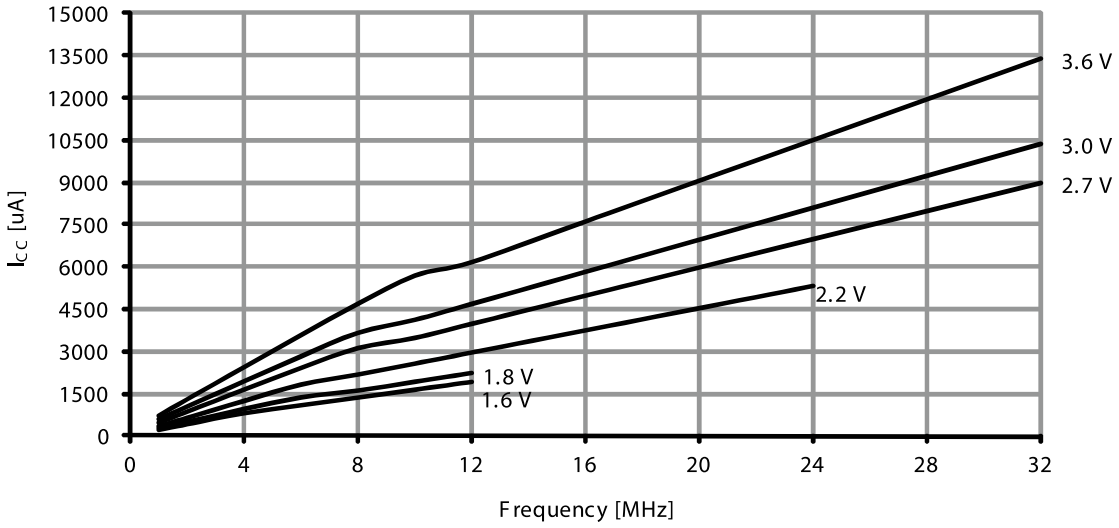


Figure 37-252. Active mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

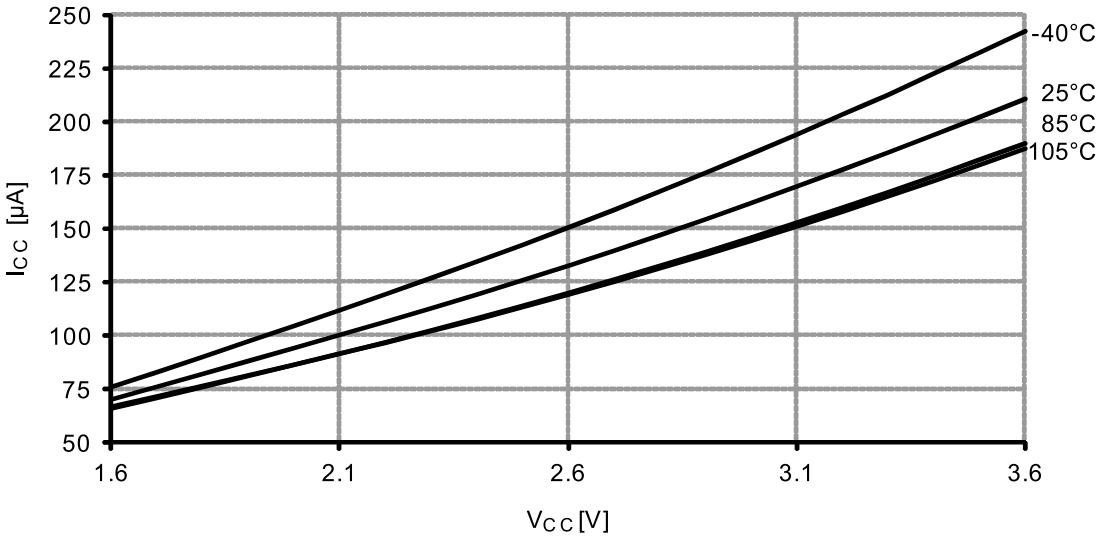


Figure 37-253. Active mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

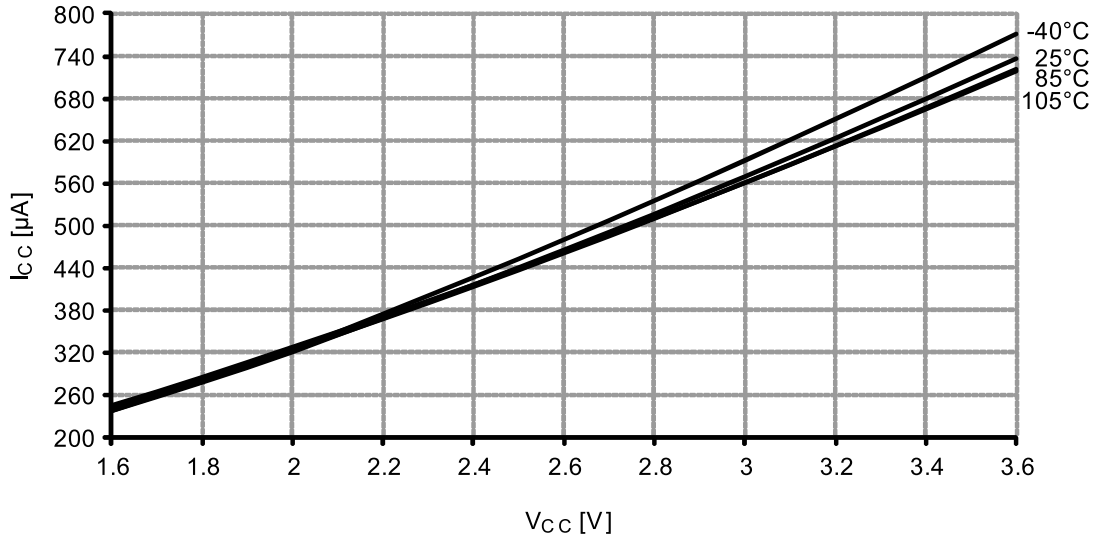


Figure 37-254. Active mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

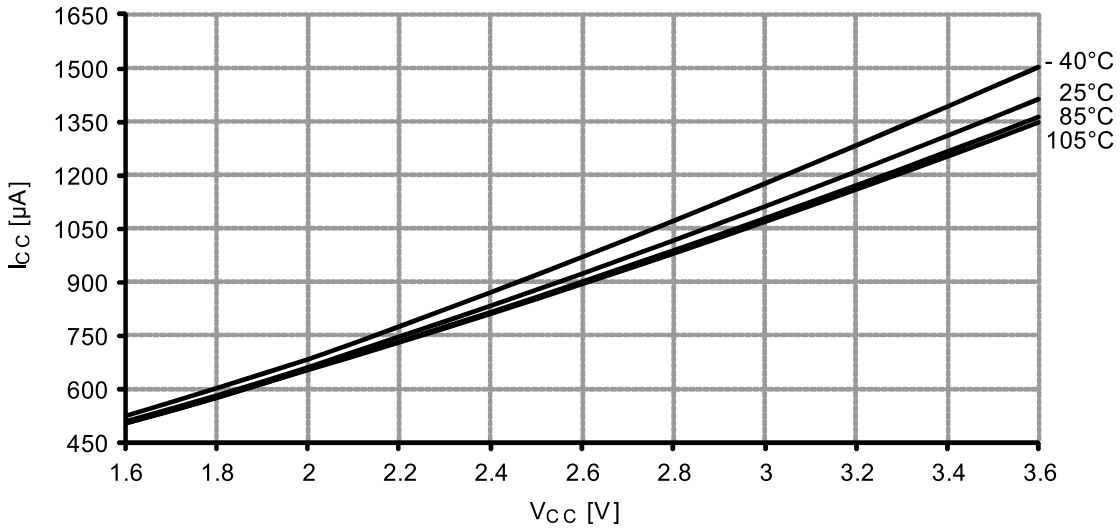


Figure 37-255. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

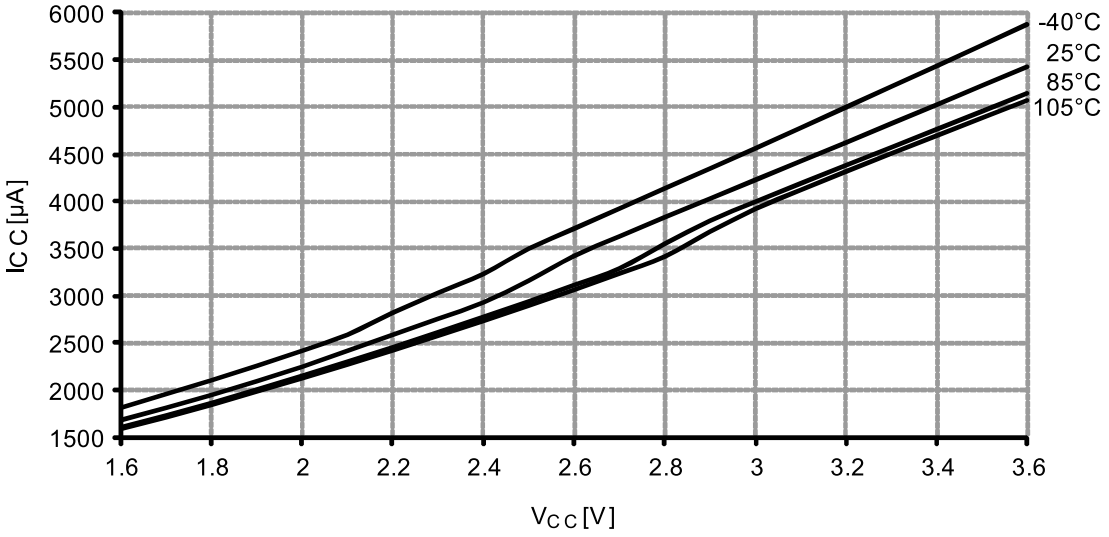
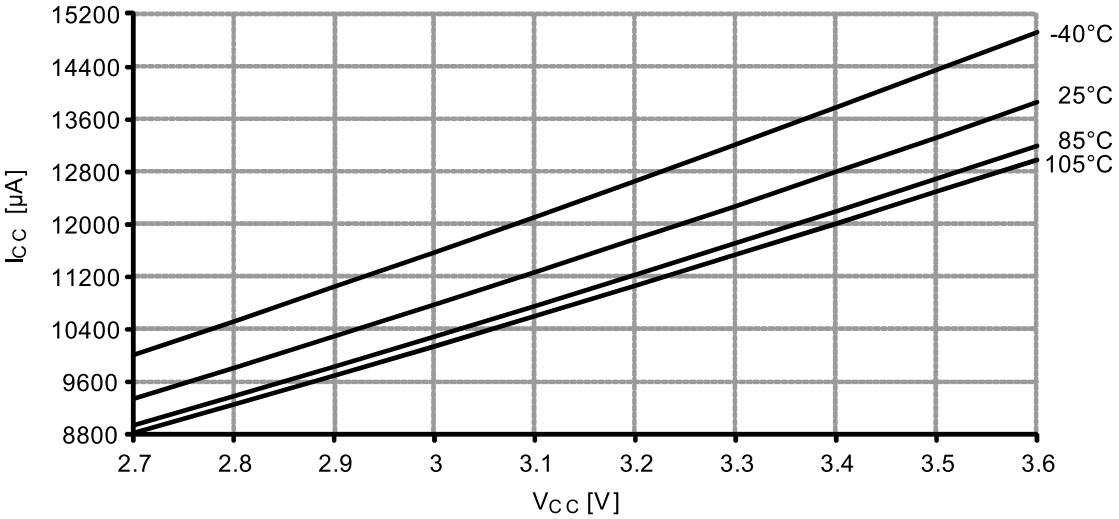


Figure 37-256. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



37.4.1.2 Idle mode supply current

Figure 37-257. Idle mode supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C.

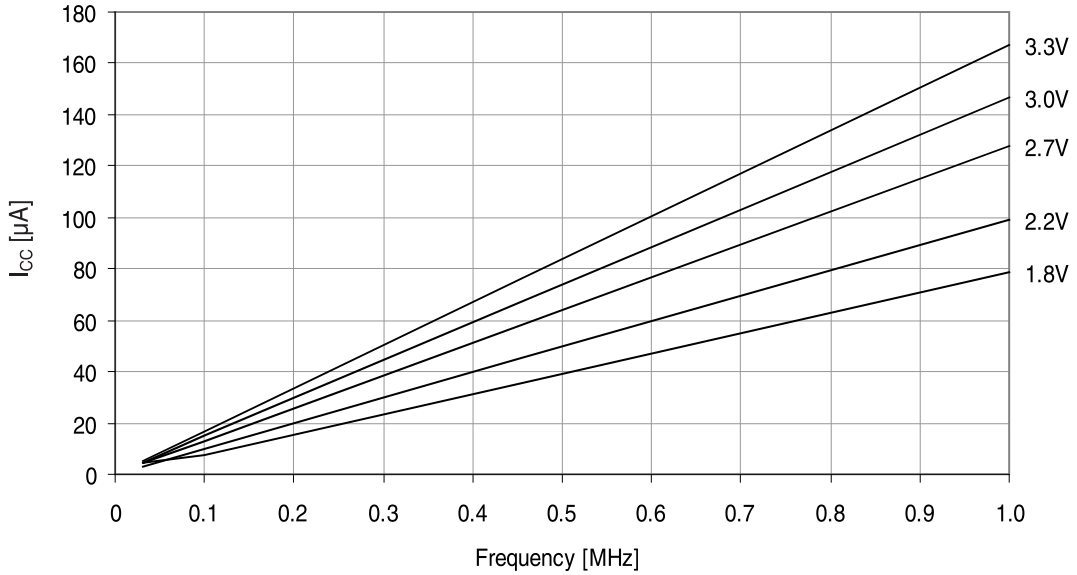


Figure 37-258. Idle mode supply current vs. frequency.

f_{SYS} = 1 - 32MHz external clock, T = 25°C.

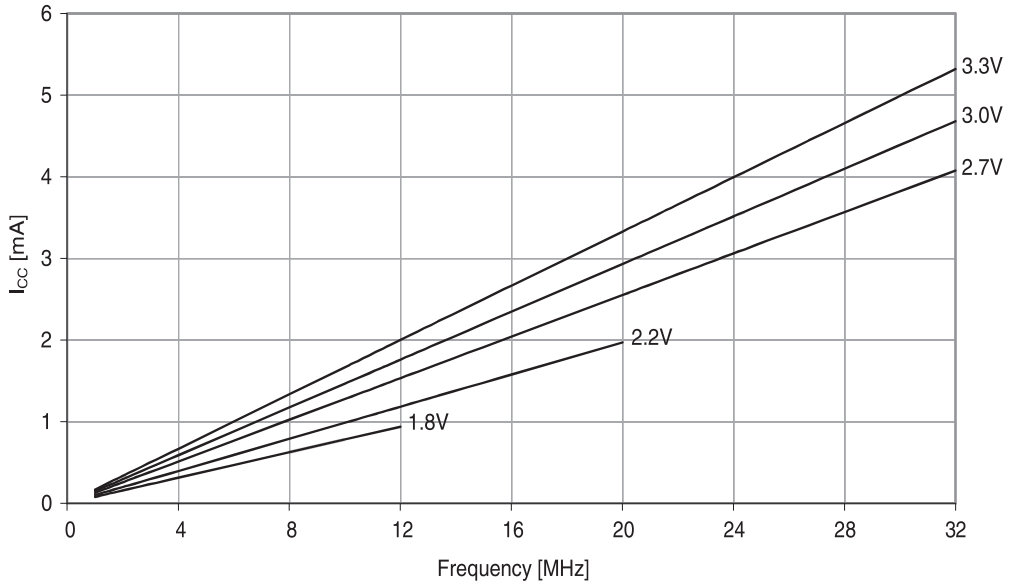


Figure 37-259. Idle mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

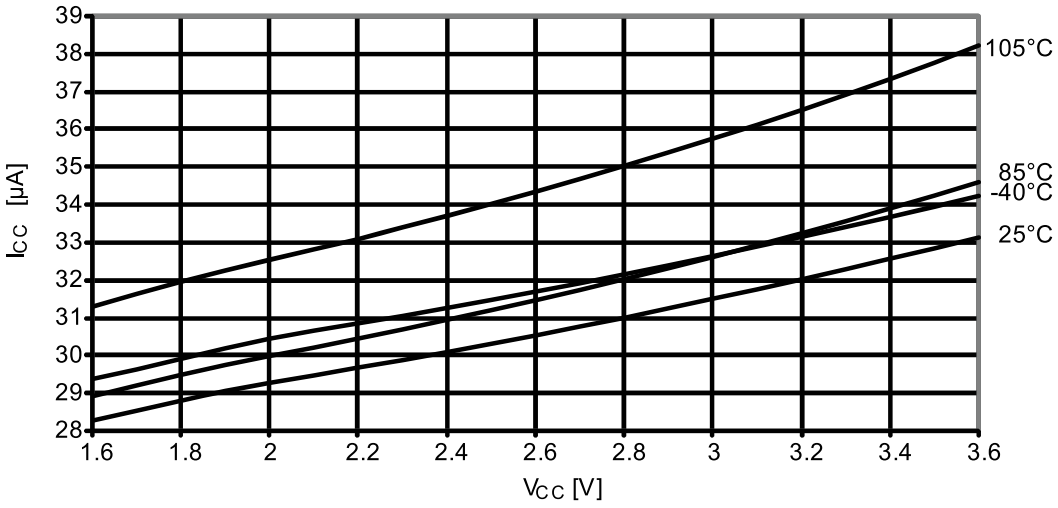


Figure 37-260. Idle mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

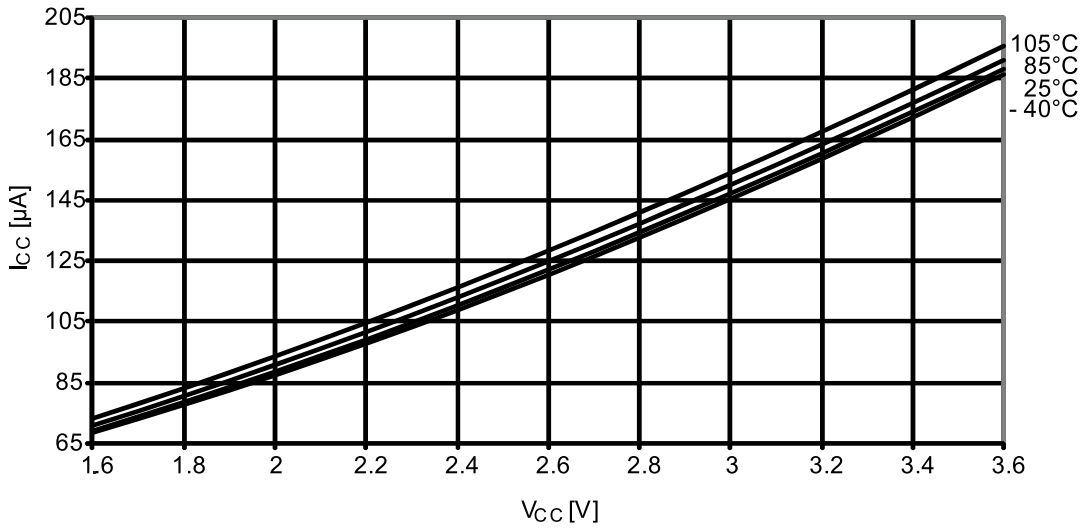


Figure 37-261. Idle mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

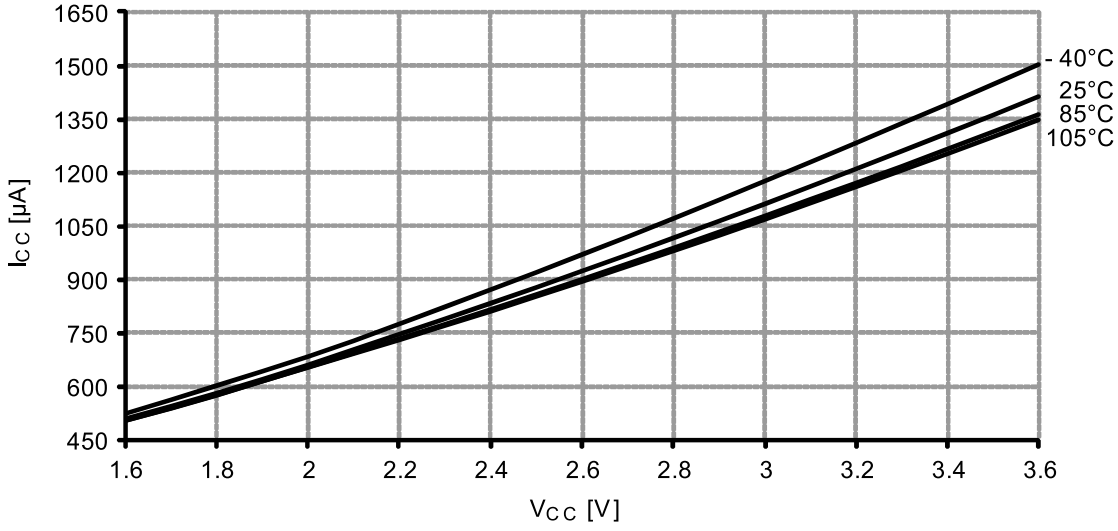


Figure 37-262. Idle mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

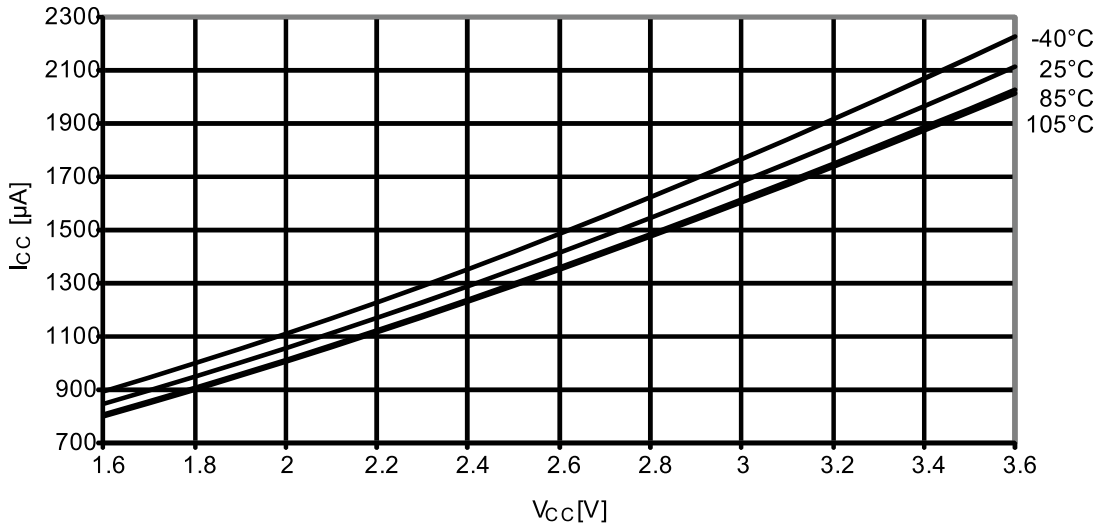
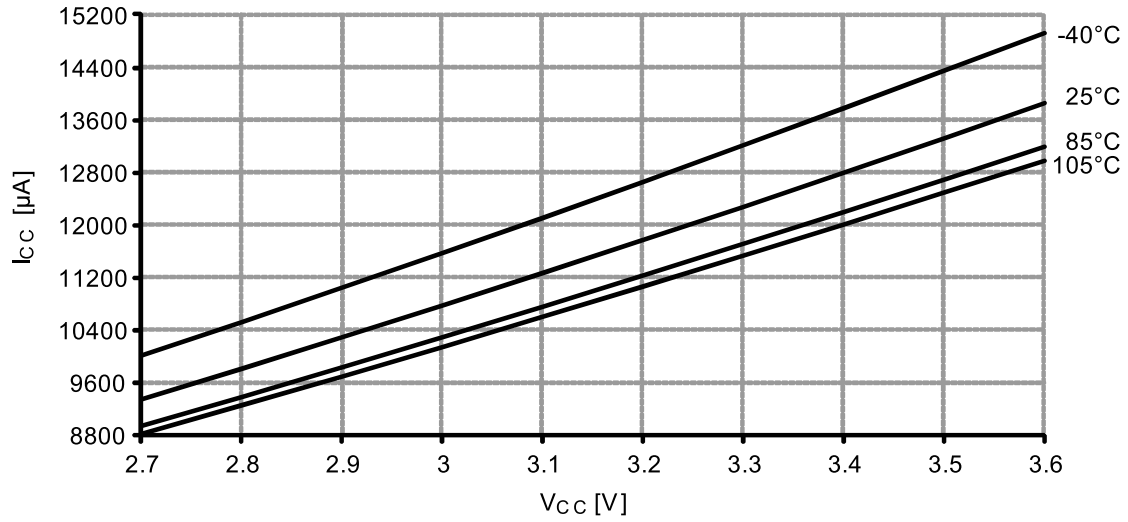


Figure 37-263. Idle mode current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



37.4.1.3 Power-down mode supply current

Figure 37-264. Power-down mode supply current vs. V_{CC}.
All functions disabled.

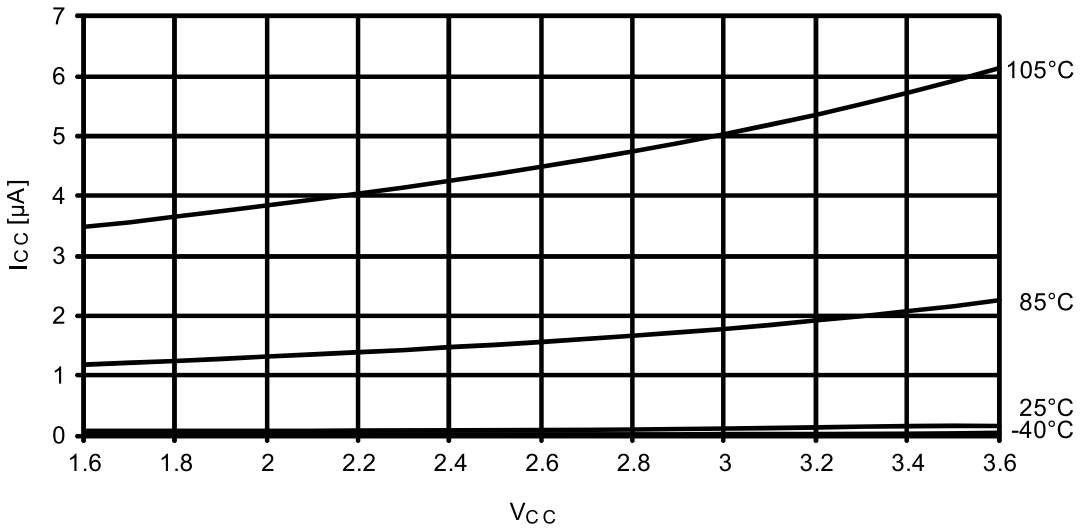
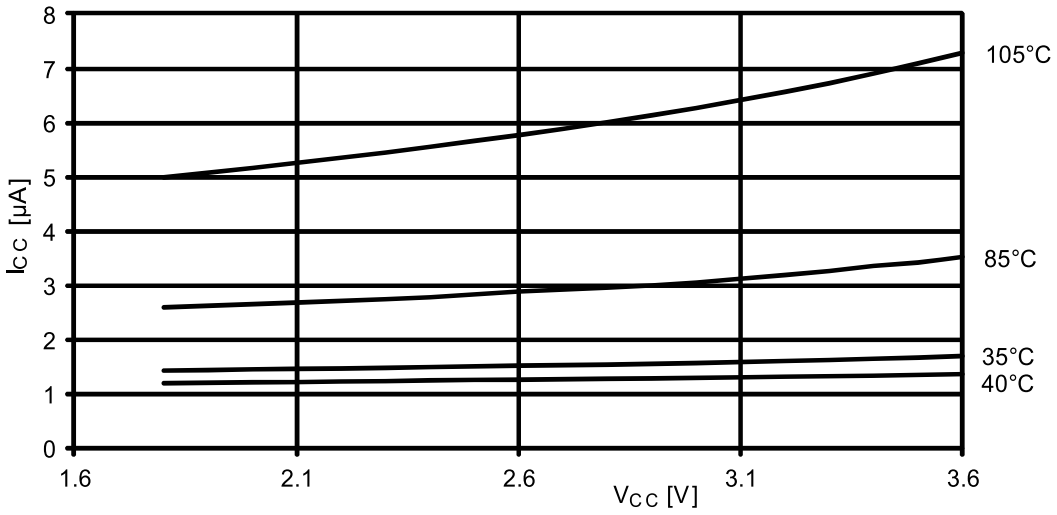


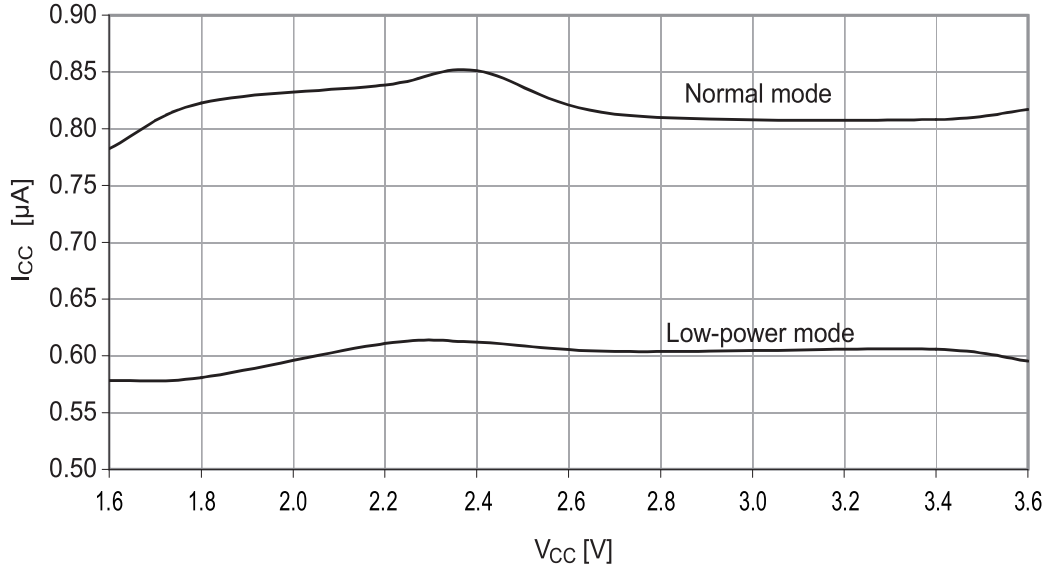
Figure 37-265. Power-down mode supply current vs. V_{CC}.
Watchdog and sampled BOD enabled.



37.4.1.4 Power-save mode supply current

Figure 37-266. Power-save mode supply current vs. V_{CC}.

Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC.



37.4.1.5 Standby mode supply current

Figure 37-267. Standby supply current vs. V_{CC}.

Standby, f_{SYS} = 1MHz.

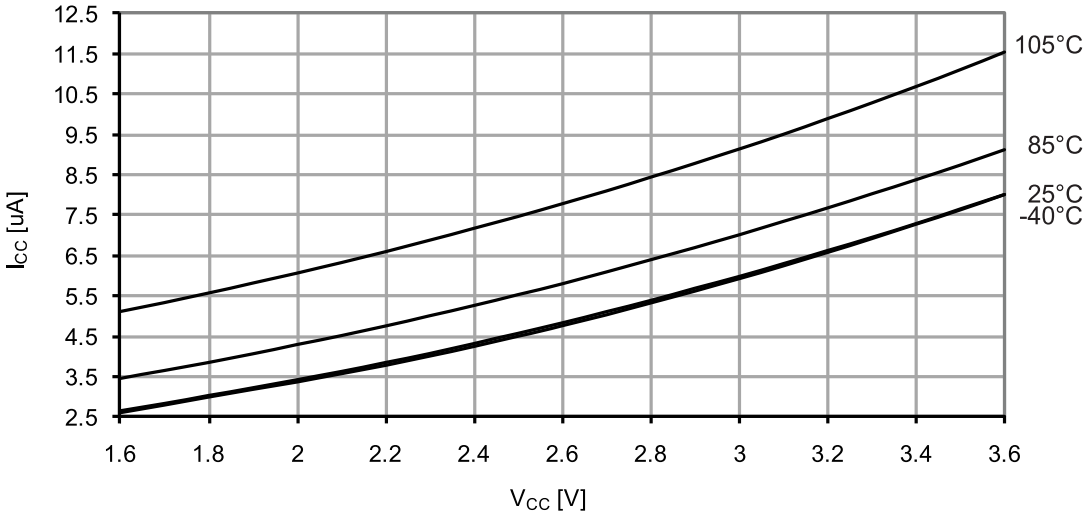
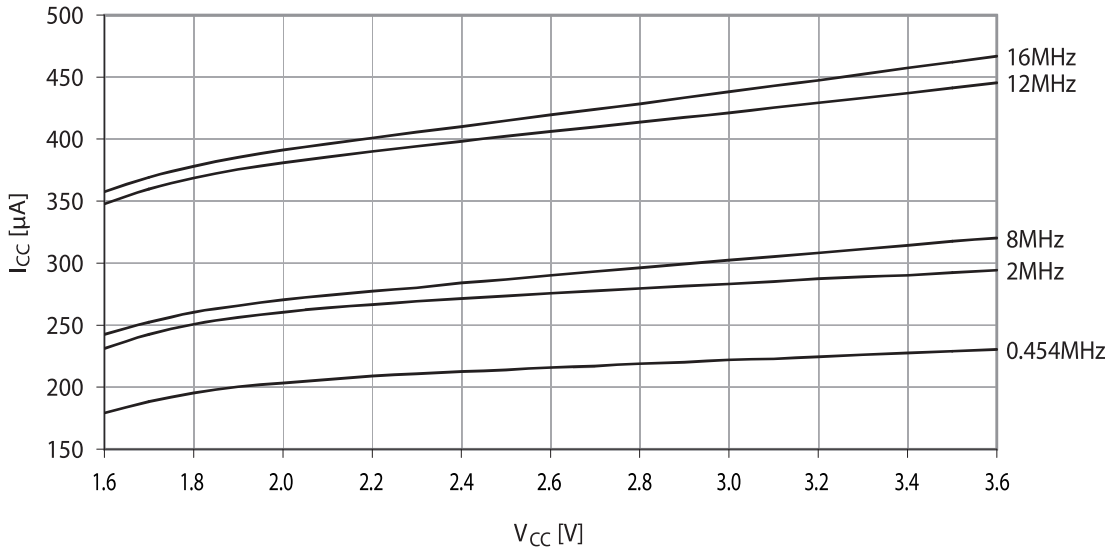


Figure 37-268. Standby supply current vs. V_{CC}.

25°C, running from different crystal oscillators.



37.4.2 I/O Pin Characteristics

37.4.2.1 Pull-up

Figure 37-269. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 1.8V.

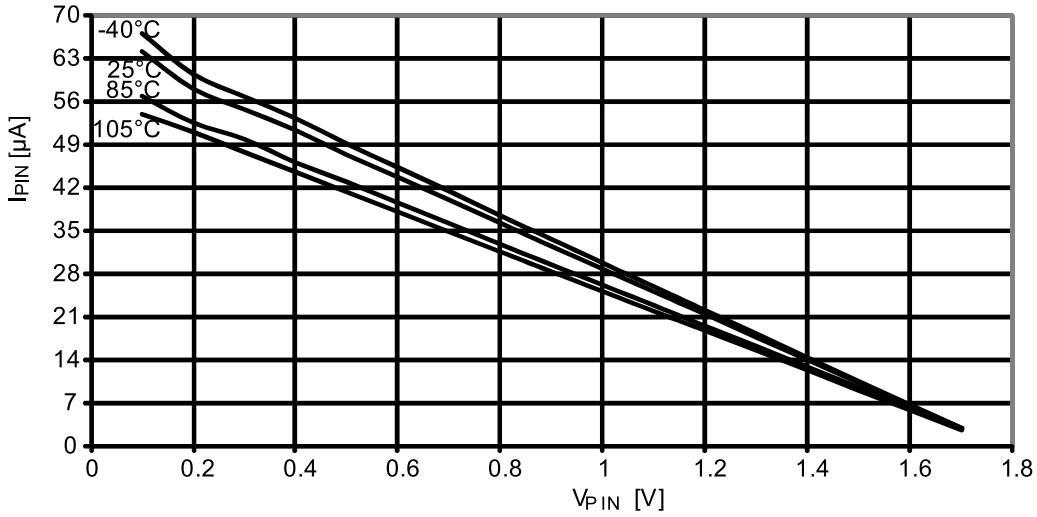


Figure 37-270. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 3.0V.

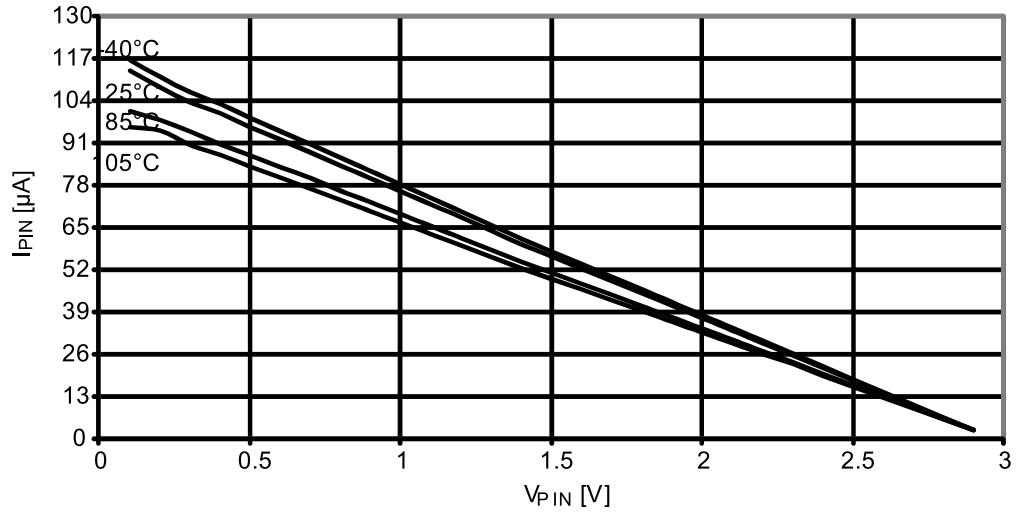
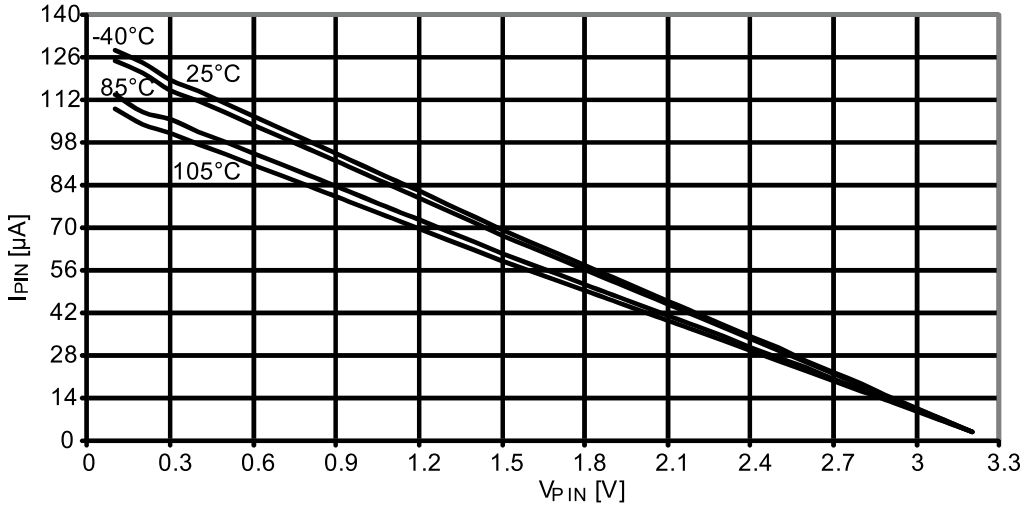


Figure 37-271. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 3.3V.



37.4.2.2 Output Voltage vs. Sink/Source Current

Figure 37-272. I/O pin output voltage vs. source current.
V_{CC} = 1.8V.

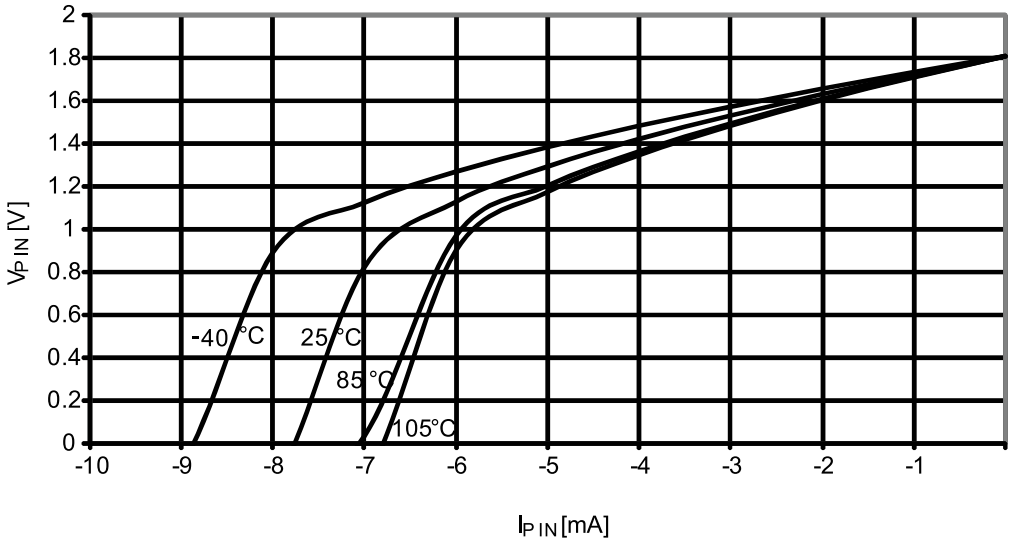


Figure 37-273. I/O pin output voltage vs. source current.
V_{CC} = 3.0V.

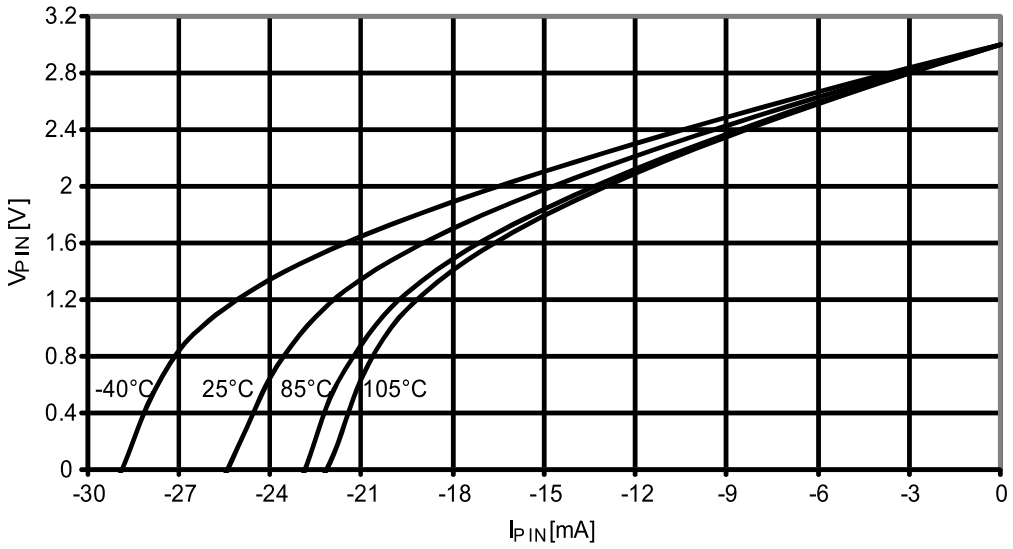


Figure 37-274. I/O pin output voltage vs. source current.

V_{CC} = 3.3V.

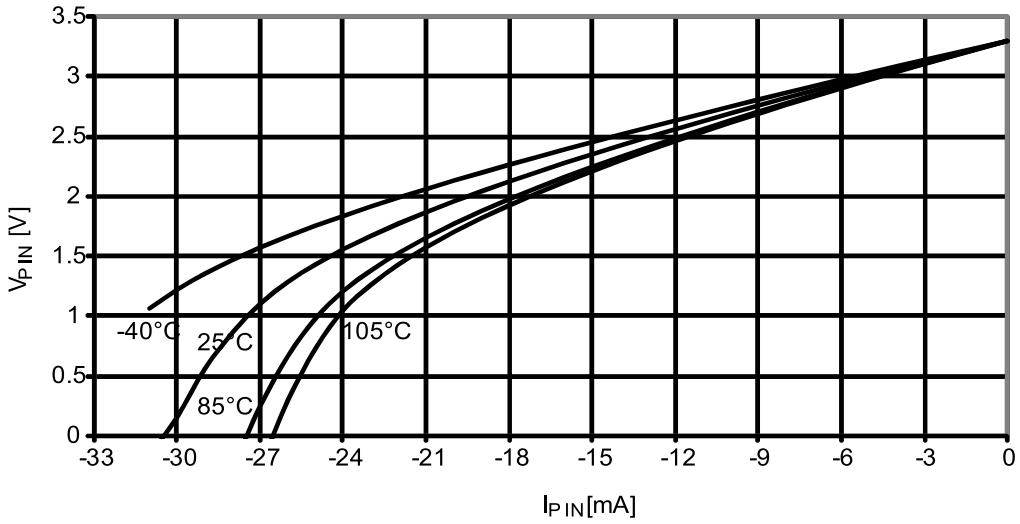


Figure 37-275. I/O pin output voltage vs. source current.

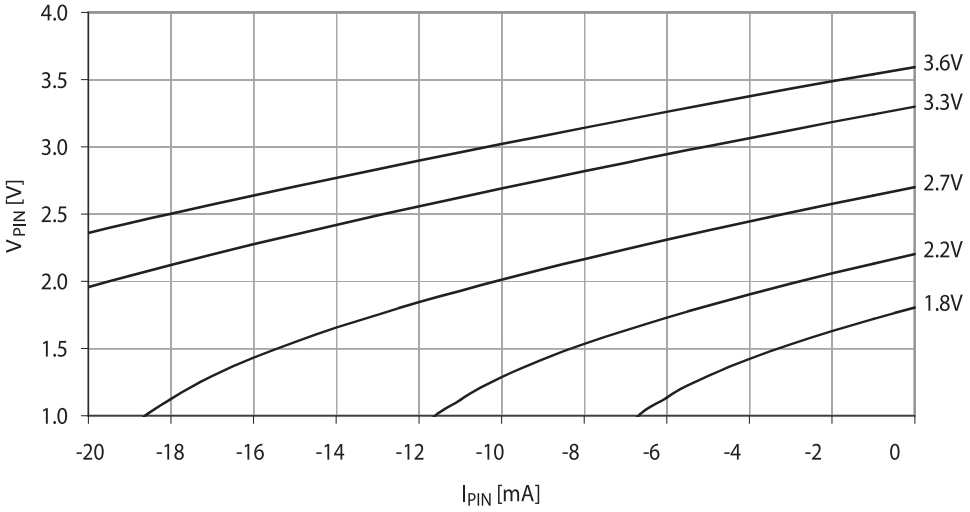


Figure 37-276. I/O pin output voltage vs. sink current.

V_{CC} = 1.8V.

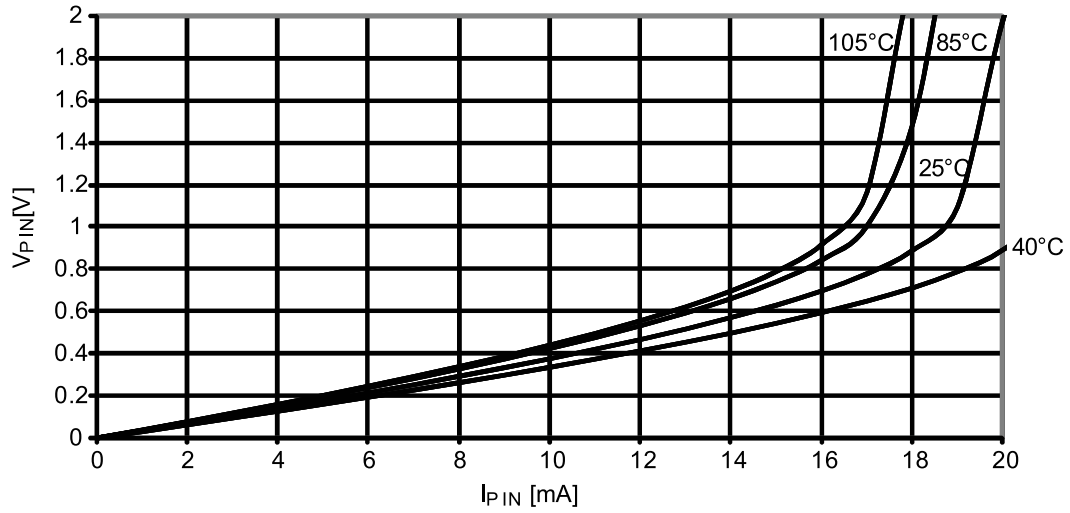


Figure 37-277. I/O pin output voltage vs. sink current.

V_{CC} = 3.0V.

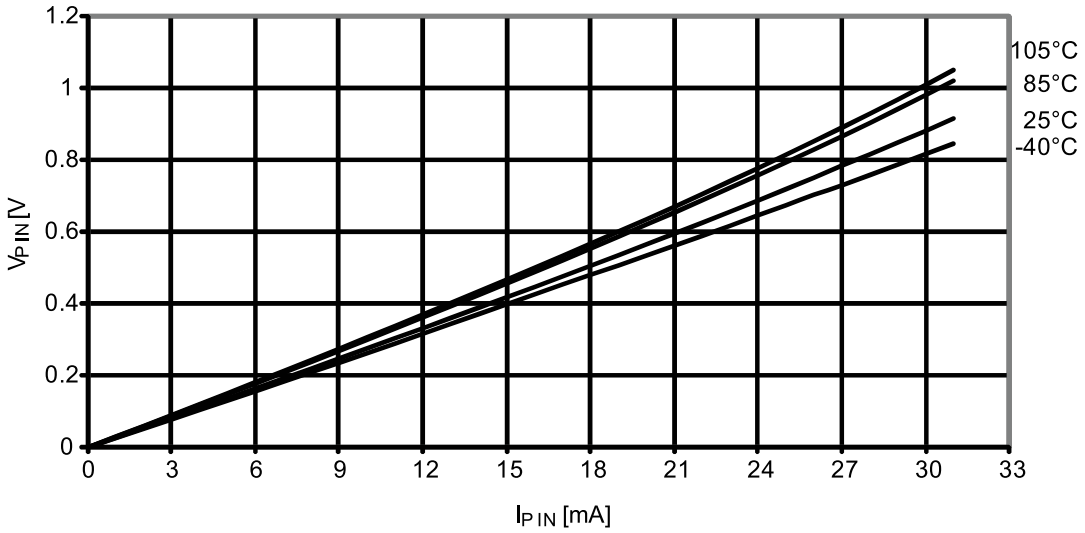


Figure 37-278. I/O pin output voltage vs. sink current.

V_{CC} = 3.3V.

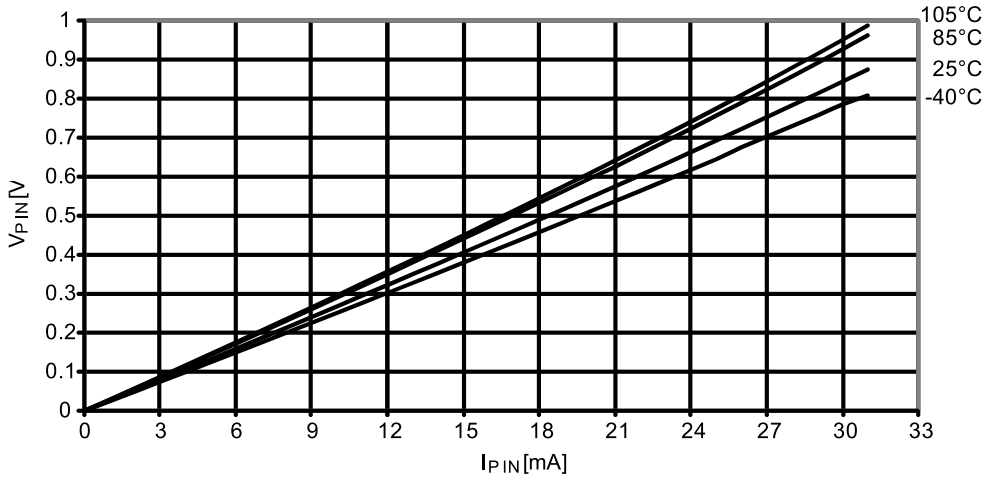
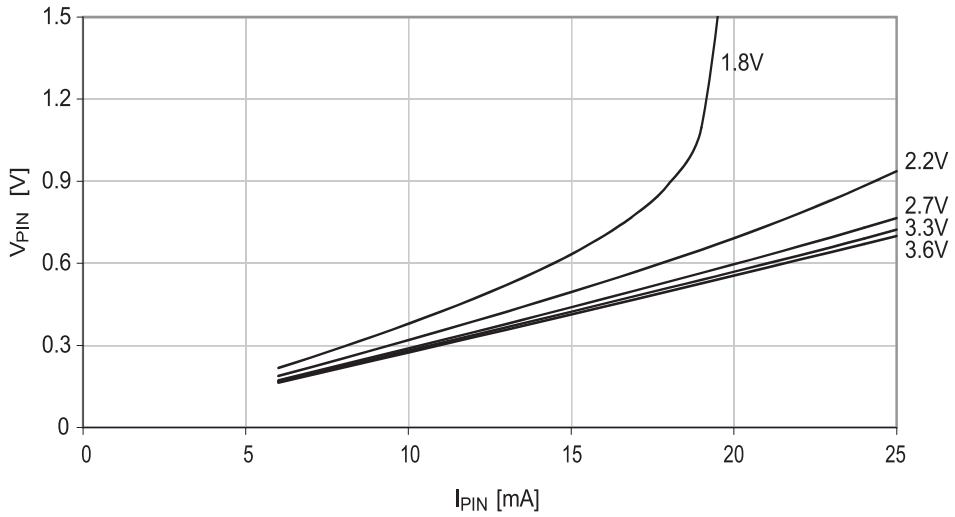


Figure 37-279. I/O pin output voltage vs. sink current.



37.4.2.3 Thresholds and Hysteresis

Figure 37-280. I/O pin input threshold voltage vs. V_{CC}.
T = 25°C.

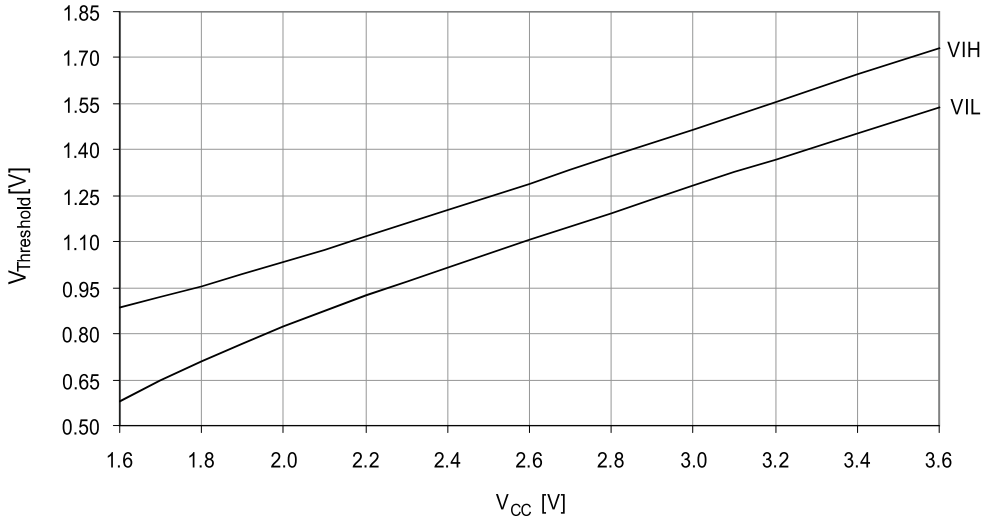


Figure 37-281. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} I/O pin read as "1".

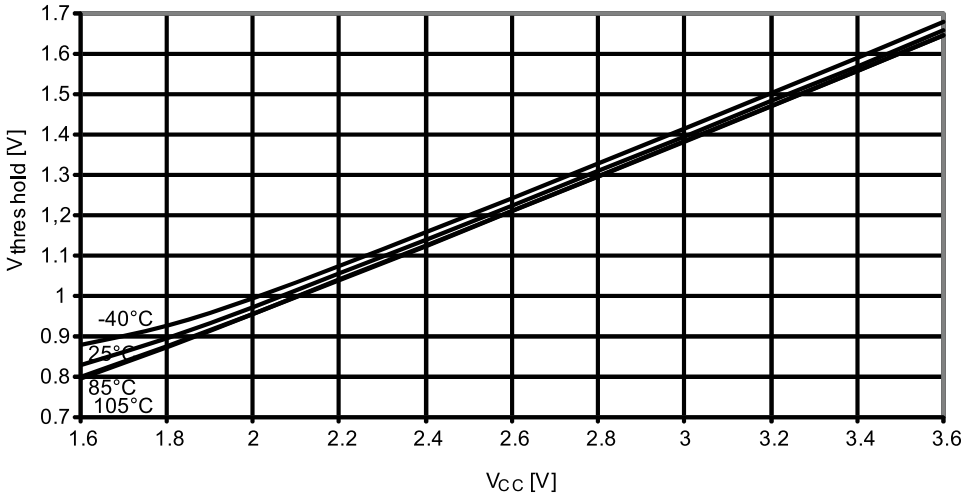


Figure 37-282. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

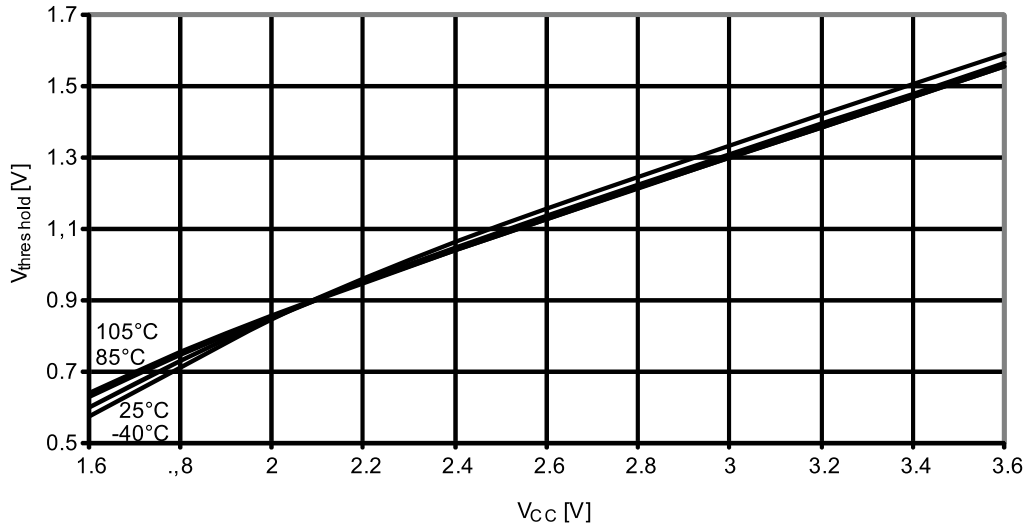
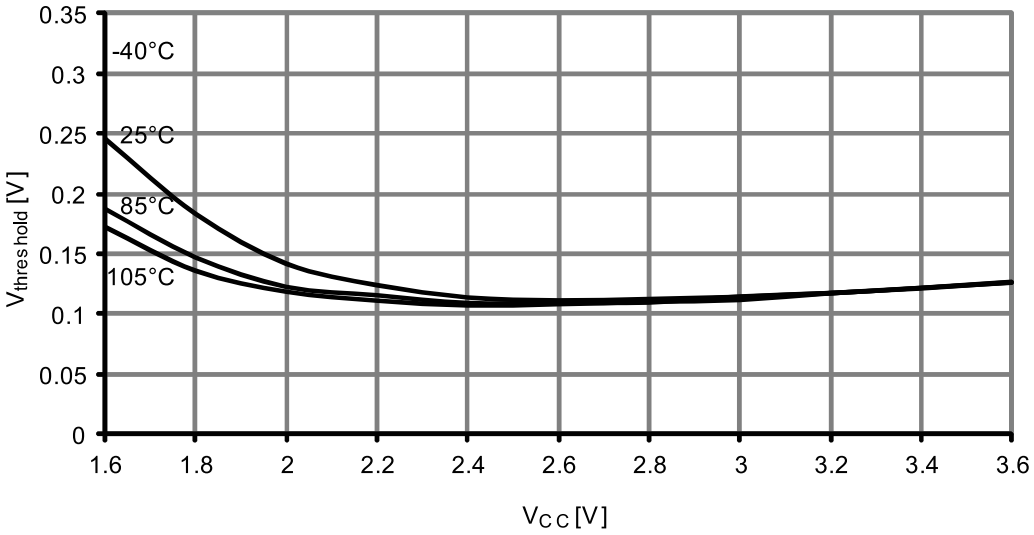


Figure 37-283. I/O pin input hysteresis vs. V_{CC}.



37.4.3 ADC Characteristics

Figure 37-284. INL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

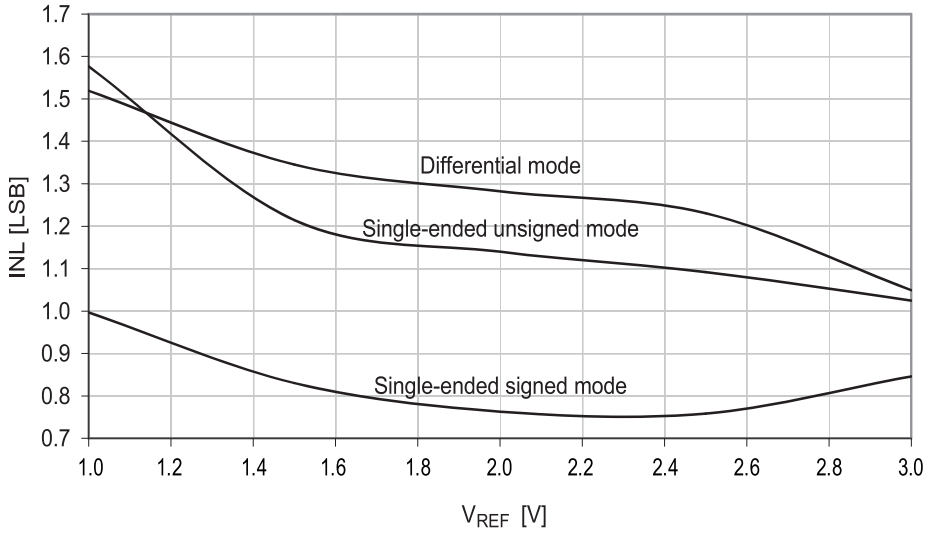


Figure 37-285. INL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

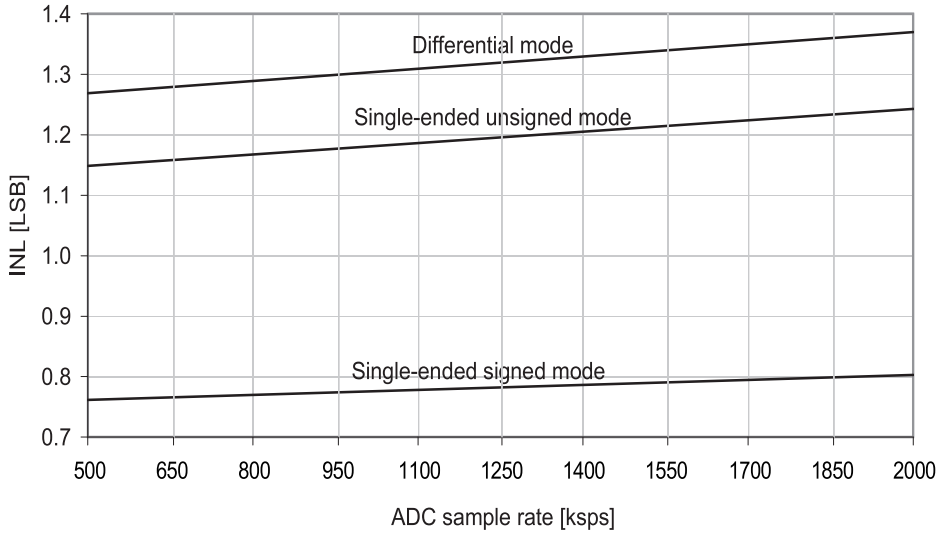


Figure 37-286. INL error vs. input code.

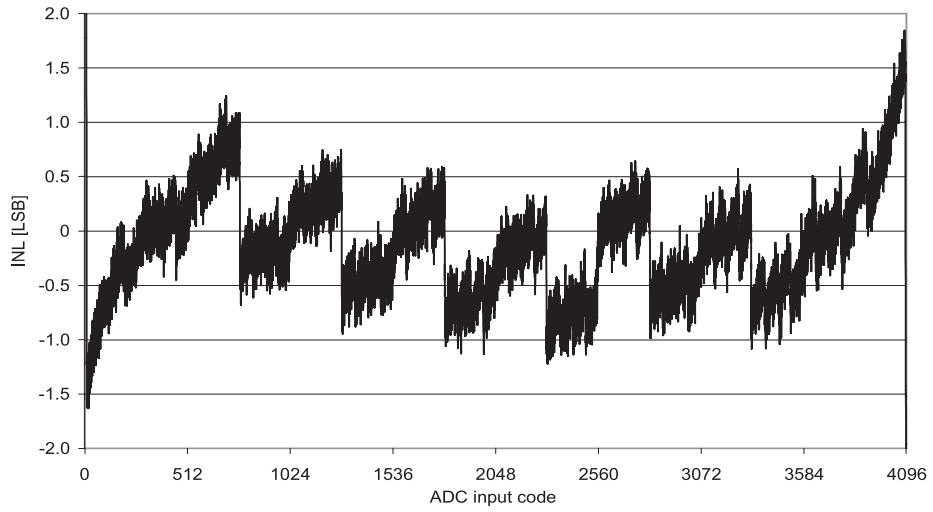


Figure 37-287. DNL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

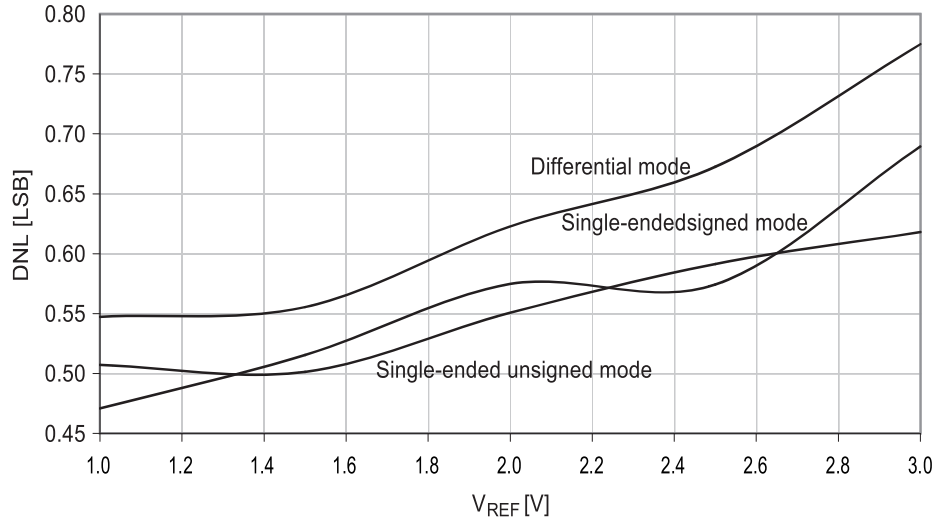


Figure 37-288. DNL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

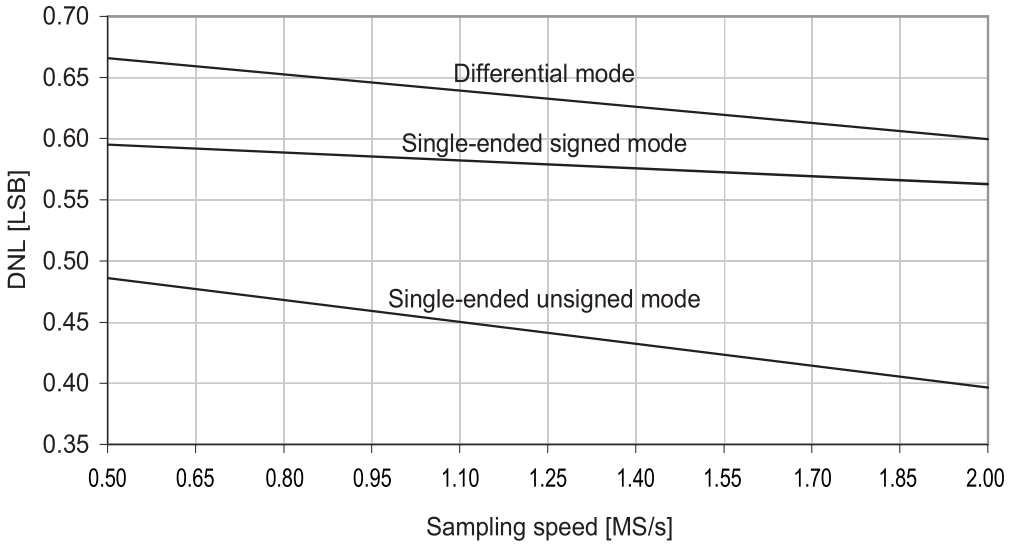


Figure 37-289. DNL error vs. input code.

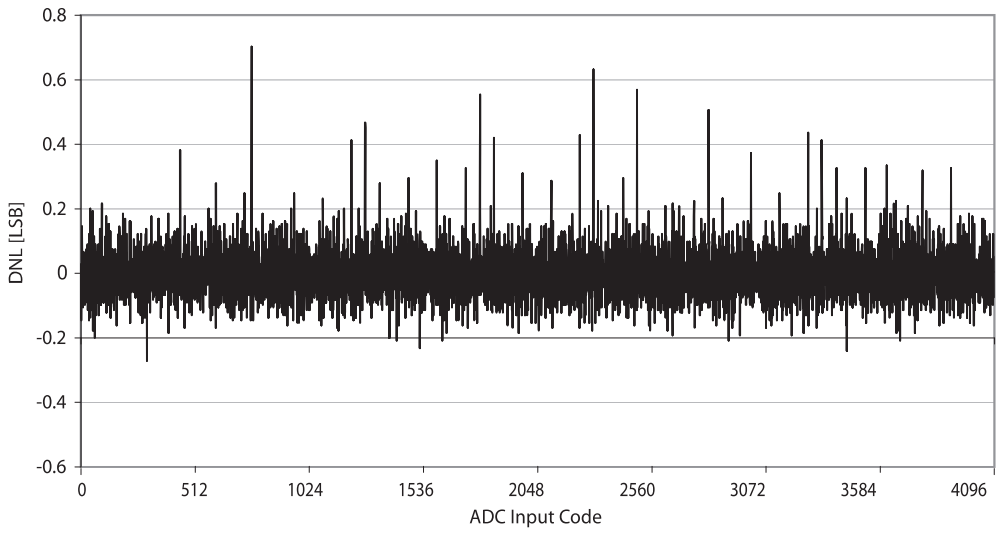


Figure 37-290. Gain error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

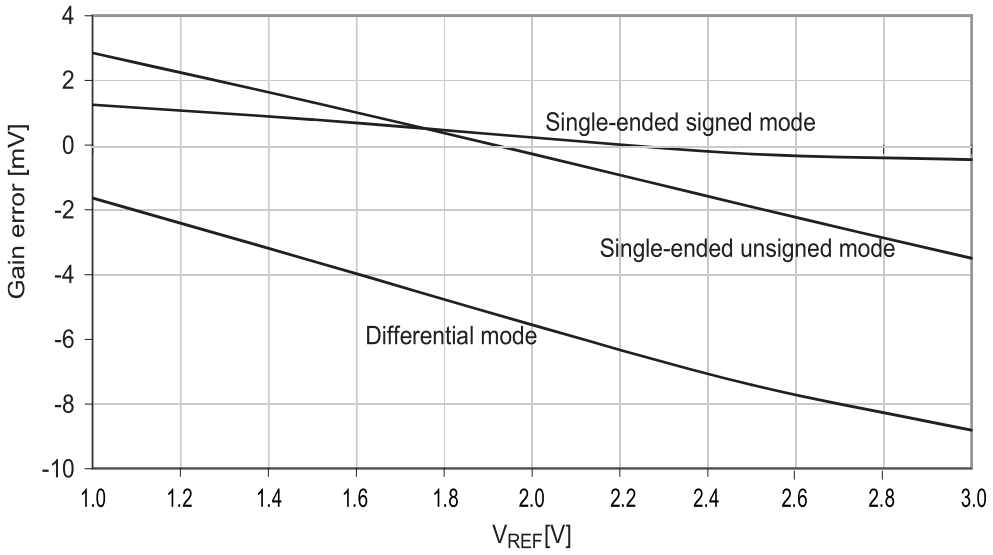


Figure 37-291. Gain error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

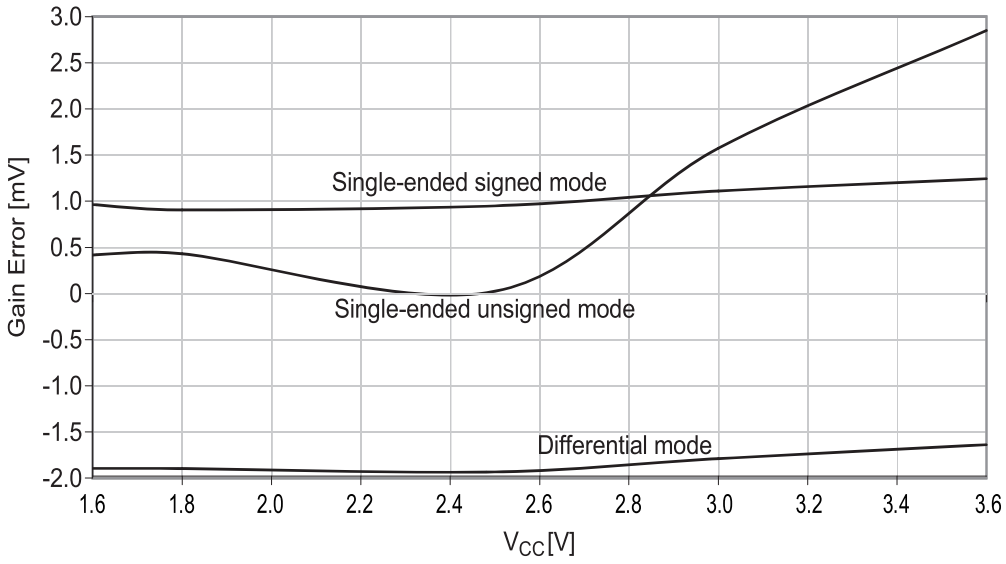


Figure 37-292. Offset error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

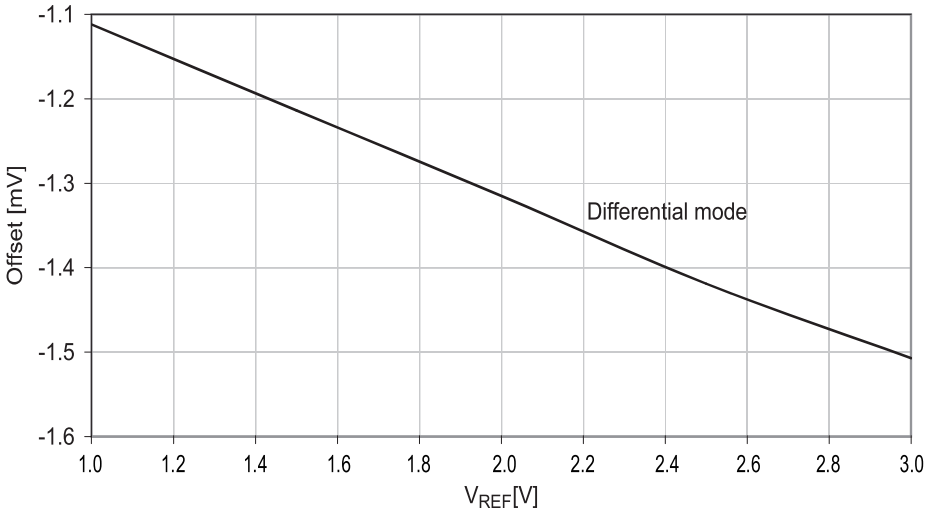


Figure 37-293. Gain error vs. temperature.

V_{CC} = 3.0V, V_{REF} = external 2.0V.

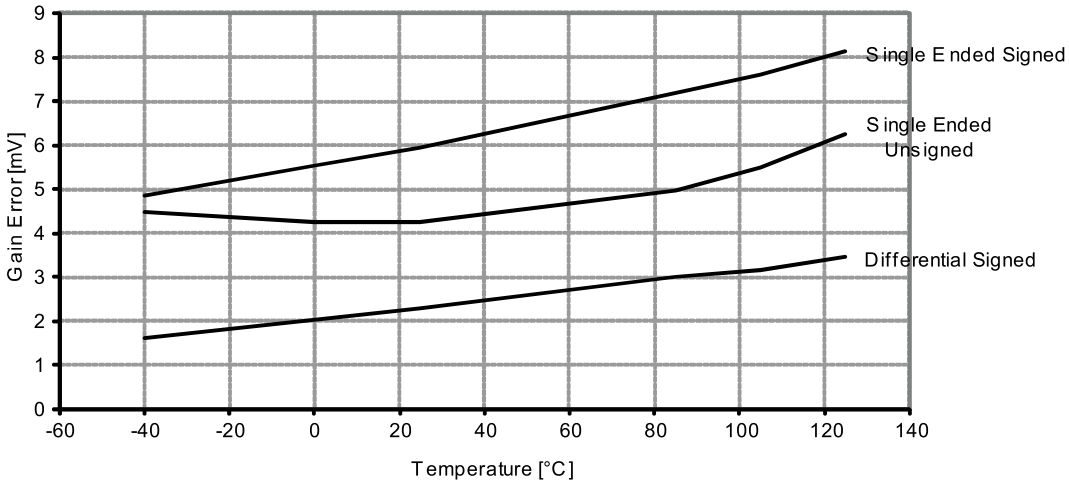


Figure 37-294. Offset error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

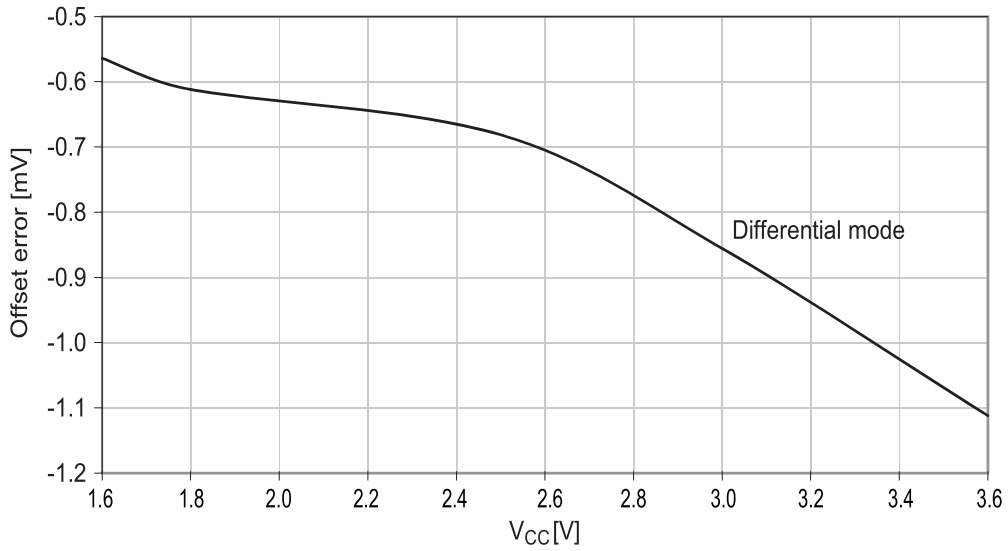


Figure 37-295. Noise vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

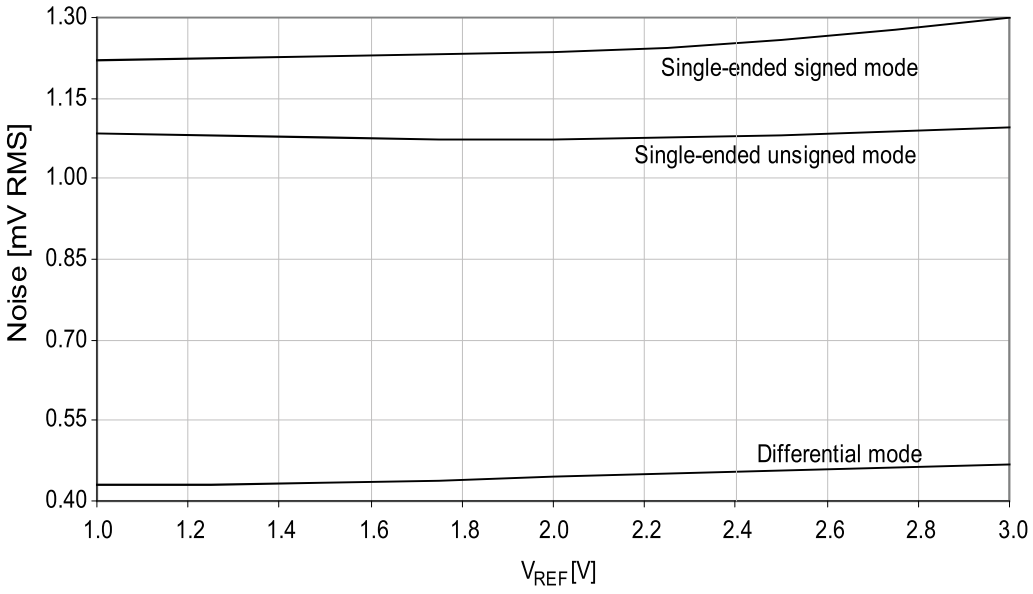
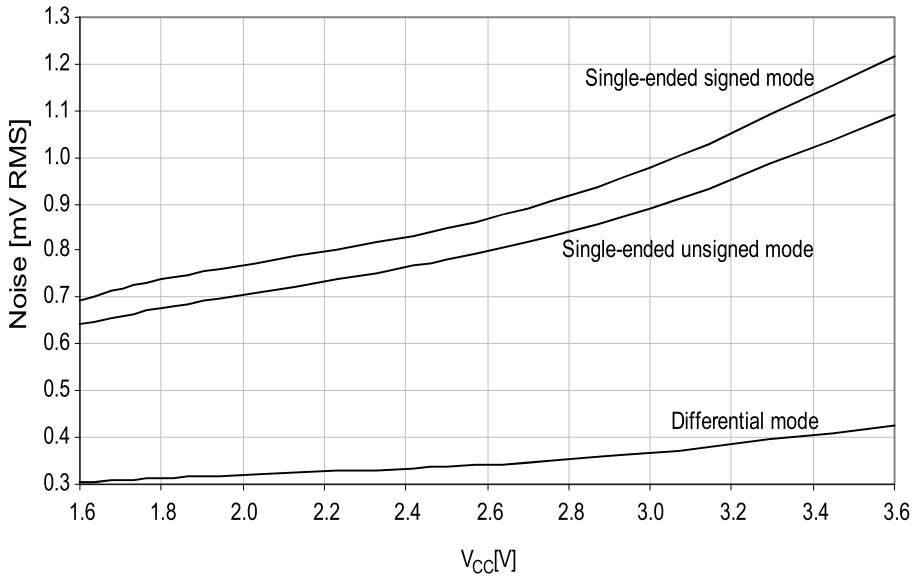


Figure 37-296. Noise vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.



37.4.4 DAC Characteristics

Figure 37-297. DAC INL error vs. V_{REF}.

V_{CC} = 3.6V.

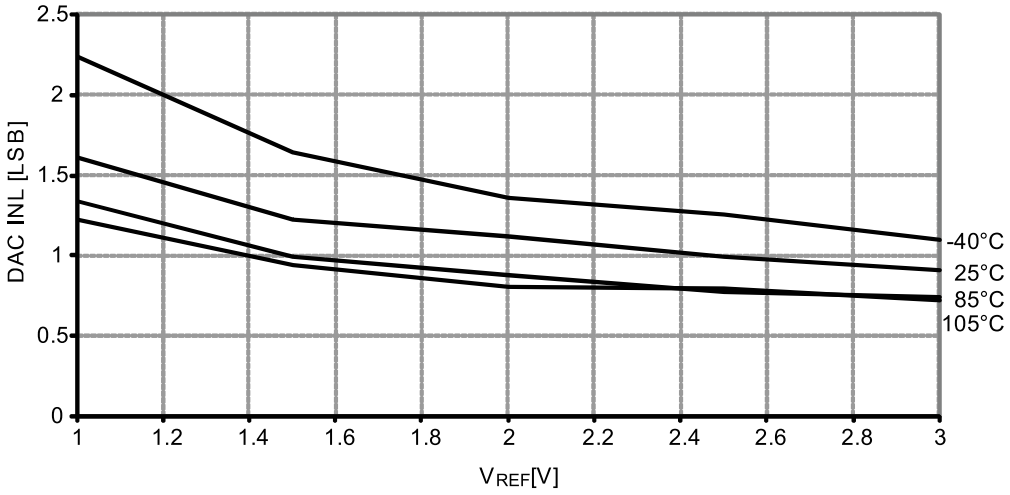


Figure 37-298. DNL error vs. V_{REF}.

$T = 25°C$, $V_{CC} = 3.6V$.

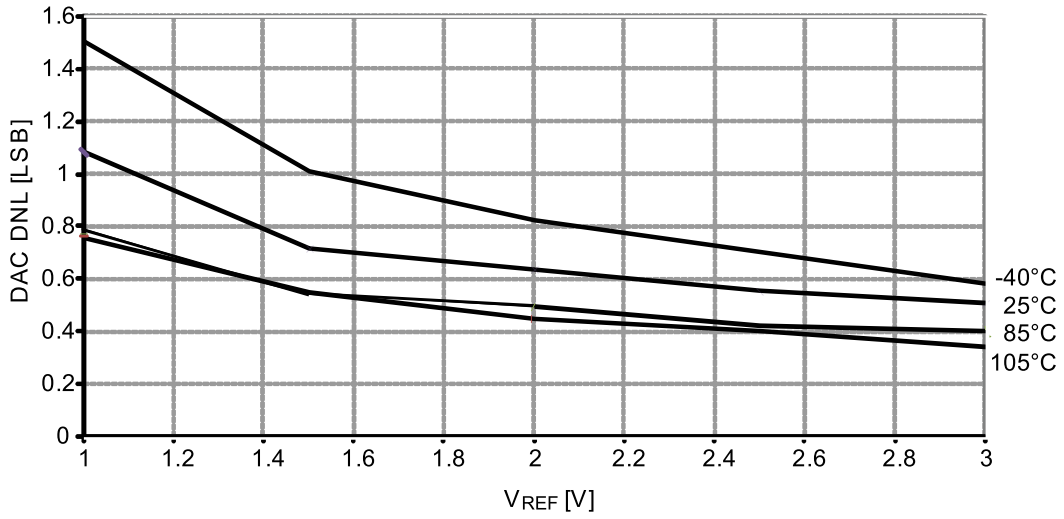
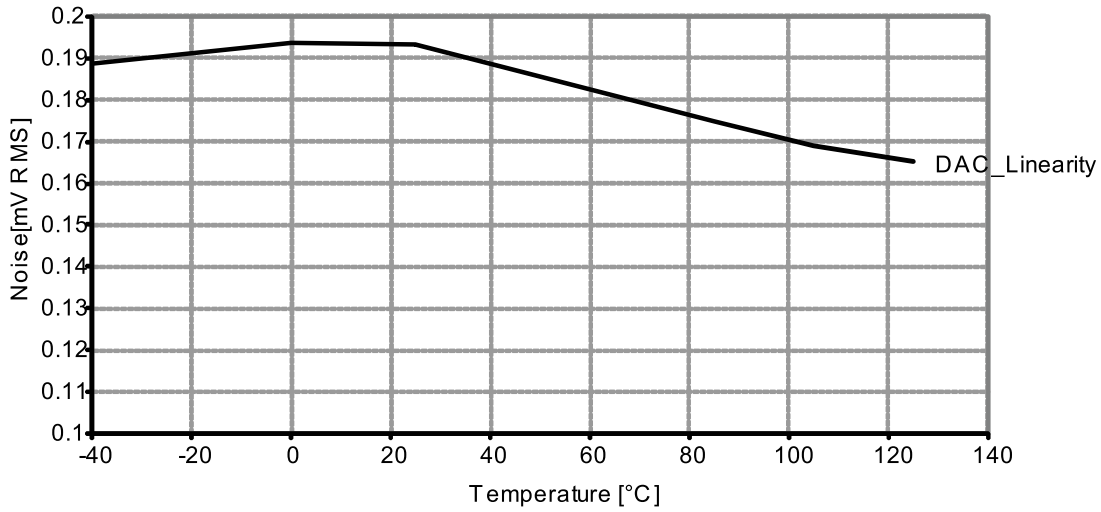


Figure 37-299. DAC noise vs. temperature.

$V_{CC} = 3.0V$, $V_{REF} = 2.4V$.



37.4.5 Analog Comparator Characteristics

Figure 37-300. Analog comparator hysteresis vs. V_{CC}

High-speed, small hysteresis.

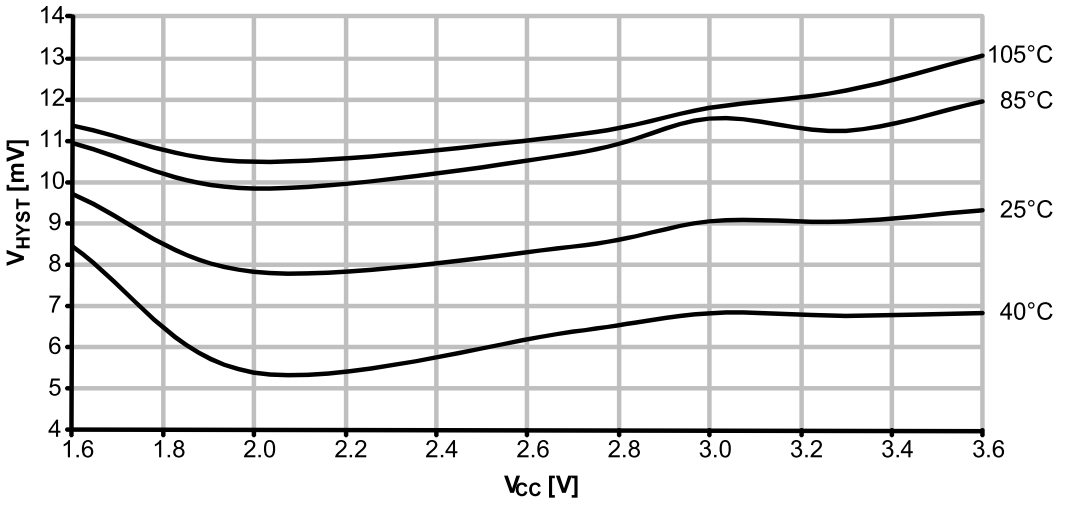


Figure 37-301. Analog comparator hysteresis vs. V_{CC}

Low power, small hysteresis.

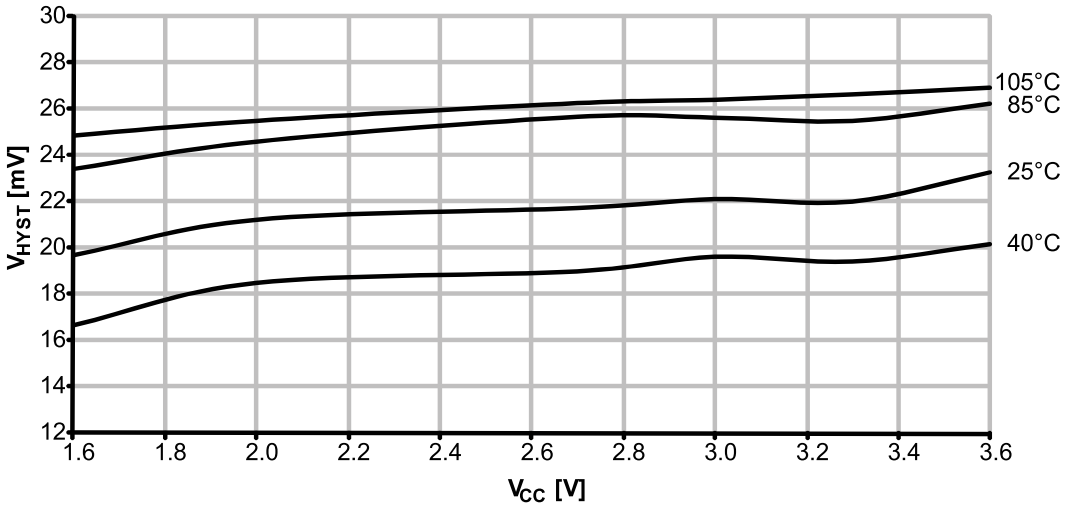


Figure 37-302. Analog comparator hysteresis vs. V_{CC}.

High-speed mode, large hysteresis.

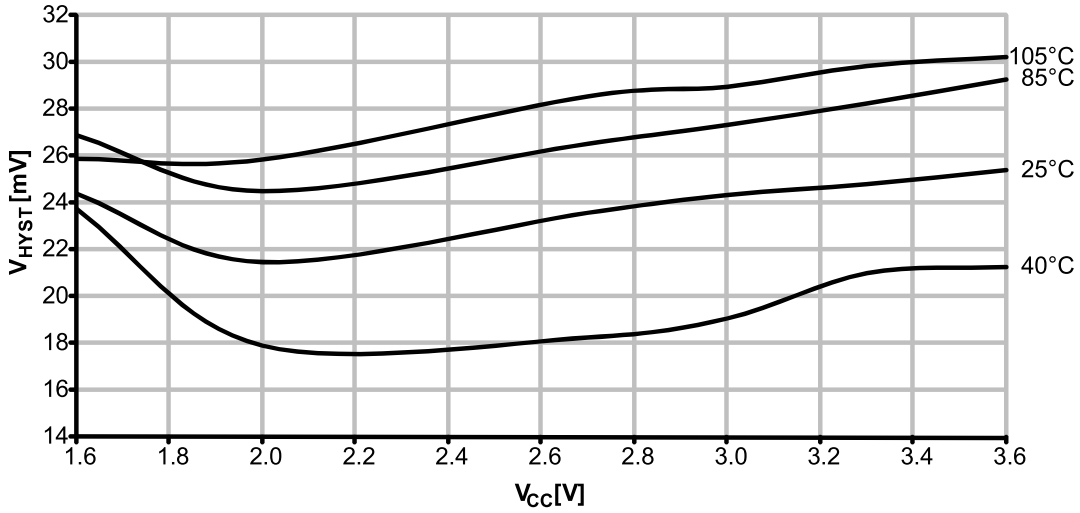


Figure 37-303. Analog comparator hysteresis vs. V_{CC}.

Low power, large hysteresis.

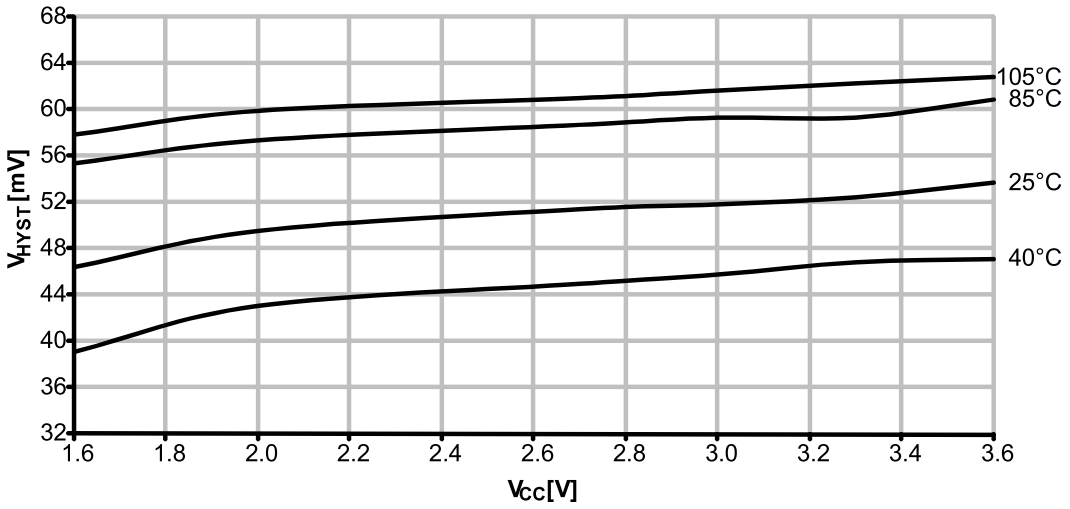


Figure 37-304. Analog comparator current source vs. calibration value.

Temperature = 25°C.

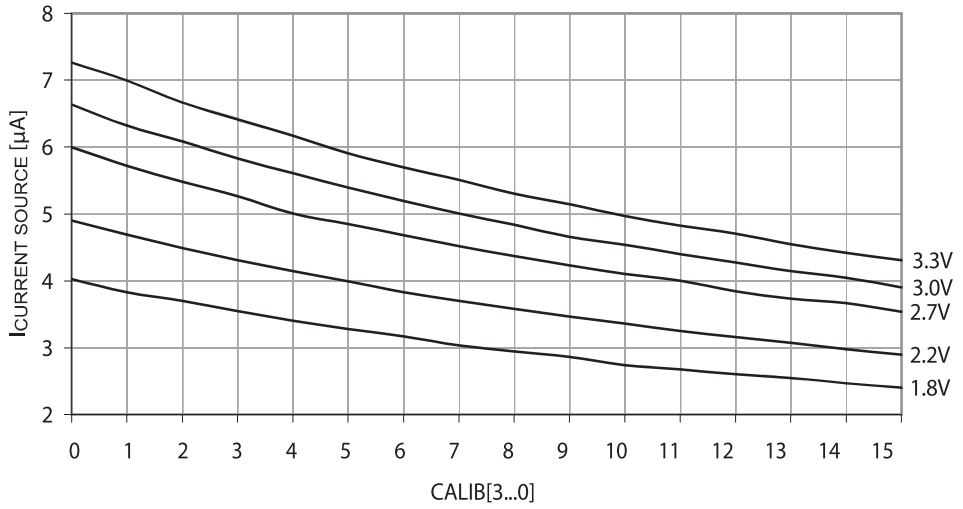


Figure 37-305. Analog comparator current source vs. calibration value.

V_{CC} = 3.0V.

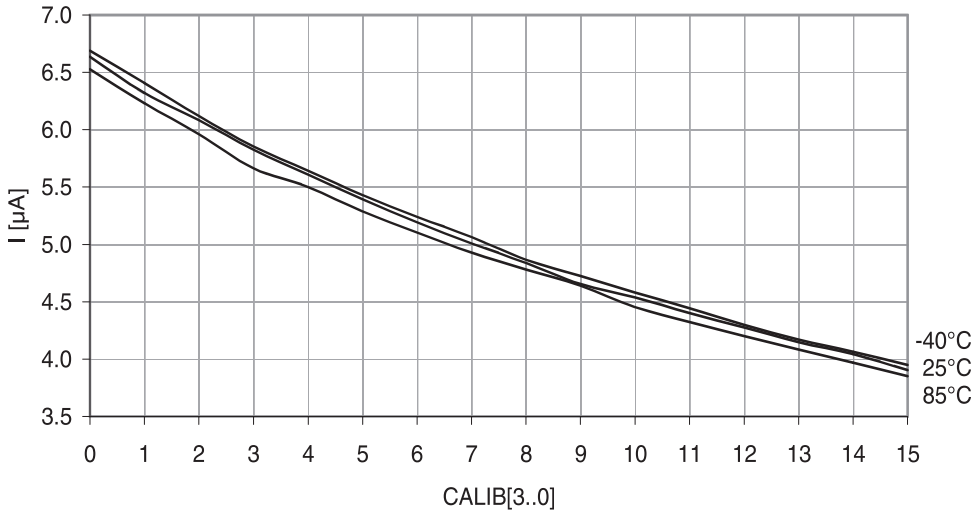
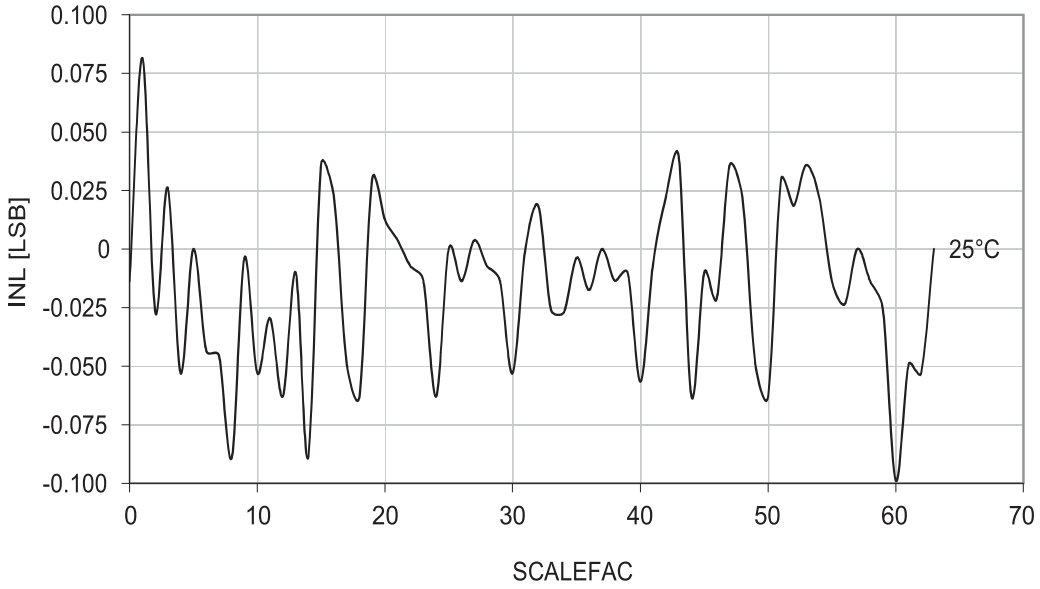


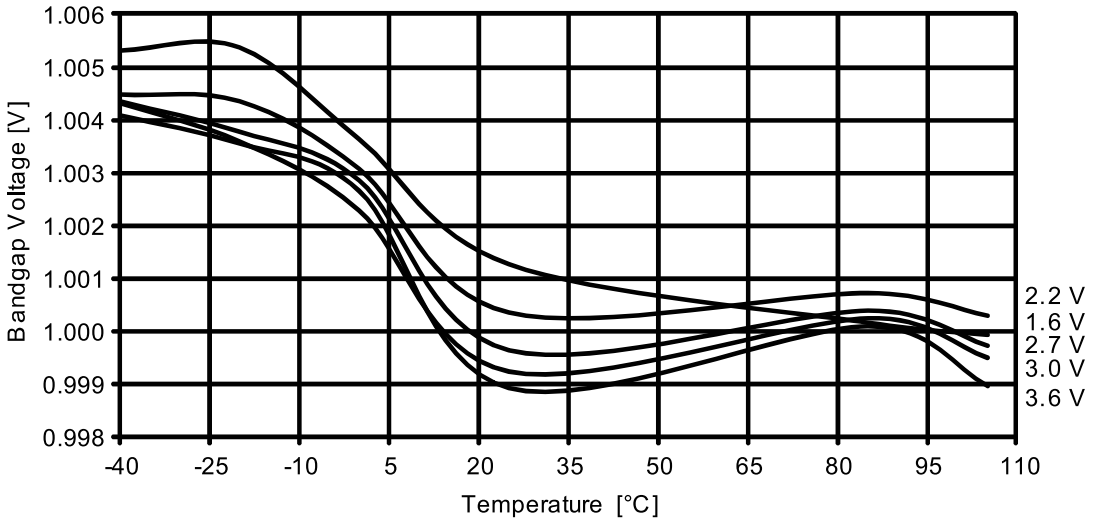
Figure 37-306. Voltage scaler INL vs. SCALEFAC.

T = 25°C, V_{CC} = 3.0V.



37.4.6 Internal 1.0V reference Characteristics

Figure 37-307. ADC/DAC Internal 1.0V reference vs. temperature



37.4.7 BOD Characteristics

Figure 37-308. BOD thresholds vs. temperature.
BOD level = 1.6V.

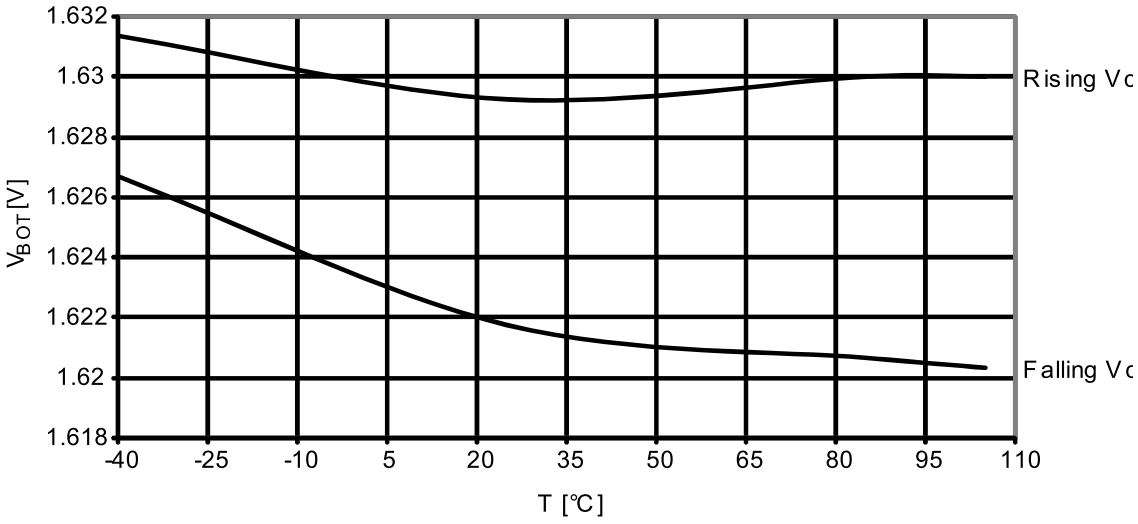
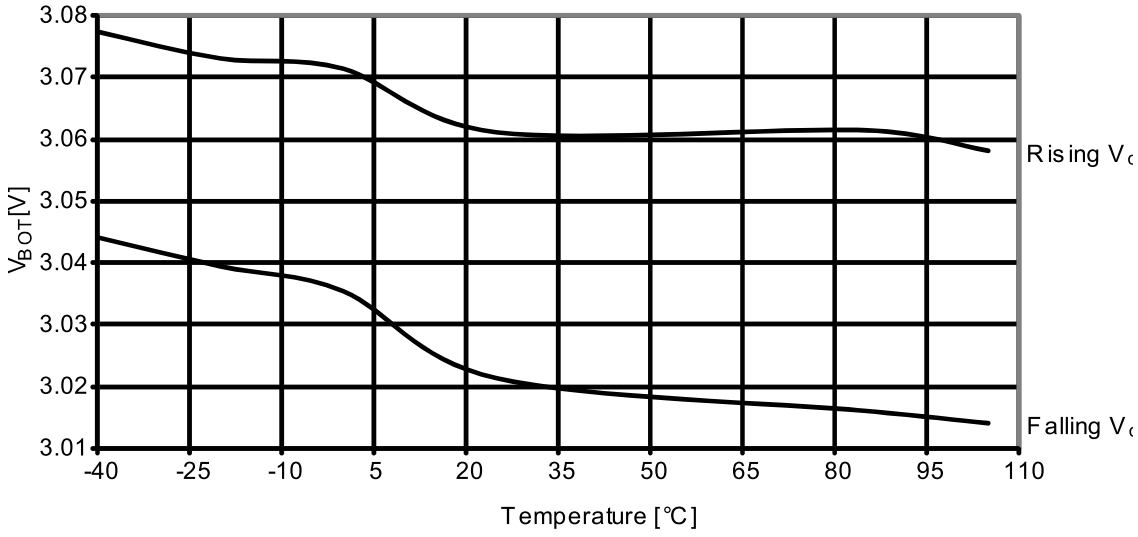


Figure 37-309. BOD thresholds vs. temperature.
BOD level = 3.0V.



37.4.8 External Reset Characteristics

Figure 37-310. Minimum Reset pin pulse width vs. V_{CC}.

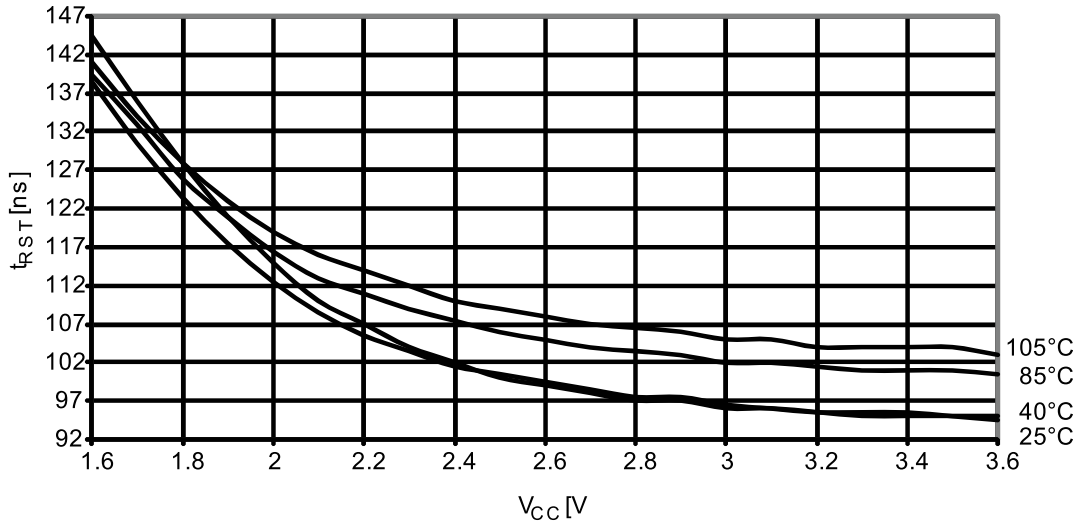


Figure 37-311. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 1.8V.

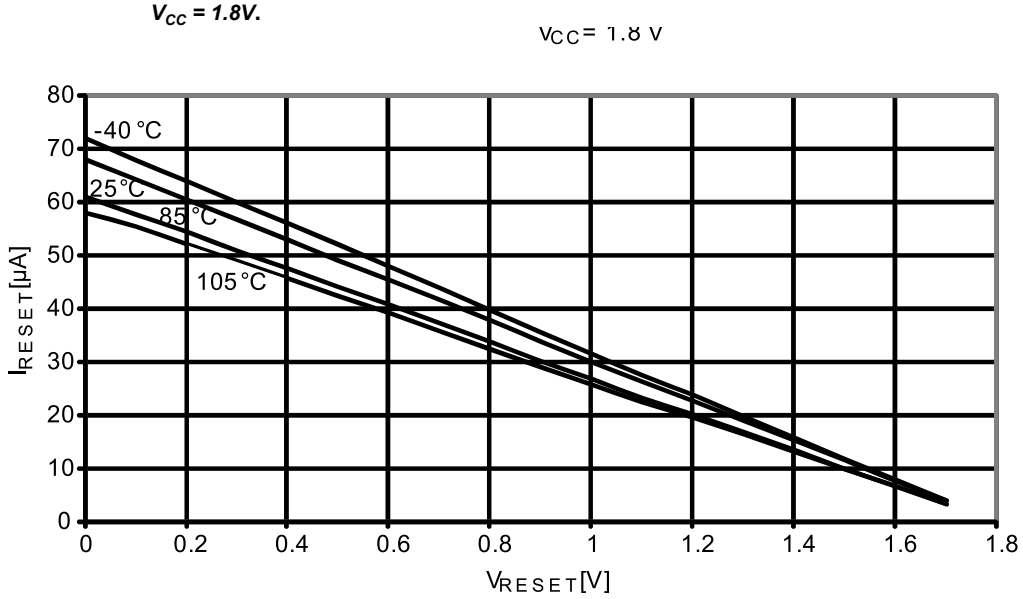


Figure 37-312. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.0V.

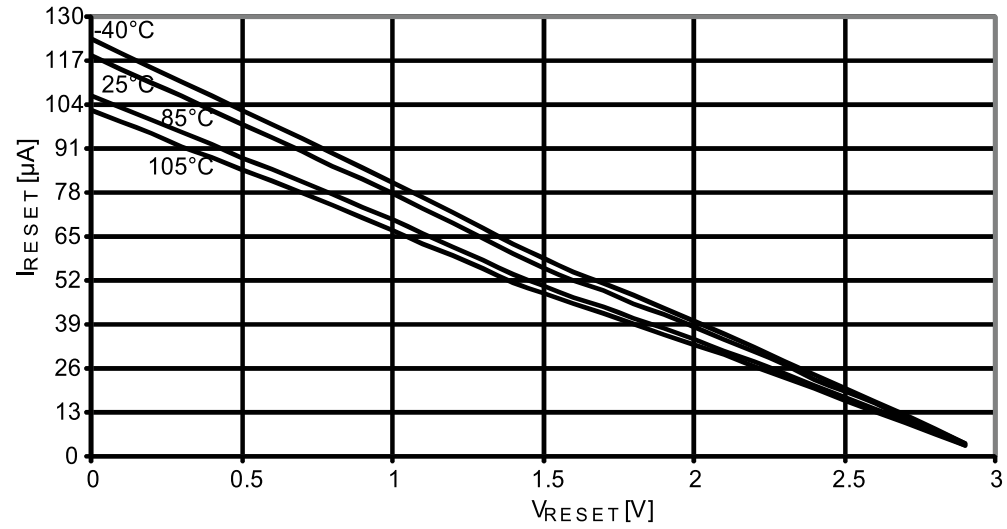


Figure 37-313. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.3V.

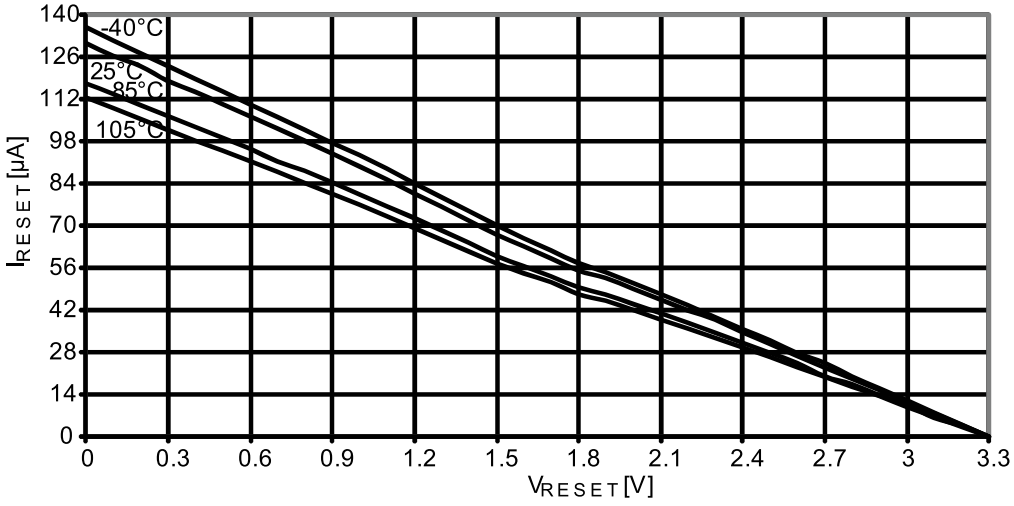


Figure 37-314. Reset pin input threshold voltage vs. V_{CC}.

V_{IH} - Reset pin read as "1".

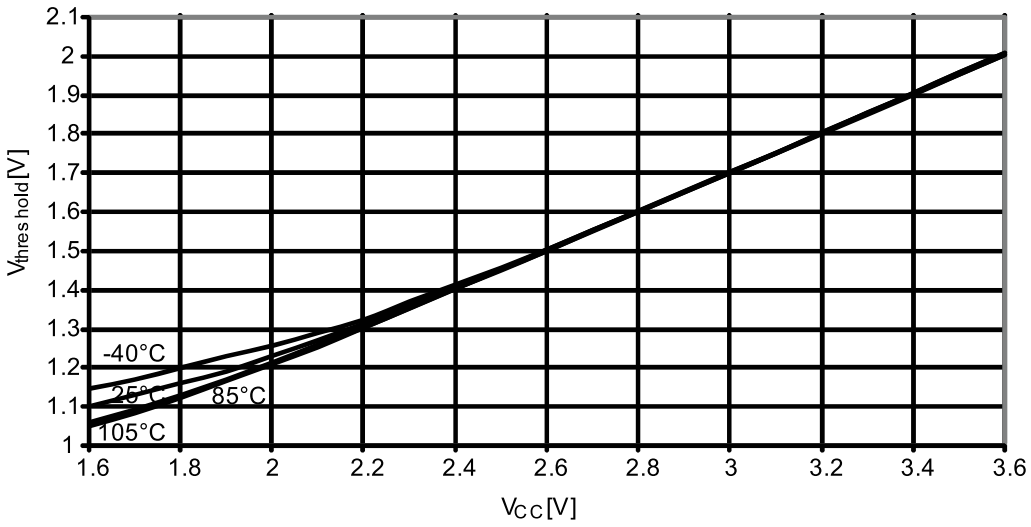
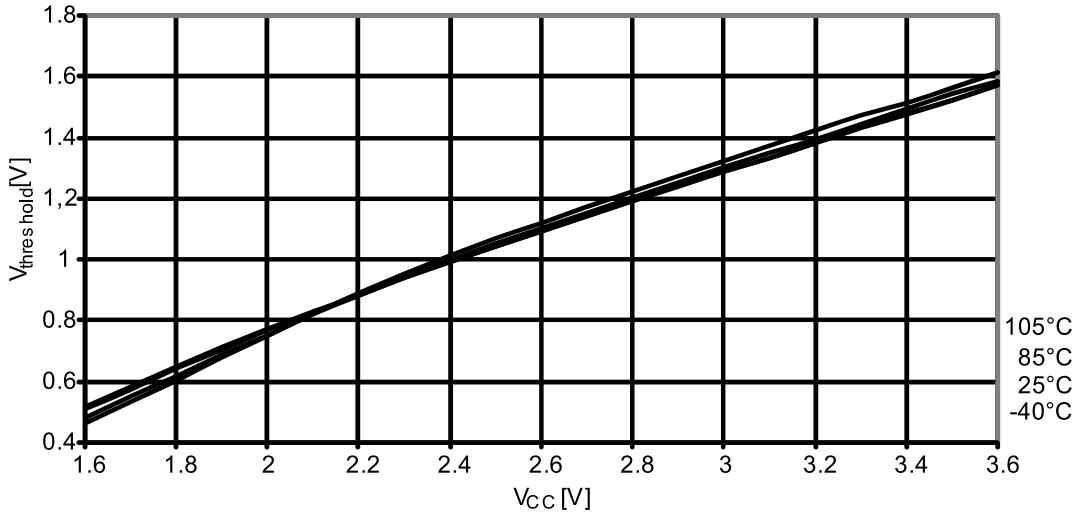


Figure 37-315. Reset pin input threshold voltage vs. V_{CC}.

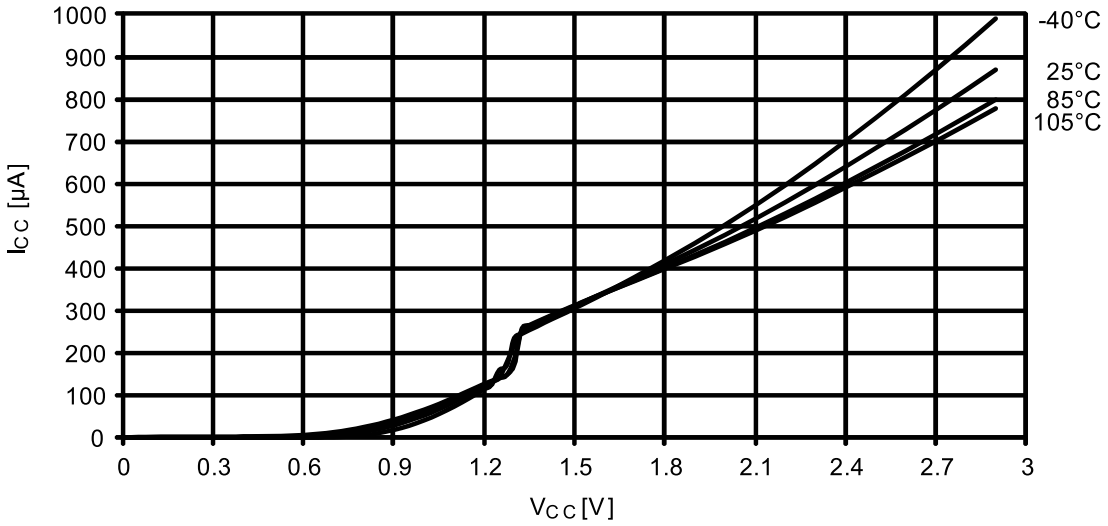
V_{IL} - Reset pin read as "0".



37.4.9 Power-on Reset Characteristics

Figure 37-316. Power-on reset current consumption vs. V_{CC}.

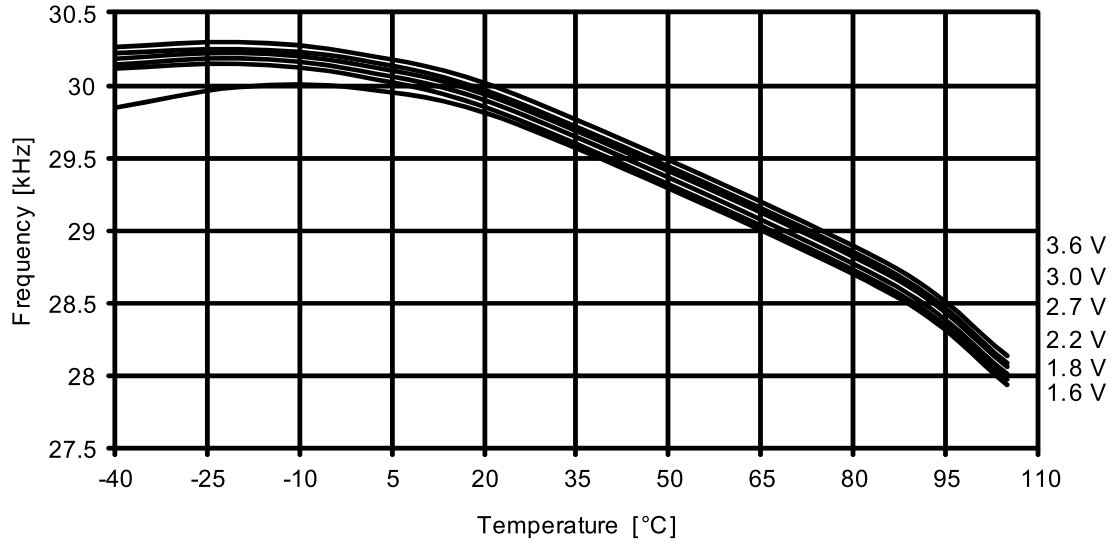
BOD level = 3.0V, enabled in continuous mode.



37.4.10 Oscillator Characteristics

37.4.10.1 Ultra Low-Power internal oscillator

Figure 37-317. Ultra Low-Power internal oscillator frequency vs. temperature.



37.4.10.2 32.768kHz Internal Oscillator

Figure 37-318. 32.768kHz internal oscillator frequency vs. temperature.

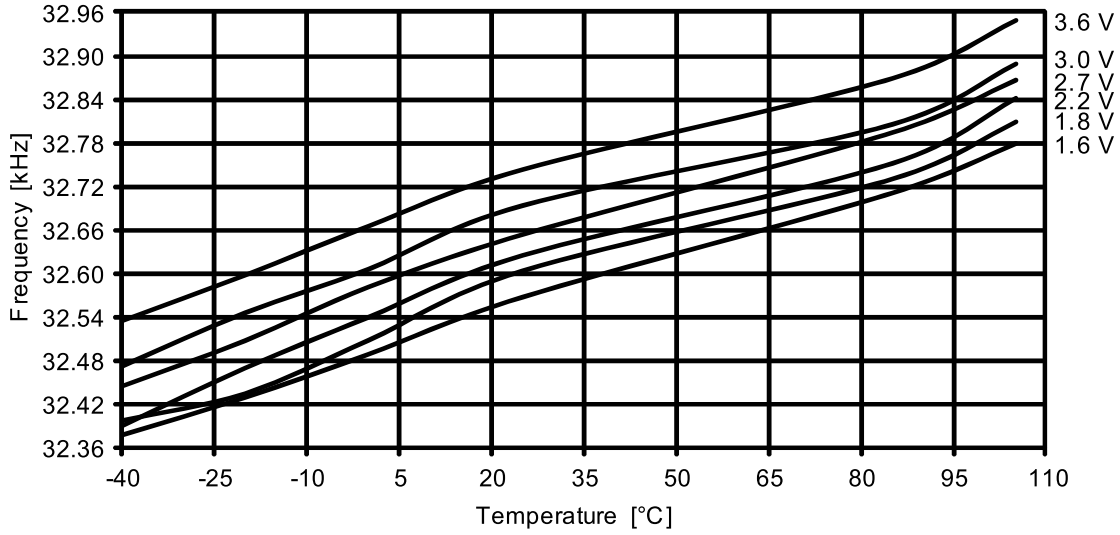
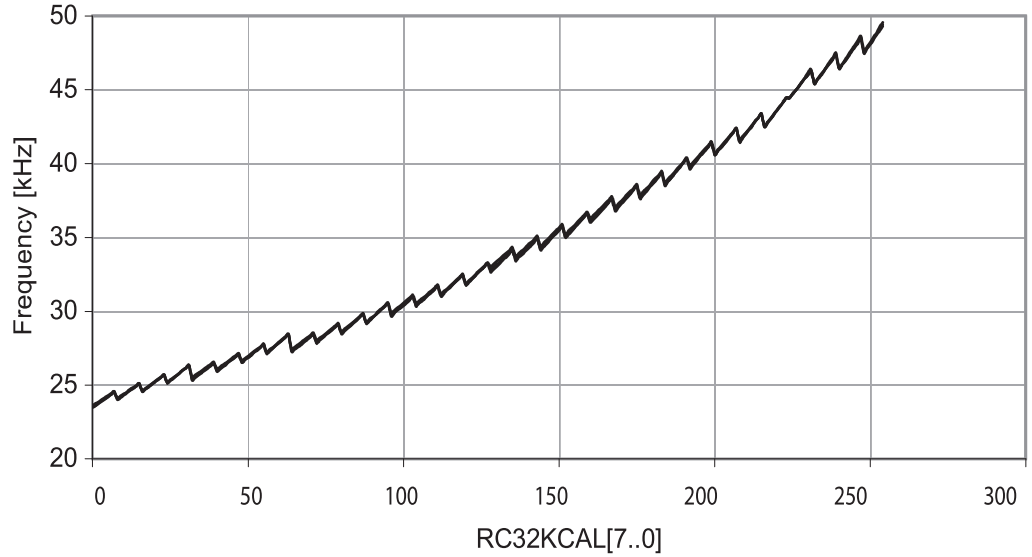


Figure 37-319. 32.768kHz internal oscillator frequency vs. calibration value.

V_{CC} = 3.0V, T = 25°C.



37.4.10.3 2MHz Internal Oscillator

Figure 37-320. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

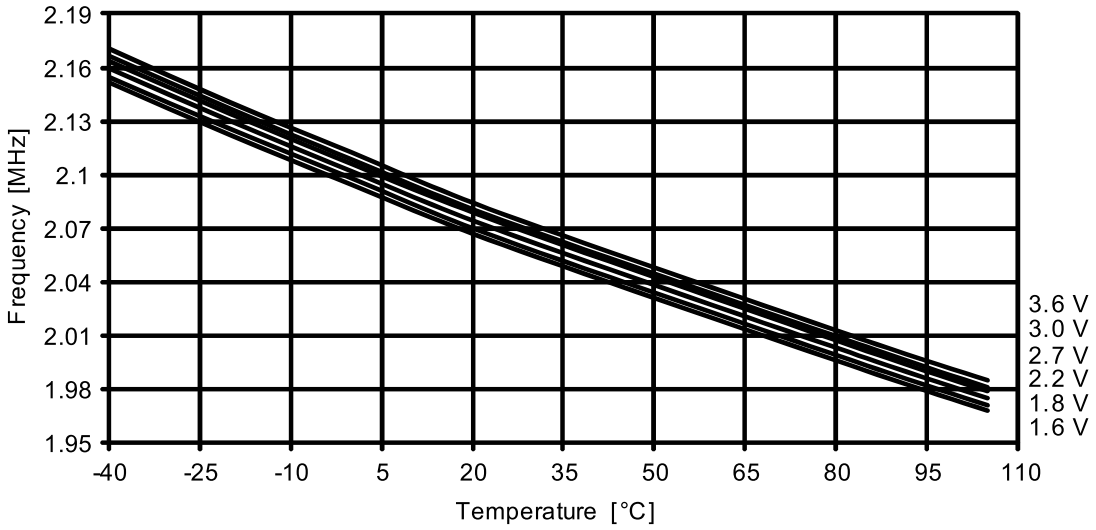


Figure 37-321. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.

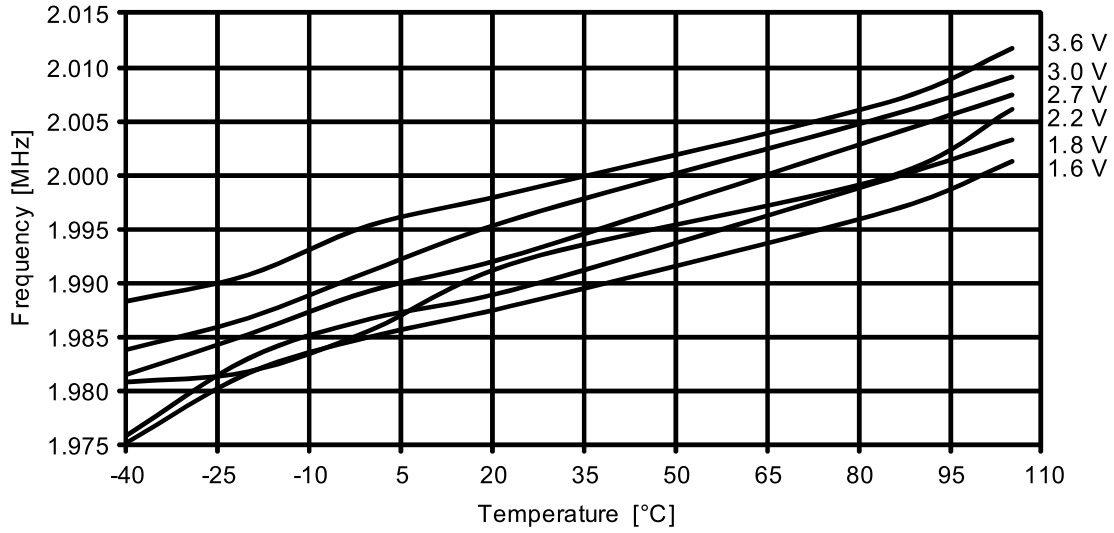
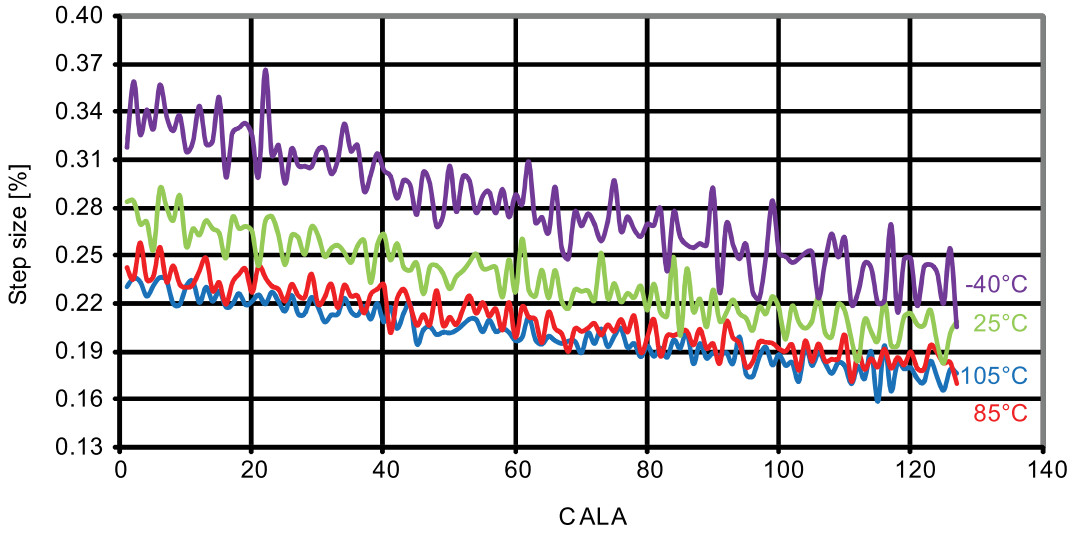


Figure 37-322. 2MHz internal oscillator CALA calibration step size.

V_{CC} = 3V.



37.4.10.4 32MHz Internal Oscillator

Figure 37-323. 32MHz internal oscillator frequency vs. temperature.
DFLL disabled.

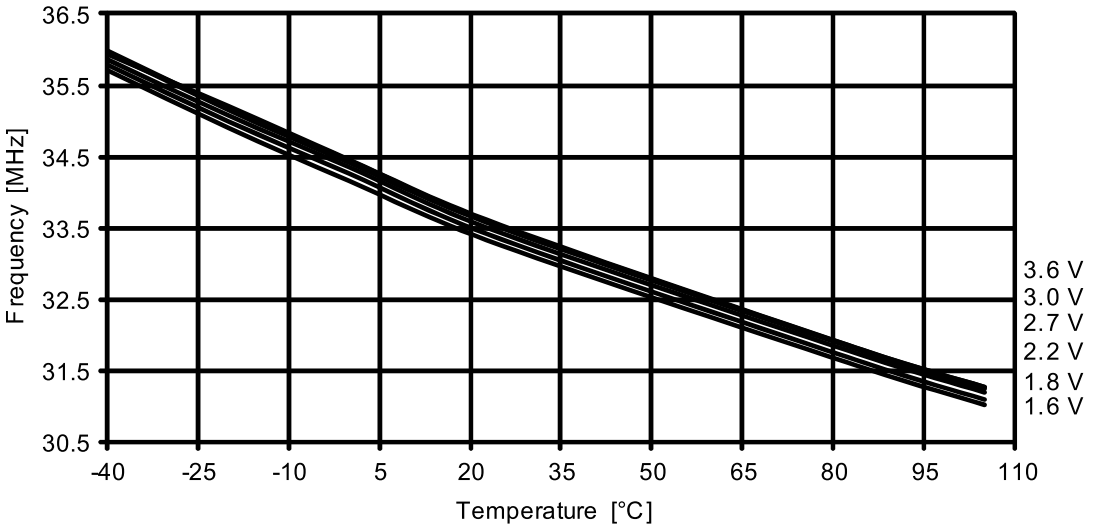


Figure 37-324. 32MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.

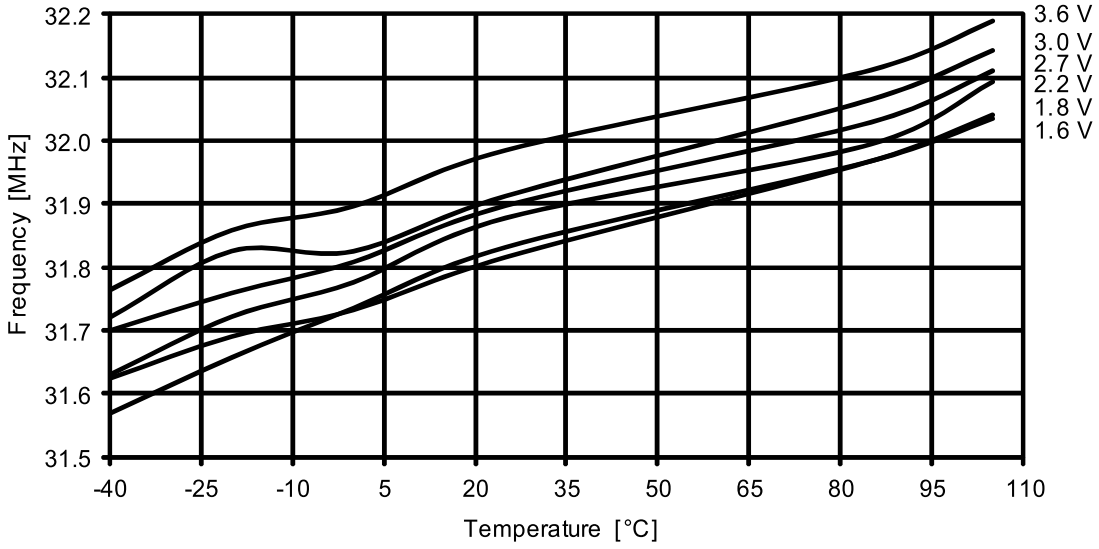


Figure 37-325. 32MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.

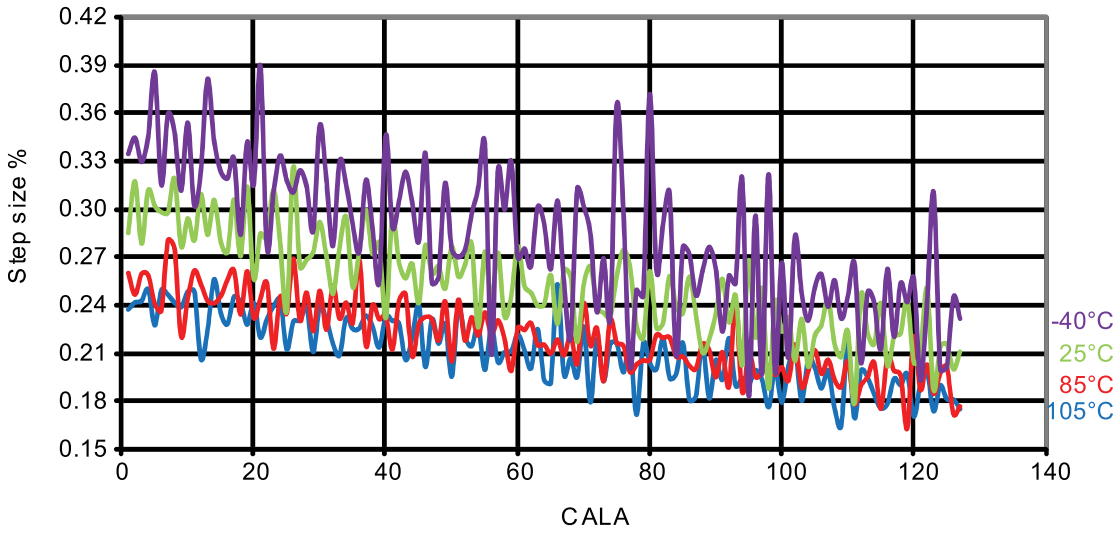
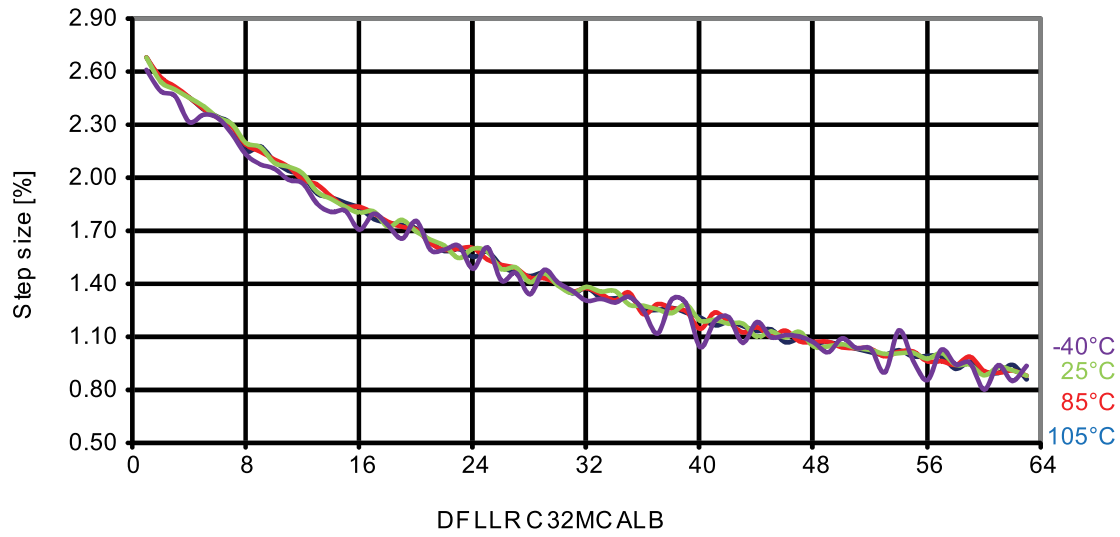


Figure 37-326. 32MHz internal oscillator frequency vs. CALB calibration value.

V_{CC} = 3.0V.



37.4.10.5 32MHz internal oscillator calibrated to 48MHz

Figure 37-327. 48MHz internal oscillator frequency vs. temperature.
DFLL disabled.

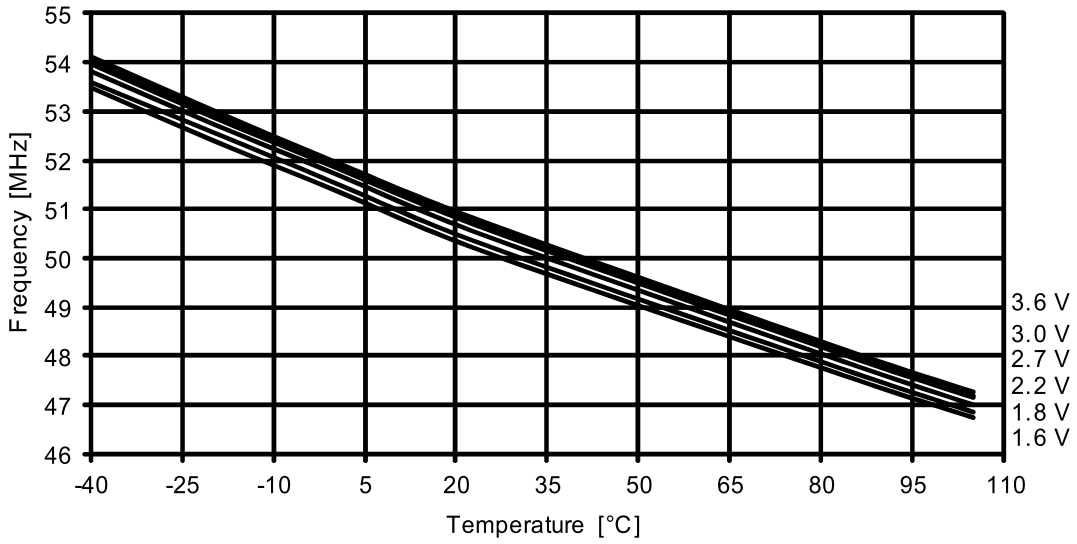


Figure 37-328. 48MHz internal oscillator frequency vs. temperature.
DFLL enabled, from the 32.768kHz internal oscillator.

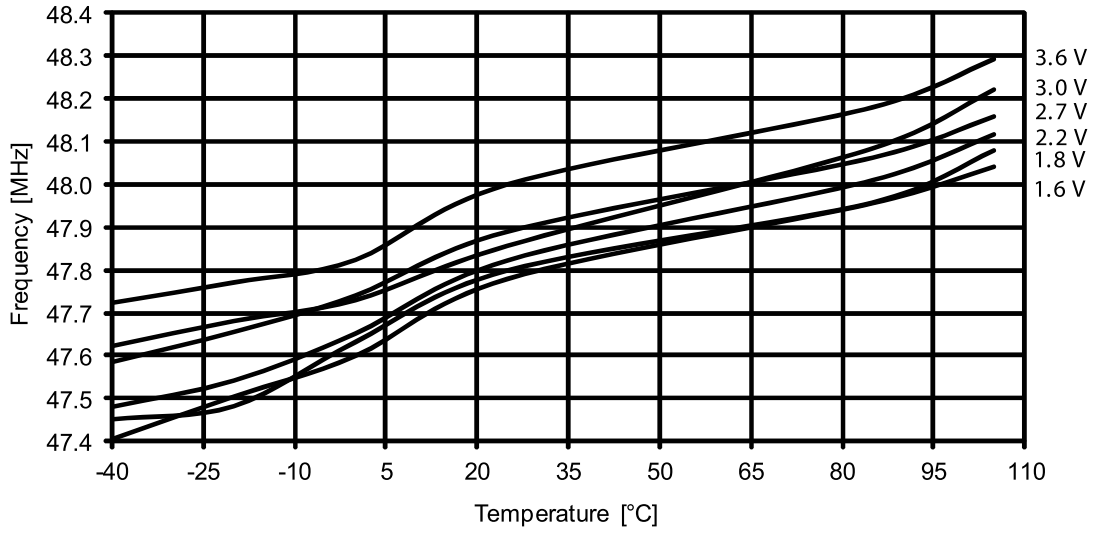
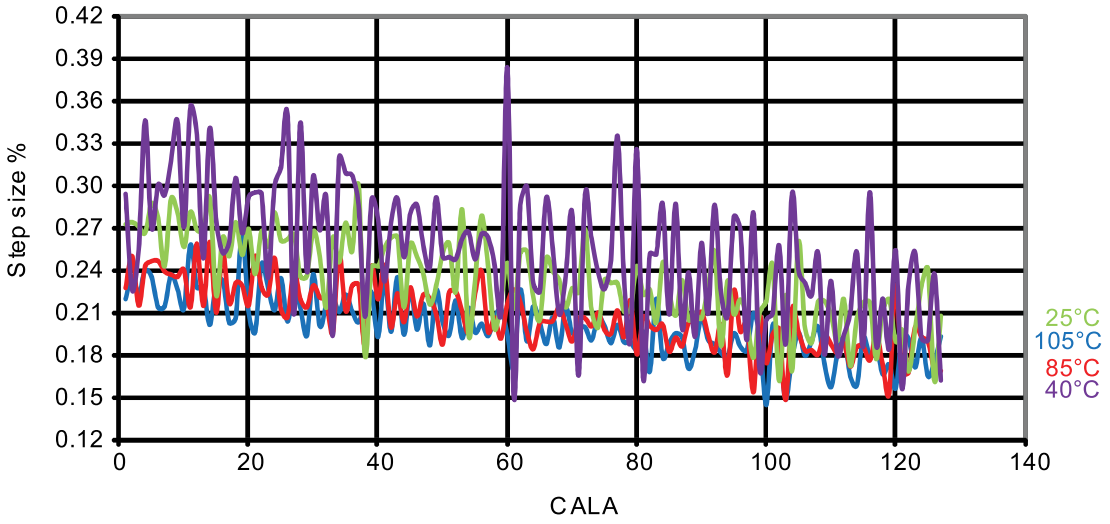


Figure 37-329. 48MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.



37.4.11 Two-Wire Interface characteristics

Figure 37-330. SDA hold time vs. V_{CC}.

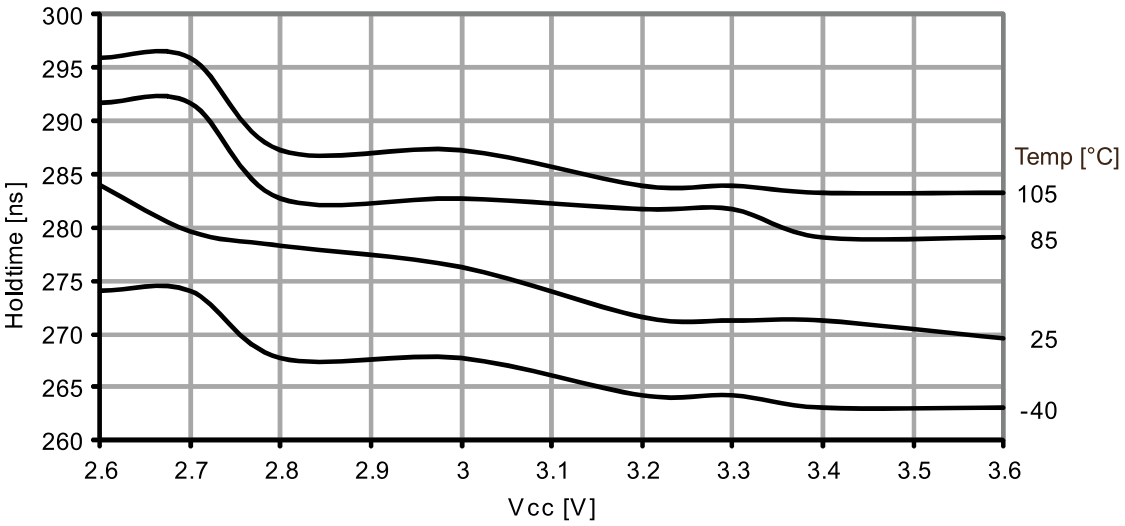
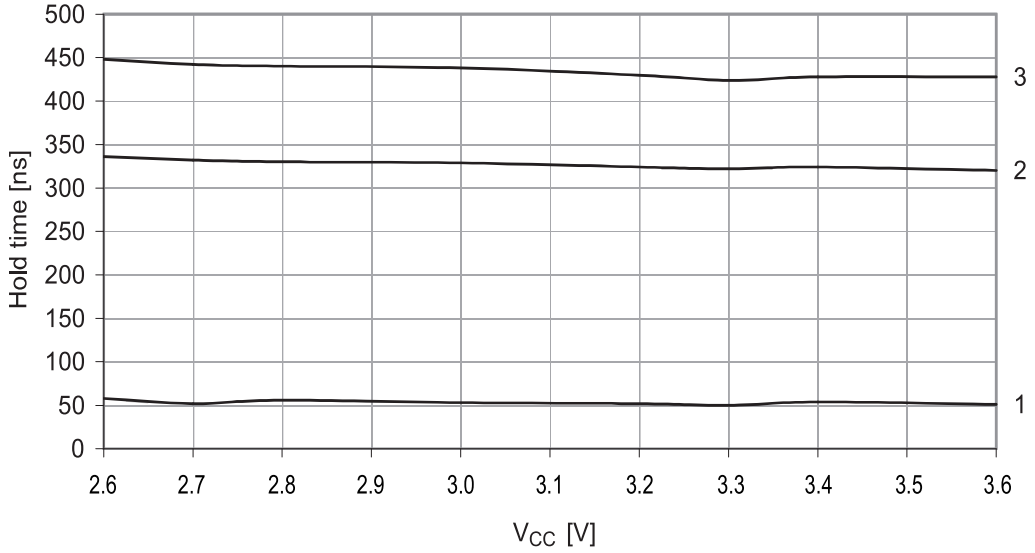
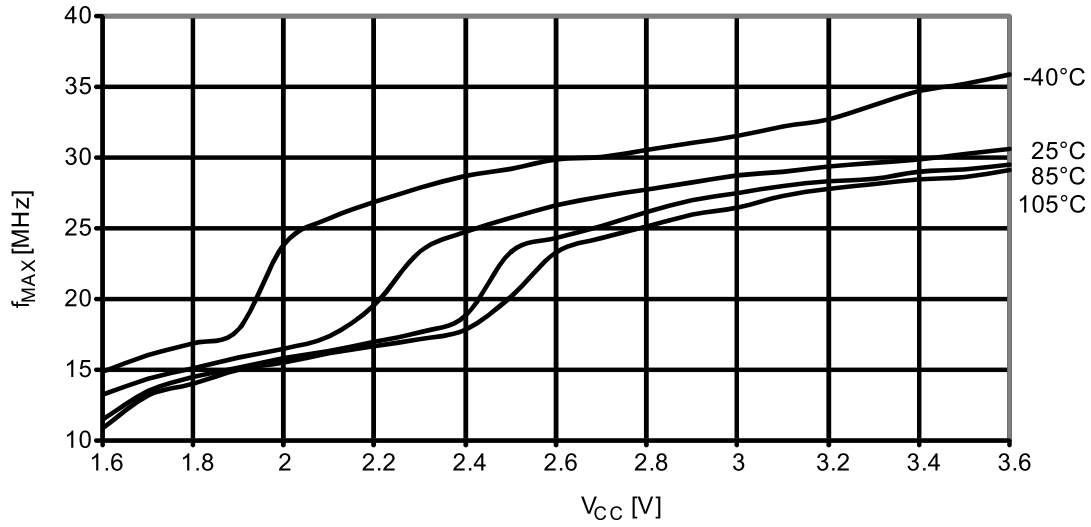


Figure 37-331. SDA hold time vs. supply voltage.



37.4.12 PDI characteristics

Figure 37-332. Maximum PDI frequency vs. V_{CC}.



38. Errata

38.1 ATxmega64A3U, ATxmega128A3U, ATxmega192A3U, ATxmega256A3U

38.1.1 Rev. G

- The DAC Channel 1 has not been calibrated in the Xmega devices released prior to April 2012.
- AWeX fault protection restore is not done correct in Pattern Generation Mode.

1. **AWeX fault protection restore is not done correct in Pattern Generation Mode**
   When a fault is detected the OUTOVEN register is cleared, and when fault condition is cleared, OUTOVEN is restored according to the corresponding enabled DTI channels. For Common Waveform Channel Mode (CWCM), this has no effect as the OUTOVEN is correct after restoring from fault. For Pattern Generation Mode (PGM), OUTOVEN should instead have been restored according to the DTLSBUF register.

   Problem fix/Workaround
   Problem fix/Workaround

   For CWCM no workaround is required.

   For PGM in latched mode, disable the DTI channels before returning from the fault condition. Then, set correct OUTOVEN value and enable the DTI channels, before the direction (DIR) register is written to enable the correct outputs again.

   For PGM in cycle-by-cycle mode there is no workaround.

38.1.2 Rev. A-F

Not sampled.

39. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

39.1 8386E – 09/2014

1.	Updated "Ordering Information" on page 3: – Added Ordering information for ATxmega64A3U/128a3U/192A3U/256A3U @ 105°C
	– Updated "Electrical Characteristics" on page 73 and onwards concerning "Power Consumption" and "Endurance and data retention" for ATxmega64A3U/128a3U/192A3U/256A3U @ 105°C
2.	– Updated "Typical Characteristics" on page 161 and onwards for ATxmega64A3U/128a3U/192A3U/256A3U @ 105°C
3.	– Corrected values for Active Current Consumption for 192A3U in Table 36-68 on page 119 and for 256A3U in Table 36-100 on page 141.
4	– Updated plots for Active supply current for 192A3U in Figure 37-167 on page 245 and Figure 37-168 on page 245
5	– Updated plots for Active supply current for 256A3U in Figure 37-251 on page 287 and Figure 37-252 on page 288
6.	– Corrected values for Bootloader start and end address for 128A3U in Table 7-1 on page 14.
7.	– Changed Vcc to AVcc in Section 28. "ADC – 12-bit Analog to Digital Converter" on page 52and in Section 30.1 "Features" on page 56.
8.	– Changed unit notation for parameter $t_{SU;DAT}$ to ns in Table 36-32 on page 93, Table 36-64 on page 115, Table 36-96 on page 137 and Table 36-128 on page 159.
9.	– Added information in Section 38. "Errata" on page 329 on missing calibration of DAC channel 1.

39.2 8386D – 03/2014

1.	Updated "Port A - alternate functions." on page 61: – Removed ACDP POS from the Table 32-1 on page 61
2.	Updated "Port B - alternate functions." on page 61: – ACDB POS changed to ADCB POS/GAINPOS in the Table 32-2 on page 61

39.3 8386C – 02/2013

1.	Updated the datasheet using the Atmel new datasheet template.
2.	Added column for TWI with external driver interface for Port C and E in "Alternate Pin Functions" on page 61.
3.	Removed TWID from Port D and updated pin numbers in"Alternate Pin Functions" on page 61.
4.	Added TOSC and removed AWEXE to/from Port E in "Alternate Pin Functions" on page 61.
5.	Added notes to table for Port D and E in "Alternate Pin Functions" on page 61.

6.	Updated pin numbers for Port D and F in “Alternate Pin Functions” on page 61.
7.	Removed AWEXE from the peripheral module address map in Table 33-1 on page 64.
8.	Updated the “Electrical Characteristics” on page 73 by separating the characteristics for each device.
9.	Updated DAC clock and timing characteristics for all memory: ATxmega64A3U: Table 36-13 on page 81. ATxmega128A3U: Table 36-45 on page 103. ATxmega192A3U: Table 36-77 on page 125. ATxmega256A3U: Table 36-109 on page 147.
10.	Added ESR parameter to External 16MHz crystal oscillator and XOSC characteristics: ATxmega64A3U: Table 36-29 on page 88. ATxmega128A3U: Table 36-61 on page 110 ATxmega192A3U: Table 36-93 on page 132 ATxmega256A3U: Table 36-125 on page 154
11.	Updated the “Typical Characteristics” on page 161 by separating the characteristics for each device.
12.	Added “Electrical Characteristics” and “Typical Characteristics” for both ATxmega64A3U and ATxmega128A3U.

39.4 8386B – 12/2011

1.	Updated the Figure 2-1 on page 5. JTAG written in the white color.
2.	Updated “Overview” on page 13.
3.	Updated Figure 30-1 on page 57.
4.	Updated “Cycle times for Data memory accesses assume internal memory accesses, and are not valid for accesses via the external RAM interface.” on page 70.
5.	Updated “Electrical Characteristics” on page 73.
6.	Updated “Typical Characteristics” on page 161.
7.	Several changes in “Typical Characteristics”

39.5 8386A – 07/2011

1.	Initial revision.

Table of Contents

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