

| 64 Pin | 128 Pin | 144 Pin | Pin Name  | Type | MFP   | Description                           |
|--------|---------|---------|-----------|------|-------|---------------------------------------|
|        |         |         |           |      |       | and digital circuit.                  |
|        | 77      | 85      | PG.9      | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |         |         | EBI_AD0   | I/O  | MFP2  | EBI address/data bus bit 0.           |
|        |         |         | SD1_DAT3  | I/O  | MFP3  | SD/SDIO1 data line bit 3.             |
|        |         |         | SPIM_D2   | I/O  | MFP4  | SPIM data 2 pin for Quad Mode I/O.    |
|        |         |         | BPWM0_CH5 | I/O  | MFP12 | BPWM0 channel 5 output/capture input. |
|        | 78      | 86      | PG.10     | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |         |         | EBI_AD1   | I/O  | MFP2  | EBI address/data bus bit 1.           |
|        |         |         | SD1_DAT2  | I/O  | MFP3  | SD/SDIO1 data line bit 2.             |
|        |         |         | SPIM_D3   | I/O  | MFP4  | SPIM data 3 pin for Quad Mode I/O.    |
|        |         |         | BPWM0_CH4 | I/O  | MFP12 | BPWM0 channel 4 output/capture input. |
|        | 79      | 87      | PG.11     | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |         |         | EBI_AD2   | I/O  | MFP2  | EBI address/data bus bit 2.           |
|        |         |         | SD1_DAT1  | I/O  | MFP3  | SD/SDIO1 data line bit 1.             |
|        |         |         | SPIM_SS   | I/O  | MFP4  | SPIM slave select pin.                |
|        |         |         | BPWM0_CH3 | I/O  | MFP12 | BPWM0 channel 3 output/capture input. |
|        | 80      | 88      | PG.12     | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |         |         | EBI_AD3   | I/O  | MFP2  | EBI address/data bus bit 3.           |
|        |         |         | SD1_DAT0  | I/O  | MFP3  | SD/SDIO1 data line bit 0.             |
|        |         |         | SPIM_CLK  | I/O  | MFP4  | SPIM serial clock pin.                |
|        |         |         | BPWM0_CH2 | I/O  | MFP12 | BPWM0 channel 2 output/capture input. |
|        | 81      | 89      | PG.13     | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |         |         | EBI_AD4   | I/O  | MFP2  | EBI address/data bus bit 4.           |
|        |         |         | SD1_CMD   | I/O  | MFP3  | SD/SDIO1 command/response pin         |
|        |         |         | SPIM_MISO | I/O  | MFP4  | SPIM MISO (Master In, Slave Out) pin. |
|        |         |         | BPWM0_CH1 | I/O  | MFP12 | BPWM0 channel 1 output/capture input. |
|        | 82      | 90      | PG.14     | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |         |         | EBI_AD5   | I/O  | MFP2  | EBI address/data bus bit 5.           |
|        |         |         | SD1_CLK   | O    | MFP3  | SD/SDIO1 clock output pin             |
|        |         |         | SPIM_MOSI | I/O  | MFP4  | SPIM MOSI (Master Out, Slave In) pin. |
|        |         |         | BPWM0_CH0 | I/O  | MFP12 | BPWM0 channel 0 output/capture input. |
|        | 83      | 91      | PG.15     | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |         |         | SD1_nCD   | I    | MFP3  | SD/SDIO1 card detect input pin        |
|        |         |         | CLKO      | O    | MFP14 | Clock Out                             |

| 64 Pin | 128 Pin | 144 Pin | Pin Name              | Type | MFP   | Description                                   |
|--------|---------|---------|-----------------------|------|-------|---|
|        |         |         | EADC0_ST              | I    | MFP15 | EADC0 external trigger input.                 |
|        |         | 92      | PD.3                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         |         | EBI_AD10              | I/O  | MFP2  | EBI address/data bus bit 10.                  |
|        |         |         | USCI0_CTL1            | I/O  | MFP3  | USCI0 control 1 pin.                          |
|        |         |         | SPI0_SS               | I/O  | MFP4  | SPI0 slave select pin.                        |
|        |         |         | UART3_nRTS            | O    | MFP5  | UART3 request to Send output pin.             |
|        |         |         | USCI1_CTL0            | I/O  | MFP6  | USCI1 control 0 pin.                          |
|        |         |         | SC2_PWR               | O    | MFP7  | Smart Card 2 power pin.                       |
|        |         |         | SC1_nCD               | I    | MFP8  | Smart Card 1 card detect pin.                 |
|        |         |         | UART0_TXD             | O    | MFP9  | UART0 data transmitter output pin.            |
|        |         | 93      | PD.2                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         |         | EBI_AD11              | I/O  | MFP2  | EBI address/data bus bit 11.                  |
|        |         |         | USCI0_DAT1            | I/O  | MFP3  | USCI0 data 1 pin.                             |
|        |         |         | SPI0_CLK              | I/O  | MFP4  | SPI0 serial clock pin.                        |
|        |         |         | UART3_nCTS            | I    | MFP5  | UART3 clear to Send input pin.                |
|        |         |         | SC2_RST               | O    | MFP7  | Smart Card 2 reset pin.                       |
|        |         |         | UART0_RXD             | I    | MFP9  | UART0 data receiver input pin.                |
|        |         | 94      | PD.1                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         |         | EBI_AD12              | I/O  | MFP2  | EBI address/data bus bit 12.                  |
|        |         |         | USCI0_DAT0            | I/O  | MFP3  | USCI0 data 0 pin.                             |
|        |         |         | SPI0_MISO             | I/O  | MFP4  | SPI0 MISO (Master In, Slave Out) pin.         |
|        |         |         | UART3_TXD             | O    | MFP5  | UART3 data transmitter output pin.            |
|        |         |         | I <sup>2</sup> C2_SCL | I/O  | MFP6  | I <sup>2</sup> C2 clock pin.                  |
|        |         |         | SC2_DAT               | I/O  | MFP7  | Smart Card 2 data pin.                        |
|        |         | 95      | PD.0                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         |         | EBI_AD13              | I/O  | MFP2  | EBI address/data bus bit 13.                  |
|        |         |         | USCI0_CLK             | I/O  | MFP3  | USCI0 clock pin.                              |
|        |         |         | SPI0_MOSI             | I/O  | MFP4  | SPI0 MOSI (Master Out, Slave In) pin.         |
|        |         |         | UART3_RXD             | I    | MFP5  | UART3 data receiver input pin.                |
|        |         |         | I <sup>2</sup> C2_SDA | I/O  | MFP6  | I <sup>2</sup> C2 data input/output pin.      |
|        |         |         | SC2_CLK               | O    | MFP7  | Smart Card 2 clock pin.                       |
|        |         |         | TM2                   | I/O  | MFP14 | Timer2 event counter input/toggle output pin. |
|        | 84      | 96      | PD.13                 | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         |         | EBI_AD10              | I/O  | MFP2  | EBI address/data bus bit 10.                  |

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|--------|---------|---------|------------------------|------|-------|---|
|        |         |         | SD0_nCD                | I    | MFP3  | SD/SDIO0 card detect input pin                |
|        |         |         | SPI0_I2SMCLK           | I/O  | MFP4  | SPI0 I <sup>2</sup> S master clock output pin |
|        |         |         | SPI1_I2SMCLK           | I/O  | MFP5  | SPI1 I <sup>2</sup> S master clock output pin |
|        |         |         | SC2_nCD                | I    | MFP7  | Smart Card 2 card detect pin.                 |
|        | 85      | 97      | PA.12                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         |         | I <sup>2</sup> S0_BCLK | O    | MFP2  | I <sup>2</sup> S0 bit clock output pin.       |
|        |         |         | UART4_TXD              | O    | MFP3  | UART4 data transmitter output pin.            |
|        |         |         | I <sup>2</sup> C1_SCL  | I/O  | MFP4  | I <sup>2</sup> C1 clock pin.                  |
|        |         |         | SPI2_SS                | I/O  | MFP5  | SPI2 slave select pin.                        |
|        |         |         | CAN0_TXD               | O    | MFP6  | CAN0 bus transmitter output.                  |
|        |         |         | SC2_PWR                | O    | MFP7  | Smart Card 2 power pin.                       |
|        |         |         | BPWM1_CH2              | I/O  | MFP11 | BPWM1 channel 2 output/capture input.         |
|        |         |         | QE11_INDEX             | I    | MFP12 | Quadrature encoder 1 index input              |
|        |         |         | USB_VBUS               | P    | MFP14 | Power supply from USB host or HUB.            |
|        | 86      | 98      | PA.13                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         |         | I <sup>2</sup> S0_MCLK | O    | MFP2  | I <sup>2</sup> S0 master clock output pin.    |
|        |         |         | UART4_RXD              | I    | MFP3  | UART4 data receiver input pin.                |
|        |         |         | I <sup>2</sup> C1_SDA  | I/O  | MFP4  | I <sup>2</sup> C1 data input/output pin.      |
|        |         |         | SPI2_CLK               | I/O  | MFP5  | SPI2 serial clock pin.                        |
|        |         |         | CAN0_RXD               | I    | MFP6  | CAN0 bus receiver input.                      |
|        |         |         | SC2_RST                | O    | MFP7  | Smart Card 2 reset pin.                       |
|        |         |         | BPWM1_CH3              | I/O  | MFP11 | BPWM1 channel 3 output/capture input.         |
|        |         |         | QE11_A                 | I    | MFP12 | Quadrature encoder 1 phase A input            |
|        |         |         | USB_D-                 | A    | MFP14 | USB differential signal D-.                   |
|        | 87      | 99      | PA.14                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         |         | I <sup>2</sup> S0_DI   | I    | MFP2  | I <sup>2</sup> S0 data input pin.             |
|        |         |         | UART0_TXD              | O    | MFP3  | UART0 data transmitter output pin.            |
|        |         |         | SPI2_MISO              | I/O  | MFP5  | SPI2 MISO (Master In, Slave Out) pin.         |
|        |         |         | I <sup>2</sup> C2_SCL  | I/O  | MFP6  | I <sup>2</sup> C2 clock pin.                  |
|        |         |         | SC2_DAT                | I/O  | MFP7  | Smart Card 2 data pin.                        |
|        |         |         | BPWM1_CH4              | I/O  | MFP11 | BPWM1 channel 4 output/capture input.         |
|        |         |         | QE11_B                 | I    | MFP12 | Quadrature encoder 1 phase B input            |
|        |         |         | USB_D+                 | A    | MFP14 | USB differential signal D+.                   |
|        | 88      | 100     | PA.15                  | I/O  | MFP0  | General purpose digital I/O pin.              |

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|--------|---------|---------|------------------------------|------|-------|---|
|        |         |         | I <sup>2</sup> S0_DO         | O    | MFP2  | I <sup>2</sup> S0 data output pin.  |
|        |         |         | UART0_RXD                    | I    | MFP3  | UART0 data receiver input pin.  |
|        |         |         | SPI2_MOSI                    | I/O  | MFP5  | SPI2 MOSI (Master Out, Slave In) pin.   |
|        |         |         | I <sup>2</sup> C2_SDA        | I/O  | MFP6  | I <sup>2</sup> C2 data input/output pin.  |
|        |         |         | SC2_CLK                      | O    | MFP7  | Smart Card 2 clock pin.   |
|        |         |         | BPWM1_CH5                    | I/O  | MFP11 | BPWM1 channel 5 output/capture input.   |
|        |         |         | EPWM0_SYNC_IN                | I    | MFP12 | EPWM0 counter synchronous trigger input pin.  |
|        |         |         | USB_OTG_ID                   | I    | MFP14 | USB identification.   |
| 41     | 89      | 101     | HSUSB_VRES                   | A    | MFP0  | HSUSB module reference resistor   |
| 42     | 90      | 102     | HSUSB_V <sub>DD33</sub>      | P    | MFP0  | Power supply for HSUSB V <sub>DD33</sub>  |
| 43     | 91      | 103     | HSUSB_VBUS                   | P    | MFP0  | HSUSB Power supply from USB host or HUB.  |
| 44     | 92      | 104     | HSUSB_D-                     | A    | MFP0  | HSUSB differential signal D-.   |
| 45     | 93      | 105     | HSUSB_VSS                    | P    | MFP0  | Ground pin for HSUSB.   |
| 46     | 94      | 106     | HSUSB_D+                     | A    | MFP0  | HSUSB differential signal D+.   |
| 47     | 95      | 107     | HSUSB_V <sub>DD12</sub> _CAP | A    | MFP0  | HSUSB Internal power regulator output 1.2V decoupling pin.<br><b>Note:</b> This pin needs to be connected with a 1uF capacitor. |
| 48     | 96      | 108     | HSUSB_ID                     | I    | MFP0  | HSUSB identification.   |
|        | 97      | 109     | PE.7                         | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         |         | SD0_CMD                      | I/O  | MFP3  | SD/SDIO0 command/response pin   |
|        |         |         | SPIM_D2                      | I/O  | MFP4  | SPIM data 2 pin for Quad Mode I/O.  |
|        |         |         | UART5_TXD                    | O    | MFP8  | UART5 data transmitter output pin.  |
|        |         |         | CAN1_TXD                     | O    | MFP9  | CAN1 bus transmitter output.  |
|        |         |         | QE11_INDEX                   | I    | MFP11 | Quadrature encoder 1 index input  |
|        |         |         | EPWM0_CH0                    | I/O  | MFP12 | EPWM0 channel 0 output/capture input.   |
|        |         |         | BPWM0_CH5                    | I/O  | MFP13 | BPWM0 channel 5 output/capture input.   |
|        | 98      | 110     | PE.6                         | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         |         | SD0_CLK                      | O    | MFP3  | SD/SDIO0 clock output pin   |
|        |         |         | SPIM_D3                      | I/O  | MFP4  | SPIM data 3 pin for Quad Mode I/O.  |
|        |         |         | SPI3_I2SMCLK                 | I/O  | MFP5  | SPI3 I <sup>2</sup> S master clock output pin   |
|        |         |         | SC0_nCD                      | I    | MFP6  | Smart Card 0 card detect pin.   |
|        |         |         | USCI0_CTL0                   | I/O  | MFP7  | USCI0 control 0 pin.  |
|        |         |         | UART5_RXD                    | I    | MFP8  | UART5 data receiver input pin.  |
|        |         |         | CAN1_RXD                     | I    | MFP9  | CAN1 bus receiver input.  |
|        |         |         | QE11_A                       | I    | MFP11 | Quadrature encoder 1 phase A input  |

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|--------|---------|---------|------------|------|-------|---------------------------------------|
|        |         |         | EPWM0_CH1  | I/O  | MFP12 | EPWM0 channel 1 output/capture input. |
|        |         |         | BPWM0_CH4  | I/O  | MFP13 | BPWM0 channel 4 output/capture input. |
|        | 99      | 111     | PE.5       | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |         |         | EBI_nRD    | O    | MFP2  | EBI read enable output pin.           |
|        |         |         | SD0_DAT3   | I/O  | MFP3  | SD/SDIO0 data line bit 3.             |
|        |         |         | SPIM_SS    | I/O  | MFP4  | SPIM slave select pin.                |
|        |         |         | SPI3_SS    | I/O  | MFP5  | SPI3 slave select pin.                |
|        |         |         | SC0_PWR    | O    | MFP6  | Smart Card 0 power pin.               |
|        |         |         | USCI0_CTL1 | I/O  | MFP7  | USCI0 control 1 pin.                  |
|        |         |         | QE11_B     | I    | MFP11 | Quadrature encoder 1 phase B input    |
|        |         |         | EPWM0_CH2  | I/O  | MFP12 | EPWM0 channel 2 output/capture input. |
|        |         |         | BPWM0_CH3  | I/O  | MFP13 | BPWM0 channel 3 output/capture input. |
|        | 100     | 112     | PE.4       | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |         |         | EBI_nWR    | O    | MFP2  | EBI write enable output pin.          |
|        |         |         | SD0_DAT2   | I/O  | MFP3  | SD/SDIO0 data line bit 2.             |
|        |         |         | SPIM_CLK   | I/O  | MFP4  | SPIM serial clock pin.                |
|        |         |         | SPI3_CLK   | I/O  | MFP5  | SPI3 serial clock pin.                |
|        |         |         | SC0_RST    | O    | MFP6  | Smart Card 0 reset pin.               |
|        |         |         | USCI0_DAT1 | I/O  | MFP7  | USCI0 data 1 pin.                     |
|        |         |         | QE10_INDEX | I    | MFP11 | Quadrature encoder 0 index input      |
|        |         |         | EPWM0_CH3  | I/O  | MFP12 | EPWM0 channel 3 output/capture input. |
|        |         |         | BPWM0_CH2  | I/O  | MFP13 | BPWM0 channel 2 output/capture input. |
|        | 101     | 113     | PE.3       | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |         |         | EBI_MCLK   | O    | MFP2  | EBI external clock output pin.        |
|        |         |         | SD0_DAT1   | I/O  | MFP3  | SD/SDIO0 data line bit 1.             |
|        |         |         | SPIM_MISO  | I/O  | MFP4  | SPIM MISO (Master In, Slave Out) pin. |
|        |         |         | SPI3_MISO  | I/O  | MFP5  | SPI3 MISO (Master In, Slave Out) pin. |
|        |         |         | SC0_DAT    | I/O  | MFP6  | Smart Card 0 data pin.                |
|        |         |         | USCI0_DAT0 | I/O  | MFP7  | USCI0 data 0 pin.                     |
|        |         |         | QE10_A     | I    | MFP11 | Quadrature encoder 0 phase A input    |
|        |         |         | EPWM0_CH4  | I/O  | MFP12 | EPWM0 channel 4 output/capture input. |
|        |         |         | BPWM0_CH1  | I/O  | MFP13 | BPWM0 channel 1 output/capture input. |
|        | 102     | 114     | PE.2       | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |         |         | EBI_ALE    | O    | MFP2  | EBI address latch enable output pin.  |

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|--------|---------|---------|------------------------|------|-------|---|
|        |         |         | SD0_DAT0               | I/O  | MFP3  | SD/SDIO0 data line bit 0.   |
|        |         |         | SPIM_MOSI              | I/O  | MFP4  | SPIM MOSI (Master Out, Slave In) pin.   |
|        |         |         | SPI3_MOSI              | I/O  | MFP5  | SPI3 MOSI (Master Out, Slave In) pin.   |
|        |         |         | SC0_CLK                | O    | MFP6  | Smart Card 0 clock pin.   |
|        |         |         | USCI0_CLK              | I/O  | MFP7  | USCI0 clock pin.  |
|        |         |         | QEI0_B                 | I    | MFP11 | Quadrature encoder 0 phase B input  |
|        |         |         | EPWM0_CH5              | I/O  | MFP12 | EPWM0 channel 5 output/capture input.   |
|        |         |         | BPWM0_CH0              | I/O  | MFP13 | BPWM0 channel 0 output/capture input.   |
|        | 103     | 115     | V <sub>SS</sub>        | P    | MFP0  | Ground pin for digital circuit.   |
|        | 104     | 116     | V <sub>DD</sub>        | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
|        | 105     | 117     | PE.1                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         |         | EBI_AD10               | I/O  | MFP2  | EBI address/data bus bit 10.  |
|        |         |         | QSPI0_MISO0            | I/O  | MFP3  | QSPI0 MISO0 (Master In, Slave Out) pin.   |
|        |         |         | SC2_DAT                | I/O  | MFP4  | Smart Card 2 data pin.  |
|        |         |         | I <sup>2</sup> S0_BCLK | O    | MFP5  | I <sup>2</sup> S0 bit clock output pin.   |
|        |         |         | SPI1_MISO              | I/O  | MFP6  | SPI1 MISO (Master In, Slave Out) pin.   |
|        |         |         | UART3_TXD              | O    | MFP7  | UART3 data transmitter output pin.  |
|        |         |         | I <sup>2</sup> C1_SCL  | I/O  | MFP8  | I <sup>2</sup> C1 clock pin.  |
|        |         |         | UART4_nCTS             | I    | MFP9  | UART4 clear to Send input pin.  |
|        | 106     | 118     | PE.0                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         |         | EBI_AD11               | I/O  | MFP2  | EBI address/data bus bit 11.  |
|        |         |         | QSPI0_MOSI0            | I/O  | MFP3  | QSPI0 MOSI0 (Master Out, Slave In) pin.   |
|        |         |         | SC2_CLK                | O    | MFP4  | Smart Card 2 clock pin.   |
|        |         |         | I <sup>2</sup> S0_MCLK | O    | MFP5  | I <sup>2</sup> S0 master clock output pin.                                      |
|        |         |         | SPI1_MOSI              | I/O  | MFP6  | SPI1 MOSI (Master Out, Slave In) pin.   |
|        |         |         | UART3_RXD              | I    | MFP7  | UART3 data receiver input pin.  |
|        |         |         | I <sup>2</sup> C1_SDA  | I/O  | MFP8  | I <sup>2</sup> C1 data input/output pin.  |
|        |         |         | UART4_nRTS             | O    | MFP9  | UART4 request to Send output pin.   |
|        | 107     | 119     | PH.8                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         |         | EBI_AD12               | I/O  | MFP2  | EBI address/data bus bit 12.  |
|        |         |         | QSPI0_CLK              | I/O  | MFP3  | QSPI0 serial clock pin.   |
|        |         |         | SC2_PWR                | O    | MFP4  | Smart Card 2 power pin.   |
|        |         |         | I <sup>2</sup> S0_DI   | I    | MFP5  | I <sup>2</sup> S0 data input pin.   |

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|--------|---------|---------|-------------------------|------|-------|--|
|        |         |         | SPI1_CLK                | I/O  | MFP6  | SPI1 serial clock pin.                                 |
|        |         |         | UART3_nRTS              | O    | MFP7  | UART3 request to Send output pin.                      |
|        |         |         | I <sup>2</sup> C1_SMBAL | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBALTER pin                   |
|        |         |         | I <sup>2</sup> C2_SCL   | I/O  | MFP9  | I <sup>2</sup> C2 clock pin.                           |
|        |         |         | UART1_TXD               | O    | MFP10 | UART1 data transmitter output pin.                     |
|        | 108     | 120     | PH.9                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         |         | EBI_AD13                | I/O  | MFP2  | EBI address/data bus bit 13.                           |
|        |         |         | QSPI0_SS                | I/O  | MFP3  | QSPI0 slave select pin.                                |
|        |         |         | SC2_RST                 | O    | MFP4  | Smart Card 2 reset pin.                                |
|        |         |         | I <sup>2</sup> S0_DO    | O    | MFP5  | I <sup>2</sup> S0 data output pin.                     |
|        |         |         | SPI1_SS                 | I/O  | MFP6  | SPI1 slave select pin.                                 |
|        |         |         | UART3_nCTS              | I    | MFP7  | UART3 clear to Send input pin.                         |
|        |         |         | I <sup>2</sup> C1_SMBUS | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBUS pin (PMBus CONTROL pin)  |
|        |         |         | I <sup>2</sup> C2_SDA   | I/O  | MFP9  | I <sup>2</sup> C2 data input/output pin.               |
|        |         |         | UART1_RXD               | I    | MFP10 | UART1 data receiver input pin.                         |
|        | 109     | 121     | PH.10                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         |         | EBI_AD14                | I/O  | MFP2  | EBI address/data bus bit 14.                           |
|        |         |         | QSPI0_MISO1             | I/O  | MFP3  | QSPI0 MISO1 (Master In, Slave Out) pin.                |
|        |         |         | SC2_nCD                 | I    | MFP4  | Smart Card 2 card detect pin.                          |
|        |         |         | I <sup>2</sup> S0_LRCK  | O    | MFP5  | I <sup>2</sup> S0 left right channel clock output pin. |
|        |         |         | SPI1_I2SMCLK            | I/O  | MFP6  | SPI1 I <sup>2</sup> S master clock output pin          |
|        |         |         | UART4_TXD               | O    | MFP7  | UART4 data transmitter output pin.                     |
|        |         |         | UART0_TXD               | O    | MFP8  | UART0 data transmitter output pin.                     |
|        | 110     | 122     | PH.11                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         |         | EBI_AD15                | I/O  | MFP2  | EBI address/data bus bit 15.                           |
|        |         |         | QSPI0_MOSI1             | I/O  | MFP3  | QSPI0 MOSI1 (Master Out, Slave In) pin.                |
|        |         |         | UART4_RXD               | I    | MFP7  | UART4 data receiver input pin.                         |
|        |         |         | UART0_RXD               | I    | MFP8  | UART0 data receiver input pin.                         |
|        |         |         | EPWM0_CH5               | I/O  | MFP11 | EPWM0 channel 5 output/capture input.                  |
|        | 111     | 123     | PD.14                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         |         | EBI_nCS0                | O    | MFP2  | EBI chip select 0 output pin.                          |
|        |         |         | SPI3_I2SMCLK            | I/O  | MFP3  | SPI3 I <sup>2</sup> S master clock output pin          |
|        |         |         | SC1_nCD                 | I    | MFP4  | Smart Card 1 card detect pin.                          |
|        |         |         | EPWM0_CH4               | I/O  | MFP11 | EPWM0 channel 4 output/capture input.                  |

| 64 Pin | 128 Pin | 144 Pin | Pin Name        | Type | MFP   | Description  |
|--------|---------|---------|-----------------|------|-------|--|
|        |         | 124     | PG.5            | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |         |         | EBI_nCS1        | O    | MFP2  | EBI chip select 1 output pin.  |
|        |         |         | SPI3_SS         | I/O  | MFP3  | SPI3 slave select pin.   |
|        |         |         | SC1_PWR         | O    | MFP4  | Smart Card 1 power pin.  |
|        |         |         | EPWM0_CH3       | I/O  | MFP11 | EPWM0 channel 3 output/capture input.  |
|        |         | 125     | PG.6            | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |         |         | EBI_nCS2        | O    | MFP2  | EBI chip select 2 output pin.  |
|        |         |         | SPI3_CLK        | I/O  | MFP3  | SPI3 serial clock pin.   |
|        |         |         | SC1_RST         | O    | MFP4  | Smart Card 1 reset pin.  |
|        |         |         | EPWM0_CH2       | I/O  | MFP11 | EPWM0 channel 2 output/capture input.  |
|        |         | 126     | PG.7            | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |         |         | EBI_nWRL        | O    | MFP2  | EBI low byte write enable output pin.  |
|        |         |         | SPI3_MISO       | I/O  | MFP3  | SPI3 MISO (Master In, Slave Out) pin.  |
|        |         |         | SC1_DAT         | I/O  | MFP4  | Smart Card 1 data pin.   |
|        |         |         | EPWM0_CH1       | I/O  | MFP11 | EPWM0 channel 1 output/capture input.  |
|        |         | 127     | PG.8            | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |         |         | EBI_nWRH        | O    | MFP2  | EBI high byte write enable output pin  |
|        |         |         | SPI3_MOSI       | I/O  | MFP3  | SPI3 MOSI (Master Out, Slave In) pin.  |
|        |         |         | SC1_CLK         | O    | MFP4  | Smart Card 1 clock pin.  |
|        |         |         | EPWM0_CH0       | I/O  | MFP11 | EPWM0 channel 0 output/capture input.  |
| 49     | 112     | 128     | V <sub>SS</sub> | P    | MFP0  | Ground pin for digital circuit.  |
| 50     | 113     | 129     | LDO_CAP         | A    | MFP0  | LDO output pin.<br><b>Note:</b> This pin needs to be connected with an external capacitor. |
| 51     | 114     | 130     | V <sub>DD</sub> | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit.            |
| 52     | 115     | 131     | PC.14           | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |         |         | EBI_AD11        | I/O  | MFP2  | EBI address/data bus bit 11.   |
|        |         |         | SC1_nCD         | I    | MFP3  | Smart Card 1 card detect pin.  |
|        |         |         | SPI0_I2SMCLK    | I/O  | MFP4  | SPI0 I <sup>2</sup> S master clock output pin  |
|        |         |         | USCI0_CTL0      | I/O  | MFP5  | USCI0 control 0 pin.   |
|        |         |         | QSPI0_CLK       | I/O  | MFP6  | QSPI0 serial clock pin.  |
|        |         |         | EPWM0_SYNC_IN   | I    | MFP11 | EPWM0 counter synchronous trigger input pin.   |
|        |         |         | ETM_TRACE_CLK   | I    | MFP12 | ETM receiver Trace Clock input pin   |
|        |         |         | TM1             | I/O  | MFP13 | Timer1 event counter input/toggle output pin.  |



| 64 Pin | 128 Pin | 144 Pin | Pin Name                 | Type | MFP   | Description  |
|--------|---------|---------|--------------------------|------|-------|--|
|        |         |         | USB_VBUS_ST              | I    | MFP14 | USB external VBUS regulator status pin.                |
|        |         |         | HSUSB_VBUS_ST            | I    | MFP15 | HSUSB external VBUS regulator status pin.              |
| 53     | 116     | 132     | PB.15                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         |         | EADC0_CH15               | A    | MFP1  | EADC0 channel 15 analog input.                         |
|        |         |         | EBI_AD12                 | I/O  | MFP2  | EBI address/data bus bit 12.                           |
|        |         |         | SC1_PWR                  | O    | MFP3  | Smart Card 1 power pin.                                |
|        |         |         | SPI0_SS                  | I/O  | MFP4  | SPI0 slave select pin.                                 |
|        |         |         | USCI0_CTL1               | I/O  | MFP5  | USCI0 control 1 pin.                                   |
|        |         |         | UART0_nCTS               | I    | MFP6  | UART0 clear to Send input pin.                         |
|        |         |         | UART3_TXD                | O    | MFP7  | UART3 data transmitter output pin.                     |
|        |         |         | I <sup>2</sup> C2_SMBAL  | O    | MFP8  | I <sup>2</sup> C2 SMBus SMBALTER pin                   |
|        |         |         | EPWM1_CH0                | I/O  | MFP11 | EPWM1 channel 0 output/capture input.                  |
|        |         |         | ETM_TRACE_DATA0          | I    | MFP12 | ETM receiver Trace Data 0 input pin                    |
|        |         |         | TM0_EXT                  | I/O  | MFP13 | Timer0 event counter input/toggle output pin.          |
|        |         |         | USB_VBUS_EN              | O    | MFP14 | USB external VBUS regulator enable pin.                |
|        |         |         | HSUSB_VBUS_EN            | O    | MFP15 | HSUSB external VBUS regulator enable pin.              |
| 54     | 117     | 133     | PB.14                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         |         | EADC0_CH14               | A    | MFP1  | EADC0 channel 14 analog input.                         |
|        |         |         | EBI_AD13                 | I/O  | MFP2  | EBI address/data bus bit 13.                           |
|        |         |         | SC1_RST                  | O    | MFP3  | Smart Card 1 reset pin.                                |
|        |         |         | SPI0_CLK                 | I/O  | MFP4  | SPI0 serial clock pin.                                 |
|        |         |         | USCI0_DAT1               | I/O  | MFP5  | USCI0 data 1 pin.                                      |
|        |         |         | UART0_nRTS               | O    | MFP6  | UART0 request to Send output pin.                      |
|        |         |         | UART3_RXD                | I    | MFP7  | UART3 data receiver input pin.                         |
|        |         |         | I <sup>2</sup> C2_SMBSUS | O    | MFP8  | I <sup>2</sup> C2 SMBus SMBSUS pin (PMBus CONTROL pin) |
|        |         |         | EPWM1_CH1                | I/O  | MFP11 | EPWM1 channel 1 output/capture input.                  |
|        |         |         | ETM_TRACE_DATA1          | I    | MFP12 | ETM receiver Trace Data 1 input pin                    |
|        |         |         | TM1_EXT                  | I/O  | MFP13 | Timer1 event counter input/toggle output pin.          |
|        |         |         | CLKO                     | O    | MFP14 | Clock Out  |
| 55     | 118     | 134     | PB.13                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         |         | EADC0_CH13               | A    | MFP1  | EADC0 channel 13 analog input.                         |
|        |         |         | DAC1_OUT                 | A    | MFP1  | DAC1 channel analog output.                            |
|        |         |         | ACMP0_P3                 | A    | MFP1  | Analog comparator 0 positive input 3 pin.              |
|        |         |         | ACMP1_P3                 | A    | MFP1  | Analog comparator 1 positive input 3 pin.              |

| 64 Pin | 128 Pin | 144 Pin | Pin Name              | Type | MFP   | Description   |
|--------|---------|---------|-----------------------|------|-------|---|
|        |         |         | EBI_AD14              | I/O  | MFP2  | EBI address/data bus bit 14.  |
|        |         |         | SC1_DAT               | I/O  | MFP3  | Smart Card 1 data pin.  |
|        |         |         | SPI0_MISO             | I/O  | MFP4  | SPI0 MISO (Master In, Slave Out) pin.   |
|        |         |         | USCI0_DAT0            | I/O  | MFP5  | USCI0 data 0 pin.   |
|        |         |         | UART0_TXD             | O    | MFP6  | UART0 data transmitter output pin.  |
|        |         |         | UART3_nRTS            | O    | MFP7  | UART3 request to Send output pin.   |
|        |         |         | I <sup>2</sup> C2_SCL | I/O  | MFP8  | I <sup>2</sup> C2 clock pin.  |
|        |         |         | EPWM1_CH2             | I/O  | MFP11 | EPWM1 channel 2 output/capture input.   |
|        |         |         | ETM_TRACE_DATA2       | I    | MFP12 | ETM receiver Trace Data 2 input pin   |
|        |         |         | TM2_EXT               | I/O  | MFP13 | Timer2 event counter input/toggle output pin.   |
| 56     | 119     | 135     | PB.12                 | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         |         | EADC0_CH12            | A    | MFP1  | EADC0 channel 12 analog input.  |
|        |         |         | DAC0_OUT              | A    | MFP1  | DAC0 channel analog output.   |
|        |         |         | ACMP0_P2              | A    | MFP1  | Analog comparator 0 positive input 2 pin.   |
|        |         |         | ACMP1_P2              | A    | MFP1  | Analog comparator 1 positive input 2 pin.   |
|        |         |         | EBI_AD15              | I/O  | MFP2  | EBI address/data bus bit 15.  |
|        |         |         | SC1_CLK               | O    | MFP3  | Smart Card 1 clock pin.   |
|        |         |         | SPI0_MOSI             | I/O  | MFP4  | SPI0 MOSI (Master Out, Slave In) pin.   |
|        |         |         | USCI0_CLK             | I/O  | MFP5  | USCI0 clock pin.  |
|        |         |         | UART0_RXD             | I    | MFP6  | UART0 data receiver input pin.  |
|        |         |         | UART3_nCTS            | I    | MFP7  | UART3 clear to Send input pin.  |
|        |         |         | I <sup>2</sup> C2_SDA | I/O  | MFP8  | I <sup>2</sup> C2 data input/output pin.  |
|        |         |         | SD0_nCD               | I    | MFP9  | SD/SDIO0 card detect input pin  |
|        |         |         | EPWM1_CH3             | I/O  | MFP11 | EPWM1 channel 3 output/capture input.   |
|        |         |         | ETM_TRACE_DATA3       | I    | MFP12 | ETM receiver Trace Data 3 input pin   |
|        |         |         | TM3_EXT               | I/O  | MFP13 | Timer3 event counter input/toggle output pin.   |
| 57     | 120     | 136     | AV <sub>DD</sub>      | P    | MFP0  | Power supply for internal analog circuit.   |
| 58     | 121     | 137     | V <sub>REF</sub>      | A    | MFP0  | ADC reference voltage input.<br><b>Note:</b> This pin needs to be connected with a 1uF capacitor. |
| 59     | 122     | 138     | AV <sub>SS</sub>      | P    | MFP0  | Ground pin for analog circuit.  |
| 60     | 123     | 139     | PB.11                 | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         |         | EADC0_CH11            | A    | MFP1  | EADC0 channel 11 analog input.  |
|        |         |         | EBI_ADR16             | O    | MFP2  | EBI address bus bit 16.   |
|        |         |         | EMAC_RMII_MDC         | O    | MFP3  | EMAC RMII PHY Management Clock output pin.  |

| 64 Pin | 128 Pin | 144 Pin | Pin Name                | Type | MFP   | Description                                   |
|--------|---------|---------|-------------------------|------|-------|---|
|        |         |         | UART0_nCTS              | I    | MFP5  | UART0 clear to Send input pin.                |
|        |         |         | UART4_TXD               | O    | MFP6  | UART4 data transmitter output pin.            |
|        |         |         | I <sup>2</sup> C1_SCL   | I/O  | MFP7  | I <sup>2</sup> C1 clock pin.                  |
|        |         |         | CAN0_TXD                | O    | MFP8  | CAN0 bus transmitter output.                  |
|        |         |         | SPI0_I2SMCLK            | I/O  | MFP9  | SPI0 I <sup>2</sup> S master clock output pin |
|        |         |         | BPWM1_CH0               | I/O  | MFP10 | BPWM1 channel 0 output/capture input.         |
|        |         |         | SPI3_CLK                | I/O  | MFP11 | SPI3 serial clock pin.                        |
|        |         |         | HSUSB_VBUS_ST           | I    | MFP14 | HSUSB external VBUS regulator status pin.     |
| 61     | 124     | 140     | PB.10                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         |         | EADC0_CH10              | A    | MFP1  | EADC0 channel 10 analog input.                |
|        |         |         | EBI_ADR17               | O    | MFP2  | EBI address bus bit 17.                       |
|        |         |         | EMAC_RMII_MDIO          | I/O  | MFP3  | EMAC RMII PHY Management Data pin.            |
|        |         |         | USCI1_CTL0              | I/O  | MFP4  | USCI1 control 0 pin.                          |
|        |         |         | UART0_nRTS              | O    | MFP5  | UART0 request to Send output pin.             |
|        |         |         | UART4_RXD               | I    | MFP6  | UART4 data receiver input pin.                |
|        |         |         | I <sup>2</sup> C1_SDA   | I/O  | MFP7  | I <sup>2</sup> C1 data input/output pin.      |
|        |         |         | CAN0_RXD                | I    | MFP8  | CAN0 bus receiver input.                      |
|        |         |         | BPWM1_CH1               | I/O  | MFP10 | BPWM1 channel 1 output/capture input.         |
|        |         |         | SPI3_SS                 | I/O  | MFP11 | SPI3 slave select pin.                        |
|        |         |         | HSUSB_VBUS_EN           | O    | MFP14 | HSUSB external VBUS regulator enable pin.     |
| 62     | 125     | 141     | PB.9                    | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         |         | EADC0_CH9               | A    | MFP1  | EADC0 channel 9 analog input.                 |
|        |         |         | EBI_ADR18               | O    | MFP2  | EBI address bus bit 18.                       |
|        |         |         | EMAC_RMII_TXD0          | O    | MFP3  | EMAC RMII Transmit Data bus bit 0.            |
|        |         |         | USCI1_CTL1              | I/O  | MFP4  | USCI1 control 1 pin.                          |
|        |         |         | UART0_TXD               | O    | MFP5  | UART0 data transmitter output pin.            |
|        |         |         | UART1_nCTS              | I    | MFP6  | UART1 clear to Send input pin.                |
|        |         |         | I <sup>2</sup> C1_SMBAL | O    | MFP7  | I <sup>2</sup> C1 SMBus SMBALTER pin          |
|        |         |         | BPWM1_CH2               | I/O  | MFP10 | BPWM1 channel 2 output/capture input.         |
|        |         |         | SPI3_MISO               | I/O  | MFP11 | SPI3 MISO (Master In, Slave Out) pin.         |
|        |         |         | INT7                    | I    | MFP13 | External interrupt 7 input pin.               |
| 63     | 126     | 142     | PB.8                    | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         |         | EADC0_CH8               | A    | MFP1  | EADC0 channel 8 analog input.                 |
|        |         |         | EBI_ADR19               | O    | MFP2  | EBI address bus bit 19.                       |

| 64 Pin | 128 Pin | 144 Pin | Pin Name                | Type | MFP   | Description   |
|--------|---------|---------|-------------------------|------|-------|---|
|        |         |         | EMAC_RMII_TXD1          | O    | MFP3  | EMAC RMII Transmit Data bus bit 1.                    |
|        |         |         | USCI1_CLK               | I/O  | MFP4  | USCI1 clock pin.                                      |
|        |         |         | UART0_RXD               | I    | MFP5  | UART0 data receiver input pin.                        |
|        |         |         | UART1_nRTS              | O    | MFP6  | UART1 request to Send output pin.                     |
|        |         |         | I <sup>2</sup> C1_SMBUS | O    | MFP7  | I <sup>2</sup> C1 SMBus SMBUS pin (PMBus CONTROL pin) |
|        |         |         | BPWM1_CH3               | I/O  | MFP10 | BPWM1 channel 3 output/capture input.                 |
|        |         |         | SPI3_MOSI               | I/O  | MFP11 | SPI3 MOSI (Master Out, Slave In) pin.                 |
|        |         |         | INT6                    | I    | MFP13 | External interrupt 6 input pin.                       |
| 64     | 127     | 143     | PB.7                    | I/O  | MFP0  | General purpose digital I/O pin.                      |
|        |         |         | EADC0_CH7               | A    | MFP1  | EADC0 channel 7 analog input.                         |
|        |         |         | EBI_nWRL                | O    | MFP2  | EBI low byte write enable output pin.                 |
|        |         |         | EMAC_RMII_TXEN          | O    | MFP3  | EMAC RMII Transmit Enable output pin.                 |
|        |         |         | USCI1_DAT0              | I/O  | MFP4  | USCI1 data 0 pin.                                     |
|        |         |         | CAN1_TXD                | O    | MFP5  | CAN1 bus transmitter output.                          |
|        |         |         | UART1_TXD               | O    | MFP6  | UART1 data transmitter output pin.                    |
|        |         |         | SD1_CMD                 | I/O  | MFP7  | SD/SDIO1 command/response pin                         |
|        |         |         | EBI_nCS0                | O    | MFP8  | EBI chip select 0 output pin.                         |
|        |         |         | BPWM1_CH4               | I/O  | MFP10 | BPWM1 channel 4 output/capture input.                 |
|        |         |         | EPWM1_BRAKE0            | I    | MFP11 | EPWM1 Brake 0 input pin.                              |
|        |         |         | EPWM1_CH4               | I/O  | MFP12 | EPWM1 channel 4 output/capture input.                 |
|        |         |         | INT5                    | I    | MFP13 | External interrupt 5 input pin.                       |
|        |         |         | USB_VBUS_ST             | I    | MFP14 | USB external VBUS regulator status pin.               |
|        |         |         | ACMP0_O                 | O    | MFP15 | Analog comparator 0 output pin.                       |
| 1      | 128     | 144     | PB.6                    | I/O  | MFP0  | General purpose digital I/O pin.                      |
|        |         |         | EADC0_CH6               | A    | MFP1  | EADC0 channel 6 analog input.                         |
|        |         |         | EBI_nWRH                | O    | MFP2  | EBI high byte write enable output pin                 |
|        |         |         | EMAC_PPS                | O    | MFP3  | EMAC Pulse Per Second output pin.                     |
|        |         |         | USCI1_DAT1              | I/O  | MFP4  | USCI1 data 1 pin.                                     |
|        |         |         | CAN1_RXD                | I    | MFP5  | CAN1 bus receiver input.                              |
|        |         |         | UART1_RXD               | I    | MFP6  | UART1 data receiver input pin.                        |
|        |         |         | SD1_CLK                 | O    | MFP7  | SD/SDIO1 clock output pin                             |
|        |         |         | EBI_nCS1                | O    | MFP8  | EBI chip select 1 output pin.                         |
|        |         |         | BPWM1_CH5               | I/O  | MFP10 | BPWM1 channel 5 output/capture input.                 |
|        |         |         | EPWM1_BRAKE1            | I    | MFP11 | EPWM1 Brake 1 input pin.                              |

| 64 Pin | 128 Pin | 144 Pin | Pin Name    | Type | MFP   | Description                             |
|--------|---------|---------|-------------|------|-------|---|
|        |         |         | EPWM1_CH5   | I/O  | MFP12 | EPWM1 channel 5 output/capture input.   |
|        |         |         | INT4        | I    | MFP13 | External interrupt 4 input pin.         |
|        |         |         | USB_VBUS_EN | O    | MFP14 | USB external VBUS regulator enable pin. |
|        |         |         | ACMP1_O     | O    | MFP15 | Analog comparator 1 output pin.         |

### 4.3 M48xxE8AE/M48xxGCAE Pin Description

#### 4.3.1 M481 Series Pin Description

MFP\* = Multi-function pin. (Refer to section SYS\_GP<sub>x</sub>\_MFPL and SYS\_GP<sub>x</sub>\_MFPH)

PA.0 MFP0 means SYS\_GPA\_MFPL[3:0] = 0x0.

PA.9 MFP5 means SYS\_GPA\_MFPH[7:4] = 0x5.

| 32 Pin | 48 Pin | 64 Pin | Pin Name               | Type | MFP   | Description                                   |
|--------|--------|--------|------------------------|------|-------|---|
|        | 48     | 1      | PB.6                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        | EADC0_CH6              | A    | MFP1  | EADC0 channel 6 analog input.                 |
|        |        |        | EBI_nWRHPA.1           | O    | MFP2  | EBI high byte write enable output pin         |
|        |        |        | CAN1_RXD               | I    | MFP5  | CAN1 bus receiver input.                      |
|        |        |        | UART1_RXD              | I    | MFP6  | UART1 data receiver input pin.                |
|        |        |        | EBI_nCS1               | O    | MFP8  | EBI chip select 1 output pin.                 |
|        |        |        | BPWM1_CH5              | I/O  | MFP10 | BPWM1 channel 5 output/capture input.         |
|        |        |        | EPWM1_BRAKE1           | I    | MFP11 | EPWM1 Brake 1 input pin.                      |
|        |        |        | EPWM1_CH5              | I/O  | MFP12 | EPWM1 channel 5 output/capture input.         |
|        |        |        | INT4                   | I    | MFP13 | External interrupt 4 input pin.               |
|        |        |        | USB_VBUS_EN            | O    | MFP14 | USB external VBUS regulator enable pin.       |
|        |        |        | ACMP1_O                | O    | MFP15 | Analog comparator 1 output pin.               |
| 1      | 1      | 2      | PB.5                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        | EADC0_CH5              | A    | MFP1  | EADC0 channel 5 analog input.                 |
|        |        |        | ACMP1_N                | A    | MFP1  | Analog comparator 1 negative input pin.       |
|        |        |        | EBI_ADR0               | O    | MFP2  | EBI address bus bit 0.                        |
|        |        |        | SD0_DAT3               | I/O  | MFP3  | SD/SDIO0 data line bit 3.                     |
|        |        |        | SPI1_MISO              | I/O  | MFP5  | SPI1 MISO (Master In, Slave Out) pin.         |
|        |        |        | I <sup>2</sup> C0_SCL  | I/O  | MFP6  | I <sup>2</sup> C0 clock pin.                  |
|        |        |        | UART5_TXD              | O    | MFP7  | UART5 data transmitter output pin.            |
|        |        |        | SC0_CLK                | O    | MFP9  | Smart Card 0 clock pin.                       |
|        |        |        | I <sup>2</sup> S0_BCLK | O    | MFP10 | I <sup>2</sup> S0 bit clock output pin.       |
|        |        |        | EPWM0_CH0              | I/O  | MFP11 | EPWM0 channel 0 output/capture input.         |
|        |        |        | UART2_TXD              | O    | MFP12 | UART2 data transmitter output pin.            |
|        |        |        | TM0                    | I/O  | MFP14 | Timer0 event counter input/toggle output pin. |
|        |        |        | INT0                   | I    | MFP15 | External interrupt 0 input pin.               |
| 2      | 2      | 3      | PB.4                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        | EADC0_CH4              | A    | MFP1  | EADC0 channel 4 analog input.                 |
|        |        |        | ACMP1_P1               | A    | MFP1  | Analog comparator 1 positive input 1 pin.     |

| 32 Pin | 48 Pin | 64 Pin | Pin Name               | Type | MFP   | Description                                   |
|--------|--------|--------|------------------------|------|-------|---|
|        |        |        | EBI_ADR1               | O    | MFP2  | EBI address bus bit 1.                        |
|        |        |        | SD0_DAT2               | I/O  | MFP3  | SD/SDIO0 data line bit 2.                     |
|        |        |        | SPI1_MOSI              | I/O  | MFP5  | SPI1 MOSI (Master Out, Slave In) pin.         |
|        |        |        | I <sup>2</sup> C0_SDA  | I/O  | MFP6  | I <sup>2</sup> C0 data input/output pin.      |
|        |        |        | UART5_RXD              | I    | MFP7  | UART5 data receiver input pin.                |
|        |        |        | SC0_DAT                | I/O  | MFP9  | Smart Card 0 data pin.                        |
|        |        |        | I <sup>2</sup> S0_MCLK | O    | MFP10 | I <sup>2</sup> S0 master clock output pin.    |
|        |        |        | EPWM0_CH1              | I/O  | MFP11 | EPWM0 channel 1 output/capture input.         |
|        |        |        | UART2_RXD              | I    | MFP12 | UART2 data receiver input pin.                |
|        |        |        | TM1                    | I/O  | MFP14 | Timer1 event counter input/toggle output pin. |
|        |        |        | INT1                   | I    | MFP15 | External interrupt 1 input pin.               |
| 3      | 3      | 4      | PB.3                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        | EADC0_CH3              | A    | MFP1  | EADC0 channel 3 analog input.                 |
|        |        |        | EADC1_CH11             | A    | MFP1  | EADC1 channel 11 analog input.                |
|        |        |        | ACMP0_N                | A    | MFP1  | Analog comparator 0 negative input pin.       |
|        |        |        | EBI_ADR2               | O    | MFP2  | EBI address bus bit 2.                        |
|        |        |        | SD0_DAT1               | I/O  | MFP3  | SD/SDIO0 data line bit 1.                     |
|        |        |        | SPI1_CLK               | I/O  | MFP5  | SPI1 serial clock pin.                        |
|        |        |        | UART1_TXD              | O    | MFP6  | UART1 data transmitter output pin.            |
|        |        |        | UART5_nRTS             | O    | MFP7  | UART5 request to Send output pin.             |
|        |        |        | SC0_RST                | O    | MFP9  | Smart Card 0 reset pin.                       |
|        |        |        | I <sup>2</sup> S0_DI   | I    | MFP10 | I <sup>2</sup> S0 data input pin.             |
|        |        |        | EPWM0_CH2              | I/O  | MFP11 | EPWM0 channel 2 output/capture input.         |
|        |        |        | I <sup>2</sup> C1_SCL  | I/O  | MFP12 | I <sup>2</sup> C1 clock pin.                  |
|        |        |        | TM2                    | I/O  | MFP14 | Timer2 event counter input/toggle output pin. |
|        |        |        | INT2                   | I    | MFP15 | External interrupt 2 input pin.               |
| 4      | 4      | 5      | PB.2                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        | EADC0_CH2              | A    | MFP1  | EADC0 channel 2 analog input.                 |
|        |        |        | EADC1_CH10             | A    | MFP1  | EADC1 channel 10 analog input.                |
|        |        |        | ACMP0_P1               | A    | MFP1  | Analog comparator 0 positive input 1 pin.     |
|        |        |        | EBI_ADR3               | O    | MFP2  | EBI address bus bit 3.                        |
|        |        |        | SD0_DAT0               | I/O  | MFP3  | SD/SDIO0 data line bit 0.                     |
|        |        |        | SPI1_SS                | I/O  | MFP5  | SPI1 slave select pin.                        |
|        |        |        | UART1_RXD              | I    | MFP6  | UART1 data receiver input pin.                |

| 32 Pin | 48 Pin | 64 Pin | Pin Name               | Type | MFP   | Description  |
|--------|--------|--------|------------------------|------|-------|--|
|        |        |        | UART5_nCTS             | I    | MFP7  | UART5 clear to Send input pin.                         |
|        |        |        | SC0_PWR                | O    | MFP9  | Smart Card 0 power pin.                                |
|        |        |        | I <sup>2</sup> S0_DO   | O    | MFP10 | I <sup>2</sup> S0 data output pin.                     |
|        |        |        | EPWM0_CH3              | I/O  | MFP11 | EPWM0 channel 3 output/capture input.                  |
|        |        |        | I <sup>2</sup> C1_SDA  | I/O  | MFP12 | I <sup>2</sup> C1 data input/output pin.               |
|        |        |        | TM3                    | I/O  | MFP14 | Timer3 event counter input/toggle output pin.          |
|        |        |        | INT3                   | I    | MFP15 | External interrupt 3 input pin.                        |
| 5      | 5      | 6      | PB.1                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        | EADC0_CH1              | A    | MFP1  | EADC0 channel 1 analog input.                          |
|        |        |        | EADC1_CH9              | A    | MFP1  | EADC1 channel 9 analog input.                          |
|        |        |        | EBI_ADR8               | O    | MFP2  | EBI address bus bit 8.                                 |
|        |        |        | SD0_CLK                | O    | MFP3  | SD/SDIO0 clock output pin                              |
|        |        |        | SPI1_I2SMCLK           | I/O  | MFP5  | SPI1 I <sup>2</sup> S master clock output pin          |
|        |        |        | UART2_TXD              | O    | MFP7  | UART2 data transmitter output pin.                     |
|        |        |        | I <sup>2</sup> C1_SCL  | I/O  | MFP9  | I <sup>2</sup> C1 clock pin.                           |
|        |        |        | I <sup>2</sup> S0_LRCK | O    | MFP10 | I <sup>2</sup> S0 left right channel clock output pin. |
|        |        |        | EPWM0_CH4              | I/O  | MFP11 | EPWM0 channel 4 output/capture input.                  |
|        |        |        | EPWM1_CH4              | I/O  | MFP12 | EPWM1 channel 4 output/capture input.                  |
|        |        |        | EPWM0_BRAKE0           | I    | MFP13 | EPWM0 Brake 0 input pin.                               |
| 6      | 6      | 7      | PB.0                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        | EADC0_CH0              | A    | MFP1  | EADC0 channel 0 analog input.                          |
|        |        |        | EADC1_CH8              | A    | MFP1  | EADC1 channel 8 analog input.                          |
|        |        |        | EBI_ADR9               | O    | MFP2  | EBI address bus bit 9.                                 |
|        |        |        | SD0_CMD                | I/O  | MFP3  | SD/SDIO0 command/response pin                          |
|        |        |        | SPI2_I2SMCLK           | I/O  | MFP4  | SPI2 I <sup>2</sup> S master clock output pin          |
|        |        |        | UART2_RXD              | I    | MFP7  | UART2 data receiver input pin.                         |
|        |        |        | SPI0_I2SMCLK           | I/O  | MFP8  | SPI0 I <sup>2</sup> S master clock output pin          |
|        |        |        | I <sup>2</sup> C1_SDA  | I/O  | MFP9  | I <sup>2</sup> C1 data input/output pin.               |
|        |        |        | EPWM0_CH5              | I/O  | MFP11 | EPWM0 channel 5 output/capture input.                  |
|        |        |        | EPWM1_CH5              | I/O  | MFP12 | EPWM1 channel 5 output/capture input.                  |
|        |        |        | EPWM0_BRAKE1           | I    | MFP13 | EPWM0 Brake 1 input pin.                               |
|        | 7      | 8      | PA.11                  | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        | EADC1_CH7              | A    | MFP1  | EADC1 channel 7 analog input.                          |
|        |        |        | ACMP0_P0               | A    | MFP1  | Analog comparator 0 positive input 0 pin.              |



| 32 Pin | 48 Pin | 64 Pin | Pin Name              | Type | MFP   | Description                                      |
|--------|--------|--------|-----------------------|------|-------|--|
|        |        |        | EBI_nRD               | O    | MFP2  | EBI read enable output pin.                      |
|        |        |        | SPI2_SS               | I/O  | MFP4  | SPI2 slave select pin.                           |
|        |        |        | I <sup>2</sup> C2_SCL | I/O  | MFP7  | I <sup>2</sup> C2 clock pin.                     |
|        |        |        | UART6_TXD             | O    | MFP8  | UART6 data transmitter output pin.               |
|        |        |        | BPWM0_CH0             | I/O  | MFP9  | BPWM0 channel 0 output/capture input.            |
|        |        |        | EPWM0_SYNC_OUT        | O    | MFP10 | EPWM0 counter synchronous trigger output pin.    |
|        |        |        | TM0_EXT               | I/O  | MFP13 | Timer0 external capture input/toggle output pin. |
|        | 8      | 9      | PA.10                 | I/O  | MFP0  | General purpose digital I/O pin.                 |
|        |        |        | EADC1_CH6             | A    | MFP1  | EADC1 channel 6 analog input.                    |
|        |        |        | ACMP1_P0              | A    | MFP1  | Analog comparator 1 positive input 0 pin.        |
|        |        |        | EBI_nWR               | O    | MFP2  | EBI write enable output pin.                     |
|        |        |        | SPI2_CLK              | I/O  | MFP4  | SPI2 serial clock pin.                           |
|        |        |        | I <sup>2</sup> C2_SDA | I/O  | MFP7  | I <sup>2</sup> C2 data input/output pin.         |
|        |        |        | UART6_RXD             | I    | MFP8  | UART6 data receiver input pin.                   |
|        |        |        | BPWM0_CH1             | I/O  | MFP9  | BPWM0 channel 1 output/capture input.            |
|        |        |        | QE11_INDEX            | I    | MFP10 | Quadrature encoder 1 index input                 |
|        |        |        | ECAP0_IC0             | I    | MFP11 | Enhanced capture unit 0 input 0 pin.             |
|        |        |        | TM1_EXT               | I/O  | MFP13 | Timer1 external capture input/toggle output pin. |
|        |        |        | DAC0_ST               | I    | MFP14 | DAC0 external trigger input.                     |
|        | 9      | 10     | PA.9                  | I/O  | MFP0  | General purpose digital I/O pin.                 |
|        |        |        | EADC1_CH5             | A    | MFP1  | EADC1 channel 5 analog input.                    |
|        |        |        | EBI_MCLK              | O    | MFP2  | EBI external clock output pin.                   |
|        |        |        | SPI2_MISO             | I/O  | MFP4  | SPI2 MISO (Master In, Slave Out) pin.            |
|        |        |        | UART1_TXD             | O    | MFP7  | UART1 data transmitter output pin.               |
|        |        |        | UART7_TXD             | O    | MFP8  | UART7 data transmitter output pin.               |
|        |        |        | BPWM0_CH2             | I/O  | MFP9  | BPWM0 channel 2 output/capture input.            |
|        |        |        | QE11_A                | I    | MFP10 | Quadrature encoder 1 phase A input               |
|        |        |        | ECAP0_IC1             | I    | MFP11 | Enhanced capture unit 0 input 1 pin.             |
|        |        |        | TM2_EXT               | I/O  | MFP13 | Timer2 external capture input/toggle output pin. |
|        | 10     | 11     | PA.8                  | I/O  | MFP0  | General purpose digital I/O pin.                 |
|        |        |        | EADC1_CH4             | A    | MFP1  | EADC1 channel 4 analog input.                    |
|        |        |        | EBI_ALE               | O    | MFP2  | EBI address latch enable output pin.             |

| 32 Pin | 48 Pin | 64 Pin | Pin Name               | Type | MFP   | Description  |
|--------|--------|--------|------------------------|------|-------|--|
|        |        |        | SPI2_MOSI              | I/O  | MFP4  | SPI2 MOSI (Master Out, Slave In) pin.                  |
|        |        |        | UART1_RXD              | I    | MFP7  | UART1 data receiver input pin.                         |
|        |        |        | UART7_RXD              | I    | MFP8  | UART7 data receiver input pin.                         |
|        |        |        | BPWM0_CH3              | I/O  | MFP9  | BPWM0 channel 3 output/capture input.                  |
|        |        |        | QE11_B                 | I    | MFP10 | Quadrature encoder 1 phase B input                     |
|        |        |        | ECAP0_IC2              | I    | MFP11 | Enhanced capture unit 0 input 2 pin.                   |
|        |        |        | TM3_EXT                | I/O  | MFP13 | Timer3 external capture input/toggle output pin.       |
|        |        |        | INT4                   | I    | MFP15 | External interrupt 4 input pin.                        |
|        |        | 12     | PF.6                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        | EBI_ADR19              | O    | MFP2  | EBI address bus bit 19.                                |
|        |        |        | SC0_CLK                | O    | MFP3  | Smart Card 0 clock pin.                                |
|        |        |        | I <sup>2</sup> S0_LRCK | O    | MFP4  | I <sup>2</sup> S0 left right channel clock output pin. |
|        |        |        | SPI0_MOSI              | I/O  | MFP5  | SPI0 MOSI (Master Out, Slave In) pin.                  |
|        |        |        | UART4_RXD              | I    | MFP6  | UART4 data receiver input pin.                         |
|        |        |        | EBI_nCS0               | O    | MFP7  | EBI chip select 0 output pin.                          |
|        |        |        | CAN2_RXD               | I    | MFP8  | CAN2 bus receiver input.                               |
|        |        |        | TAMPER0                | I/O  | MFP10 | TAMPER detector loop pin 0.                            |
|        |        | 13     | V <sub>BAT</sub>       | P    | MFP0  | Power supply by batteries for RTC.                     |
| 7      | 11     | 14     | PF.5                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        | UART2_RXD              | I    | MFP2  | UART2 data receiver input pin.                         |
|        |        |        | UART2_nCTS             | I    | MFP4  | UART2 clear to Send input pin.                         |
|        |        |        | EPWM0_CH0              | I/O  | MFP7  | EPWM0 channel 0 output/capture input.                  |
|        |        |        | BPWM0_CH4              | I/O  | MFP8  | BPWM0 channel 4 output/capture input.                  |
|        |        |        | EPWM0_SYNC_OUT         | O    | MFP9  | EPWM0 counter synchronous trigger output pin.          |
|        |        |        | X32_IN                 | I    | MFP10 | External 32.768 kHz crystal input pin.                 |
|        |        |        | EADC0_ST               | I    | MFP11 | EADC0 external trigger input.                          |
| 8      | 12     | 15     | PF.4                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        | UART2_TXD              | O    | MFP2  | UART2 data transmitter output pin.                     |
|        |        |        | UART2_nRTS             | O    | MFP4  | UART2 request to Send output pin.                      |
|        |        |        | EPWM0_CH1              | I/O  | MFP7  | EPWM0 channel 1 output/capture input.                  |
|        |        |        | BPWM0_CH5              | I/O  | MFP8  | BPWM0 channel 5 output/capture input.                  |
|        |        |        | X32_OUT                | O    | MFP10 | External 32.768 kHz crystal output pin.                |
|        |        |        | EADC1_ST               | I    | MFP11 | EADC1 external trigger input.                          |
| 9      | 13     | 16     | PF.3                   | I/O  | MFP0  | General purpose digital I/O pin.                       |

| 32 Pin | 48 Pin | 64 Pin | Pin Name                  | Type | MFP   | Description   |
|--------|--------|--------|---------------------------|------|-------|---|
|        |        |        | EBI_nCS0                  | O    | MFP2  | EBI chip select 0 output pin.                           |
|        |        |        | UART0_TXD                 | O    | MFP3  | UART0 data transmitter output pin.                      |
|        |        |        | I <sup>2</sup> C0_SCL     | I/O  | MFP4  | I <sup>2</sup> C0 clock pin.                            |
|        |        |        | XT1_IN                    | I    | MFP10 | External 4~24 MHz (high speed) crystal input pin.       |
|        |        |        | BPWM1_CH0                 | I/O  | MFP11 | BPWM1 channel 0 output/capture input.                   |
| 10     | 14     | 17     | PF.2                      | I/O  | MFP0  | General purpose digital I/O pin.                        |
|        |        |        | EBI_nCS1                  | O    | MFP2  | EBI chip select 1 output pin.                           |
|        |        |        | UART0_RXD                 | I    | MFP3  | UART0 data receiver input pin.                          |
|        |        |        | I <sup>2</sup> C0_SDA     | I/O  | MFP4  | I <sup>2</sup> C0 data input/output pin.                |
|        |        |        | QSPI0_CLK                 | I/O  | MFP5  | Quad SPI0 serial clock pin.                             |
|        |        |        | XT1_OUT                   | O    | MFP10 | External 4~24 MHz (high speed) crystal output pin.      |
|        |        |        | BPWM1_CH1                 | I/O  | MFP11 | BPWM1 channel 1 output/capture input.                   |
|        |        | 18     | PC.7                      | I/O  | MFP0  | General purpose digital I/O pin.                        |
|        |        |        | EBI_AD9                   | I/O  | MFP2  | EBI address/data bus bit 9.                             |
|        |        |        | SPI1_MISO                 | I/O  | MFP4  | SPI1 MISO (Master In, Slave Out) pin.                   |
|        |        |        | UART4_TXD                 | O    | MFP5  | UART4 data transmitter output pin.                      |
|        |        |        | UART0_nCTS                | I    | MFP7  | UART0 clear to Send input pin.                          |
|        |        |        | I <sup>2</sup> C1_SMBAL   | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBALTER pin                    |
|        |        |        | UART6_TXD                 | O    | MFP9  | UART6 data transmitter output pin.                      |
|        |        |        | EPWM1_CH2                 | I/O  | MFP11 | EPWM1 channel 2 output/capture input.                   |
|        |        |        | BPWM1_CH0                 | I/O  | MFP12 | BPWM1 channel 0 output/capture input.                   |
|        |        |        | TM0                       | I/O  | MFP14 | Timer0 event counter input/toggle output pin.           |
|        |        |        | INT3                      | I    | MFP15 | External interrupt 3 input pin.                         |
|        |        | 19     | PC.6                      | I/O  | MFP0  | General purpose digital I/O pin.                        |
|        |        |        | EBI_AD8                   | I/O  | MFP2  | EBI address/data bus bit 8.                             |
|        |        |        | SPI1_MOSI                 | I/O  | MFP4  | SPI1 MOSI (Master Out, Slave In) pin.                   |
|        |        |        | UART4_RXD                 | I    | MFP5  | UART4 data receiver input pin.                          |
|        |        |        | UART0_nRTS                | O    | MFP7  | UART0 request to Send output pin.                       |
|        |        |        | I <sup>2</sup> C1_SMBUSUS | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBUSUS pin (PMBus CONTROL pin) |
|        |        |        | UART6_RXD                 | I    | MFP9  | UART6 data receiver input pin.                          |
|        |        |        | EPWM1_CH3                 | I/O  | MFP11 | EPWM1 channel 3 output/capture input.                   |
|        |        |        | BPWM1_CH1                 | I/O  | MFP12 | BPWM1 channel 1 output/capture input.                   |
|        |        |        | TM1                       | I/O  | MFP14 | Timer1 event counter input/toggle output pin.           |
|        |        |        | INT2                      | I    | MFP15 | External interrupt 2 input pin.                         |

| 32 Pin | 48 Pin | 64 Pin | Pin Name              | Type | MFP   | Description  |
|--------|--------|--------|-----------------------|------|-------|--|
|        | 15     | 20     | PA.7                  | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |        |        | EBI_AD7               | I/O  | MFP2  | EBI address/data bus bit 7.  |
|        |        |        | SPI1_CLK              | I/O  | MFP4  | SPI1 serial clock pin.   |
|        |        |        | UART0_TXD             | O    | MFP7  | UART0 data transmitter output pin.   |
|        |        |        | I <sup>2</sup> C1_SCL | I/O  | MFP8  | I <sup>2</sup> C1 clock pin.   |
|        |        |        | QSPI1_MISO1           | I/O  | MFP9  | Quad SPI1 MISO1 (Master In, Slave Out) pin.  |
|        |        |        | EPWM1_CH4             | I/O  | MFP11 | EPWM1 channel 4 output/capture input.  |
|        |        |        | BPWM1_CH2             | I/O  | MFP12 | BPWM1 channel 2 output/capture input.  |
|        |        |        | ACMP0_WLAT            | I    | MFP13 | Analog comparator 0 window latch input pin   |
|        |        |        | TM2                   | I/O  | MFP14 | Timer2 event counter input/toggle output pin.  |
|        |        |        | INT1                  | I    | MFP15 | External interrupt 1 input pin.  |
|        | 16     | 21     | PA.6                  | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |        |        | EBI_AD6               | I/O  | MFP2  | EBI address/data bus bit 6.  |
|        |        |        | SPI1_SS               | I/O  | MFP4  | SPI1 slave select pin.   |
|        |        |        | UART0_RXD             | I    | MFP7  | UART0 data receiver input pin.   |
|        |        |        | I <sup>2</sup> C1_SDA | I/O  | MFP8  | I <sup>2</sup> C1 data input/output pin.   |
|        |        |        | QSPI1_MOSI1           | I/O  | MFP9  | Quad SPI1 MOSI1 (Master Out, Slave In) pin.  |
|        |        |        | EPWM1_CH5             | I/O  | MFP11 | EPWM1 channel 5 output/capture input.  |
|        |        |        | BPWM1_CH3             | I/O  | MFP12 | BPWM1 channel 3 output/capture input.  |
|        |        |        | ACMP1_WLAT            | I    | MFP13 | Analog comparator 1 window latch input pin   |
|        |        |        | TM3                   | I/O  | MFP14 | Timer3 event counter input/toggle output pin.  |
|        |        |        | INT0                  | I    | MFP15 | External interrupt 0 input pin.  |
|        |        | 22     | V <sub>SS</sub>       | P    | MFP0  | Ground pin for digital circuit.  |
|        |        | 23     | V <sub>DD</sub>       | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit.            |
|        |        | 24     | LDO_CAP               | A    | MFP0  | LDO output pin.<br><b>Note:</b> This pin needs to be connected with an external capacitor. |
|        | 17     | 25     | PA.5                  | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |        |        | QSPI0_MISO1           | I/O  | MFP3  | Quad SPI0 MISO1 (Master In, Slave Out) pin.  |
|        |        |        | SPI1_I2SMCLK          | I/O  | MFP4  | SPI1 I <sup>2</sup> S master clock output pin  |
|        |        |        | UART0_nCTS            | I    | MFP7  | UART0 clear to Send input pin.   |
|        |        |        | UART5_TXD             | O    | MFP8  | UART5 data transmitter output pin.   |
|        |        |        | I <sup>2</sup> C0_SCL | I/O  | MFP9  | I <sup>2</sup> C0 clock pin.   |
|        |        |        | CAN0_TXD              | O    | MFP10 | CAN0 bus transmitter output.   |

| 32 Pin | 48 Pin | 64 Pin | Pin Name                | Type | MFP   | Description                                   |
|--------|--------|--------|-------------------------|------|-------|---|
|        |        |        | UART0_TXD               | O    | MFP11 | UART0 data transmitter output pin.            |
|        |        |        | BPWM0_CH5               | I/O  | MFP12 | BPWM0 channel 5 output/capture input.         |
|        |        |        | EPWM0_CH0               | I/O  | MFP13 | EPWM0 channel 0 output/capture input.         |
|        |        |        | QEI0_INDEX              | I    | MFP14 | Quadrature encoder 0 index input              |
|        | 18     | 26     | PA.4                    | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        | QSPI0_MOSI1             | I/O  | MFP3  | Quad SPI0 MOSI1 (Master Out, Slave In) pin.   |
|        |        |        | SPI0_I2SMCLK            | I/O  | MFP4  | SPI0 I <sup>2</sup> S master clock output pin |
|        |        |        | SC0_nCD                 | I    | MFP6  | Smart Card 0 card detect pin.                 |
|        |        |        | UART0_nRTS              | O    | MFP7  | UART0 request to Send output pin.             |
|        |        |        | UART5_RXD               | I    | MFP8  | UART5 data receiver input pin.                |
|        |        |        | I <sup>2</sup> C0_SDA   | I/O  | MFP9  | I <sup>2</sup> C0 data input/output pin.      |
|        |        |        | CAN0_RXD                | I    | MFP10 | CAN0 bus receiver input.                      |
|        |        |        | UART0_RXD               | I    | MFP11 | UART0 data receiver input pin.                |
|        |        |        | BPWM0_CH4               | I/O  | MFP12 | BPWM0 channel 4 output/capture input.         |
|        |        |        | EPWM0_CH1               | I/O  | MFP13 | EPWM0 channel 1 output/capture input.         |
|        |        |        | QEI0_A                  | I    | MFP14 | Quadrature encoder 0 phase A input            |
| 11     | 19     | 27     | PA.3                    | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        | QSPI0_SS                | I/O  | MFP3  | Quad SPI0 slave select pin.                   |
|        |        |        | SPI0_SS                 | I/O  | MFP4  | SPI0 slave select pin.                        |
|        |        |        | SC0_PWR                 | O    | MFP6  | Smart Card 0 power pin.                       |
|        |        |        | UART4_TXD               | O    | MFP7  | UART4 data transmitter output pin.            |
|        |        |        | UART1_TXD               | O    | MFP8  | UART1 data transmitter output pin.            |
|        |        |        | I <sup>2</sup> C1_SCL   | I/O  | MFP9  | I <sup>2</sup> C1 clock pin.                  |
|        |        |        | I <sup>2</sup> C0_SMBAL | O    | MFP10 | I <sup>2</sup> C0 SMBus SMBALTER pin          |
|        |        |        | BPWM0_CH3               | I/O  | MFP12 | BPWM0 channel 3 output/capture input.         |
|        |        |        | EPWM0_CH2               | I/O  | MFP13 | EPWM0 channel 2 output/capture input.         |
|        |        |        | QEI0_B                  | I    | MFP14 | Quadrature encoder 0 phase B input            |
|        |        |        | EPWM1_BRAKE1            | I    | MFP15 | EPWM1 Brake 1 input pin.                      |
| 12     | 20     | 28     | PA.2                    | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        | QSPI0_CLK               | I/O  | MFP3  | Quad SPI0 serial clock pin.                   |
|        |        |        | SPI0_CLK                | I/O  | MFP4  | SPI0 serial clock pin.                        |
|        |        |        | SC0_RST                 | O    | MFP6  | Smart Card 0 reset pin.                       |
|        |        |        | UART4_RXD               | I    | MFP7  | UART4 data receiver input pin.                |
|        |        |        | UART1_RXD               | I    | MFP8  | UART1 data receiver input pin.                |

| 32 Pin | 48 Pin | 64 Pin | Pin Name                 | Type | MFP   | Description   |
|--------|--------|--------|--------------------------|------|-------|---|
|        |        |        | I <sup>2</sup> C1_SDA    | I/O  | MFP9  | I <sup>2</sup> C1 data input/output pin.  |
|        |        |        | I <sup>2</sup> C0_SMBSUS | O    | MFP10 | I <sup>2</sup> C0 SMBus SMBSUS pin (PMBus CONTROL pin)  |
|        |        |        | BPWM0_CH2                | I/O  | MFP12 | BPWM0 channel 2 output/capture input.   |
|        |        |        | EPWM0_CH3                | I/O  | MFP13 | EPWM0 channel 3 output/capture input.   |
| 13     | 21     | 29     | PA.1                     | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        | QSPI0_MISO0              | I/O  | MFP3  | Quad SPI0 MISO0 (Master In, Slave Out) pin.   |
|        |        |        | SPI0_MISO                | I/O  | MFP4  | SPI0 MISO (Master In, Slave Out) pin.   |
|        |        |        | SC0_DAT                  | I/O  | MFP6  | Smart Card 0 data pin.  |
|        |        |        | UART0_TXD                | O    | MFP7  | UART0 data transmitter output pin.  |
|        |        |        | UART1_nCTS               | I    | MFP8  | UART1 clear to Send input pin.  |
|        |        |        | I <sup>2</sup> C2_SCL    | I/O  | MFP9  | I <sup>2</sup> C2 clock pin.  |
|        |        |        | CCAP_DATA7               | I    | MFP10 | Camera capture data input bus bit 7.  |
|        |        |        | BPWM0_CH1                | I/O  | MFP12 | BPWM0 channel 1 output/capture input.   |
|        |        |        | EPWM0_CH4                | I/O  | MFP13 | EPWM0 channel 4 output/capture input.   |
| 14     | 22     | 30     | PA.0                     | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        | QSPI0_MOSI0              | I/O  | MFP3  | Quad SPI0 MOSI0 (Master Out, Slave In) pin.   |
|        |        |        | SPI0_MOSI                | I/O  | MFP4  | SPI0 MOSI (Master Out, Slave In) pin.   |
|        |        |        | SC0_CLK                  | O    | MFP6  | Smart Card 0 clock pin.   |
|        |        |        | UART0_RXD                | I    | MFP7  | UART0 data receiver input pin.  |
|        |        |        | UART1_nRTS               | O    | MFP8  | UART1 request to Send output pin.   |
|        |        |        | I <sup>2</sup> C2_SDA    | I/O  | MFP9  | I <sup>2</sup> C2 data input/output pin.  |
|        |        |        | CCAP_DATA6               | I    | MFP10 | Camera capture data input bus bit 6.  |
|        |        |        | BPWM0_CH0                | I/O  | MFP12 | BPWM0 channel 0 output/capture input.   |
|        |        |        | EPWM0_CH5                | I/O  | MFP13 | EPWM0 channel 5 output/capture input.   |
|        |        |        | DAC0_ST                  | I    | MFP15 | DAC0 external trigger input.  |
| 15     | 23     | 31     | V <sub>DDIO</sub>        | P    | MFP0  | Power supply for PA.0~PA.5.   |
| 16     | 24     | 32     | nRESET                   | I    | MFP0  | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.<br><b>Note:</b> It is recommended to use 10 kΩ pull-up resistor and 10 μF capacitor on nRESET pin. |
| 17     | 25     | 33     | PF.0                     | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        | UART1_TXD                | O    | MFP2  | UART1 data transmitter output pin.  |
|        |        |        | I <sup>2</sup> C1_SCL    | I/O  | MFP3  | I <sup>2</sup> C1 clock pin.  |
|        |        |        | UART0_TXD                | O    | MFP4  | UART0 data transmitter output pin.  |
|        |        |        | BPWM1_CH0                | I/O  | MFP12 | BPWM1 channel 0 output/capture input.   |

| 32 Pin | 48 Pin | 64 Pin | Pin Name               | Type | MFP   | Description   |
|--------|--------|--------|------------------------|------|-------|---|
|        |        |        | ICE_DAT                | I/O  | MFP14 | Serial wired debugger data pin.<br><b>Note:</b> It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.  |
| 18     | 26     | 34     | PF.1                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        | UART1_RXD              | I    | MFP2  | UART1 data receiver input pin.  |
|        |        |        | I <sup>2</sup> C1_SDA  | I/O  | MFP3  | I <sup>2</sup> C1 data input/output pin.  |
|        |        |        | UART0_RXD              | I    | MFP4  | UART0 data receiver input pin.  |
|        |        |        | BPWM1_CH1              | I/O  | MFP12 | BPWM1 channel 1 output/capture input.   |
|        |        |        | ICE_CLK                | I/O  | MFP14 | Serial wired debugger clock pin.<br><b>Note:</b> It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin. |
|        | 27     | 35     | PC.5                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        | EBI_AD5                | I/O  | MFP2  | EBI address/data bus bit 5.   |
|        |        |        | QSPI0_MISO1            | I/O  | MFP4  | Quad SPI0 MISO1 (Master In, Slave Out) pin.   |
|        |        |        | UART2_TXD              | O    | MFP8  | UART2 data transmitter output pin.  |
|        |        |        | I <sup>2</sup> C1_SCL  | I/O  | MFP9  | I <sup>2</sup> C1 clock pin.  |
|        |        |        | CAN0_TXD               | O    | MFP10 | CAN0 bus transmitter output.  |
|        |        |        | UART4_TXD              | O    | MFP11 | UART4 data transmitter output pin.  |
|        |        |        | EPWM1_CH0              | I/O  | MFP12 | EPWM1 channel 0 output/capture input.   |
|        |        |        | CCAP_DATA5             | I    | MFP13 | Camera capture data input bus bit 5.  |
|        |        |        | QSPI1_SS               | I/O  | MFP14 | Quad SPI1 slave select pin.   |
|        | 28     | 36     | PC.4                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        | EBI_AD4                | I/O  | MFP2  | EBI address/data bus bit 4.   |
|        |        |        | QSPI0_MOSI1            | I/O  | MFP4  | Quad SPI0 MOSI1 (Master Out, Slave In) pin.   |
|        |        |        | I <sup>2</sup> S0_BCLK | O    | MFP6  | I <sup>2</sup> S0 bit clock output pin.   |
|        |        |        | SPI1_I2SMCLK           | I/O  | MFP7  | SPI1 I <sup>2</sup> S master clock output pin   |
|        |        |        | UART2_RXD              | I    | MFP8  | UART2 data receiver input pin.  |
|        |        |        | I <sup>2</sup> C1_SDA  | I/O  | MFP9  | I <sup>2</sup> C1 data input/output pin.  |
|        |        |        | CAN0_RXD               | I    | MFP10 | CAN0 bus receiver input.  |
|        |        |        | UART4_RXD              | I    | MFP11 | UART4 data receiver input pin.  |
|        |        |        | EPWM1_CH1              | I/O  | MFP12 | EPWM1 channel 1 output/capture input.   |
|        |        |        | CCAP_DATA4             | I    | MFP13 | Camera capture data input bus bit 4.  |
|        |        |        | QSPI1_CLK              | I/O  | MFP14 | Quad SPI1 serial clock pin.   |
|        | 29     | 37     | PC.3                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        | EBI_AD3                | I/O  | MFP2  | EBI address/data bus bit 3.   |

| 32 Pin | 48 Pin | 64 Pin | Pin Name                 | Type | MFP   | Description  |
|--------|--------|--------|--------------------------|------|-------|--|
|        |        |        | QSPI0_SS                 | I/O  | MFP4  | Quad SPI0 slave select pin.                            |
|        |        |        | I <sup>2</sup> S0_MCLK   | O    | MFP6  | I <sup>2</sup> S0 master clock output pin.             |
|        |        |        | SPI1_MISO                | I/O  | MFP7  | SPI1 MISO (Master In, Slave Out) pin.                  |
|        |        |        | UART2_nRTS               | O    | MFP8  | UART2 request to Send output pin.                      |
|        |        |        | I <sup>2</sup> C0_SMBAL  | O    | MFP9  | I <sup>2</sup> C0 SMBus SMBALTER pin                   |
|        |        |        | CAN1_TXD                 | O    | MFP10 | CAN1 bus transmitter output.                           |
|        |        |        | UART3_TXD                | O    | MFP11 | UART3 data transmitter output pin.                     |
|        |        |        | EPWM1_CH2                | I/O  | MFP12 | EPWM1 channel 2 output/capture input.                  |
|        |        |        | CCAP_DATA3               | I    | MFP13 | Camera capture data input bus bit 3.                   |
|        |        |        | QSPI1_MISO0              | I/O  | MFP14 | Quad SPI1 MISO0 (Master In, Slave Out) pin.            |
|        | 30     | 38     | PC.2                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        | EBI_AD2                  | I/O  | MFP2  | EBI address/data bus bit 2.                            |
|        |        |        | QSPI0_CLK                | I/O  | MFP4  | Quad SPI0 serial clock pin.                            |
|        |        |        | I <sup>2</sup> S0_DI     | I    | MFP6  | I <sup>2</sup> S0 data input pin.                      |
|        |        |        | SPI1_MOSI                | I/O  | MFP7  | SPI1 MOSI (Master Out, Slave In) pin.                  |
|        |        |        | UART2_nCTS               | I    | MFP8  | UART2 clear to Send input pin.                         |
|        |        |        | I <sup>2</sup> C0_SMBSUS | O    | MFP9  | I <sup>2</sup> C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
|        |        |        | CAN1_RXD                 | I    | MFP10 | CAN1 bus receiver input.                               |
|        |        |        | UART3_RXD                | I    | MFP11 | UART3 data receiver input pin.                         |
|        |        |        | EPWM1_CH3                | I/O  | MFP12 | EPWM1 channel 3 output/capture input.                  |
|        |        |        | CCAP_DATA2               | I    | MFP13 | Camera capture data input bus bit 2.                   |
|        |        |        | QSPI1_MOSI0              | I/O  | MFP14 | Quad SPI1 MOSI0 (Master Out, Slave In) pin.            |
| 19     | 31     | 39     | PC.1                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        | EBI_AD1                  | I/O  | MFP2  | EBI address/data bus bit 1.                            |
|        |        |        | QSPI0_MISO0              | I/O  | MFP4  | Quad SPI0 MISO0 (Master In, Slave Out) pin.            |
|        |        |        | I <sup>2</sup> S0_DO     | O    | MFP6  | I <sup>2</sup> S0 data output pin.                     |
|        |        |        | SPI1_CLK                 | I/O  | MFP7  | SPI1 serial clock pin.                                 |
|        |        |        | UART2_TXD                | O    | MFP8  | UART2 data transmitter output pin.                     |
|        |        |        | I <sup>2</sup> C0_SCL    | I/O  | MFP9  | I <sup>2</sup> C0 clock pin.                           |
|        |        |        | CAN2_TXD                 | O    | MFP10 | CAN2 bus transmitter output.                           |
|        |        |        | EPWM1_CH4                | I/O  | MFP12 | EPWM1 channel 4 output/capture input.                  |
|        |        |        | CCAP_DATA1               | I    | MFP13 | Camera capture data input bus bit 1.                   |
|        |        |        | ACMP0_O                  | O    | MFP14 | Analog comparator 0 output pin.                        |
|        |        |        | EADC0_ST                 | I    | MFP15 | EADC0 external trigger input.                          |



| 32 Pin | 48 Pin | 64 Pin | Pin Name               | Type | MFP   | Description  |
|--------|--------|--------|------------------------|------|-------|--|
| 20     | 32     | 40     | PC.0                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        | EBI_AD0                | I/O  | MFP2  | EBI address/data bus bit 0.                            |
|        |        |        | QSPI0_MOSI0            | I/O  | MFP4  | Quad SPI0 MOSI0 (Master Out, Slave In) pin.            |
|        |        |        | I <sup>2</sup> S0_LRCK | O    | MFP6  | I <sup>2</sup> S0 left right channel clock output pin. |
|        |        |        | SPI1_SS                | I/O  | MFP7  | SPI1 slave select pin.                                 |
|        |        |        | UART2_RXD              | I    | MFP8  | UART2 data receiver input pin.                         |
|        |        |        | I <sup>2</sup> C0_SDA  | I/O  | MFP9  | I <sup>2</sup> C0 data input/output pin.               |
|        |        |        | CAN2_RXD               | I    | MFP10 | CAN2 bus receiver input.                               |
|        |        |        | EPWM1_CH5              | I/O  | MFP12 | EPWM1 channel 5 output/capture input.                  |
|        |        |        | CCAP_DATA0             | I    | MFP13 | Camera capture data input bus bit 0.                   |
|        |        |        | ACMP1_O                | O    | MFP14 | Analog comparator 1 output pin.                        |
|        |        |        | EADC1_ST               | I    | MFP15 | EADC1 external trigger input.                          |
|        |        | 41     | PD.3                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        | EBI_AD10               | I/O  | MFP2  | EBI address/data bus bit 10.                           |
|        |        |        | SPI0_SS                | I/O  | MFP4  | SPI0 slave select pin.                                 |
|        |        |        | UART3_nRTS             | O    | MFP5  | UART3 request to Send output pin.                      |
|        |        |        | UART0_TXD              | O    | MFP9  | UART0 data transmitter output pin.                     |
|        |        | 42     | PD.2                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        | EBI_AD11               | I/O  | MFP2  | EBI address/data bus bit 11.                           |
|        |        |        | SPI0_CLK               | I/O  | MFP4  | SPI0 serial clock pin.                                 |
|        |        |        | UART3_nCTS             | I    | MFP5  | UART3 clear to Send input pin.                         |
|        |        |        | UART0_RXD              | I    | MFP9  | UART0 data receiver input pin.                         |
|        |        | 43     | PD.1                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        | EBI_AD12               | I/O  | MFP2  | EBI address/data bus bit 12.                           |
|        |        |        | SPI0_MISO              | I/O  | MFP4  | SPI0 MISO (Master In, Slave Out) pin.                  |
|        |        |        | UART3_TXD              | O    | MFP5  | UART3 data transmitter output pin.                     |
|        |        |        | I <sup>2</sup> C2_SCL  | I/O  | MFP6  | I <sup>2</sup> C2 clock pin.                           |
|        |        | 44     | PD.0                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        | EBI_AD13               | I/O  | MFP2  | EBI address/data bus bit 13.                           |
|        |        |        | SPI0_MOSI              | I/O  | MFP4  | SPI0 MOSI (Master Out, Slave In) pin.                  |
|        |        |        | UART3_RXD              | I    | MFP5  | UART3 data receiver input pin.                         |
|        |        |        | I <sup>2</sup> C2_SDA  | I/O  | MFP6  | I <sup>2</sup> C2 data input/output pin.               |
|        |        |        | TM2                    | I/O  | MFP14 | Timer2 event counter input/toggle output pin.          |
| 21     | 33     | 45     | PA.12                  | I/O  | MFP0  | General purpose digital I/O pin.                       |

| 32 Pin | 48 Pin | 64 Pin | Pin Name               | Type | MFP   | Description                                  |
|--------|--------|--------|------------------------|------|-------|--|
|        |        |        | I <sup>2</sup> S0_BCLK | O    | MFP2  | I <sup>2</sup> S0 bit clock output pin.      |
|        |        |        | UART4_TXD              | O    | MFP3  | UART4 data transmitter output pin.           |
|        |        |        | I <sup>2</sup> C1_SCL  | I/O  | MFP4  | I <sup>2</sup> C1 clock pin.                 |
|        |        |        | SPI2_SS                | I/O  | MFP5  | SPI2 slave select pin.                       |
|        |        |        | CAN0_TXD               | O    | MFP6  | CAN0 bus transmitter output.                 |
|        |        |        | BPWM1_CH2              | I/O  | MFP11 | BPWM1 channel 2 output/capture input.        |
|        |        |        | QE11_INDEX             | I    | MFP12 | Quadrature encoder 1 index input             |
|        |        |        | USB_VBUS               | P    | MFP14 | Power supply from USB host or HUB.           |
| 22     | 34     | 46     | PA.13                  | I/O  | MFP0  | General purpose digital I/O pin.             |
|        |        |        | I <sup>2</sup> S0_MCLK | O    | MFP2  | I <sup>2</sup> S0 master clock output pin.   |
|        |        |        | UART4_RXD              | I    | MFP3  | UART4 data receiver input pin.               |
|        |        |        | I <sup>2</sup> C1_SDA  | I/O  | MFP4  | I <sup>2</sup> C1 data input/output pin.     |
|        |        |        | SPI2_CLK               | I/O  | MFP5  | SPI2 serial clock pin.                       |
|        |        |        | CAN0_RXD               | I    | MFP6  | CAN0 bus receiver input.                     |
|        |        |        | BPWM1_CH3              | I/O  | MFP11 | BPWM1 channel 3 output/capture input.        |
|        |        |        | QE11_A                 | I    | MFP12 | Quadrature encoder 1 phase A input           |
|        |        |        | USB_D-                 | A    | MFP14 | USB differential signal D-.                  |
| 23     | 35     | 47     | PA.14                  | I/O  | MFP0  | General purpose digital I/O pin.             |
|        |        |        | I <sup>2</sup> S0_DI   | I    | MFP2  | I <sup>2</sup> S0 data input pin.            |
|        |        |        | UART0_TXD              | O    | MFP3  | UART0 data transmitter output pin.           |
|        |        |        | SPI2_MISO              | I/O  | MFP5  | SPI2 MISO (Master In, Slave Out) pin.        |
|        |        |        | I <sup>2</sup> C2_SCL  | I/O  | MFP6  | I <sup>2</sup> C2 clock pin.                 |
|        |        |        | BPWM1_CH4              | I/O  | MFP11 | BPWM1 channel 4 output/capture input.        |
|        |        |        | QE11_B                 | I    | MFP12 | Quadrature encoder 1 phase B input           |
|        |        |        | USB_D+                 | A    | MFP14 | USB differential signal D+.                  |
| 24     | 36     | 48     | PA.15                  | I/O  | MFP0  | General purpose digital I/O pin.             |
|        |        |        | I <sup>2</sup> S0_DO   | O    | MFP2  | I <sup>2</sup> S0 data output pin.           |
|        |        |        | UART0_RXD              | I    | MFP3  | UART0 data receiver input pin.               |
|        |        |        | SPI2_MOSI              | I/O  | MFP5  | SPI2 MOSI (Master Out, Slave In) pin.        |
|        |        |        | I <sup>2</sup> C2_SDA  | I/O  | MFP6  | I <sup>2</sup> C2 data input/output pin.     |
|        |        |        | BPWM1_CH5              | I/O  | MFP11 | BPWM1 channel 5 output/capture input.        |
|        |        |        | EPWM0_SYNC_IN          | I    | MFP12 | EPWM0 counter synchronous trigger input pin. |
|        |        |        | USB_OTG_ID             | I    | MFP14 | USB_identification.                          |
| 25     | 37     | 49     | V <sub>SS</sub>        | P    | MFP0  | Ground pin for digital circuit.              |

| 32 Pin                   | 48 Pin | 64 Pin | Pin Name                | Type | MFP   | Description  |
|--------------------------|--------|--------|-------------------------|------|-------|--|
| 26                       | 38     | 50     | LDO_CAP                 | A    | MFP0  | LDO output pin.<br><b>Note:</b> This pin needs to be connected with an external capacitor. |
| 27                       | 39     | 51     | V <sub>DD</sub>         | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit.            |
|                          | 40     | 52     | PC.14                   | I/O  | MFP0  | General purpose digital I/O pin.   |
|                          |        |        | EBI_AD11                | I/O  | MFP2  | EBI address/data bus bit 11.   |
|                          |        |        | SPI0_I2SMCLK            | I/O  | MFP4  | SPI0 I <sup>2</sup> S master clock output pin  |
|                          |        |        | QSPI0_CLK               | I/O  | MFP6  | Quad SPI0 serial clock pin.  |
|                          |        |        | EPWM0_SYNC_IN           | I    | MFP11 | EPWM0 counter synchronous trigger input pin.   |
|                          |        |        | ETM_TRACE_CLK           | I    | MFP12 | ETM receiver Trace Clock input pin   |
|                          |        |        | TM1                     | I/O  | MFP13 | Timer1 event counter input/toggle output pin.  |
|                          |        |        | USB_VBUS_ST             | I    | MFP14 | USB external VBUS regulator status pin.  |
| 28                       | 41     | 53     | PB.15                   | I/O  | MFP0  | General purpose digital I/O pin.   |
|                          |        |        | EADC0_CH15              | A    | MFP1  | EADC0 channel 15 analog input.   |
|                          |        |        | EADC1_CH15              | A    | MFP1  | EADC1 channel 15 analog input.   |
|                          |        |        | EBI_AD12                | I/O  | MFP2  | EBI address/data bus bit 12.   |
|                          |        |        | SPI0_SS                 | I/O  | MFP4  | SPI0 slave select pin.   |
|                          |        |        | UART0_nCTS              | I    | MFP6  | UART0 clear to Send input pin.   |
|                          |        |        | UART3_TXD               | O    | MFP7  | UART3 data transmitter output pin.   |
|                          |        |        | I <sup>2</sup> C2_SMBAL | O    | MFP8  | I <sup>2</sup> C2 SMBus SMBALTER pin   |
|                          |        |        | EPWM0_BRAKE1            | I    | MFP10 | EPWM0 Brake 1 input pin.   |
|                          |        |        | EPWM1_CH0               | I/O  | MFP11 | EPWM1 channel 0 output/capture input.  |
|                          |        |        | ETM_TRACE_DATA0         | I    | MFP12 | ETM receiver Trace Data 0 input pin  |
|                          |        |        | TM0_EXT                 | I/O  | MFP13 | Timer0 external capture input/toggle output pin.   |
|                          |        |        | USB_VBUS_EN             | O    | MFP14 | USB external VBUS regulator enable pin.  |
|                          |        |        | 29                      | 42   | 54    | PB.14  |
| EADC0_CH14               | A      | MFP1   |                         |      |       | EADC0 channel 14 analog input.   |
| EADC1_CH14               | A      | MFP1   |                         |      |       | EADC1 channel 14 analog input.   |
| EBI_AD13                 | I/O    | MFP2   |                         |      |       | EBI address/data bus bit 13.   |
| SPI0_CLK                 | I/O    | MFP4   |                         |      |       | SPI0 serial clock pin.   |
| UART0_nRTS               | O      | MFP6   |                         |      |       | UART0 request to Send output pin.  |
| UART3_RXD                | I      | MFP7   |                         |      |       | UART3 data receiver input pin.   |
| I <sup>2</sup> C2_SMBSUS | O      | MFP8   |                         |      |       | I <sup>2</sup> C2 SMBus SMBSUS pin (PMBus CONTROL pin)                                     |
| EPWM1_CH1                | I/O    | MFP11  |                         |      |       | EPWM1 channel 1 output/capture input.  |

| 32 Pin | 48 Pin | 64 Pin | Pin Name              | Type | MFP   | Description                                      |
|--------|--------|--------|-----------------------|------|-------|--|
|        |        |        | ETM_TRACE_DATA1       | I    | MFP12 | ETM receiver Trace Data 1 input pin              |
|        |        |        | TM1_EXT               | I/O  | MFP13 | Timer1 external capture input/toggle output pin. |
|        |        |        | CLKO                  | O    | MFP14 | Clock Out  |
|        |        |        | USB_VBUS_ST           | I    | MFP15 | USB external VBUS regulator status pin.          |
| 30     | 43     | 55     | PB.13                 | I/O  | MFP0  | General purpose digital I/O pin.                 |
|        |        |        | EADC0_CH13            | A    | MFP1  | EADC0 channel 13 analog input.                   |
|        |        |        | EADC1_CH13            | A    | MFP1  | EADC1 channel 13 analog input.                   |
|        |        |        | ACMP0_P3              | A    | MFP1  | Analog comparator 0 positive input 3 pin.        |
|        |        |        | ACMP1_P3              | A    | MFP1  | Analog comparator 1 positive input 3 pin.        |
|        |        |        | EBI_AD14              | I/O  | MFP2  | EBI address/data bus bit 14.                     |
|        |        |        | SPI0_MISO             | I/O  | MFP4  | SPI0 MISO (Master In, Slave Out) pin.            |
|        |        |        | UART0_TXD             | O    | MFP6  | UART0 data transmitter output pin.               |
|        |        |        | UART3_nRTS            | O    | MFP7  | UART3 request to Send output pin.                |
|        |        |        | I <sup>2</sup> C2_SCL | I/O  | MFP8  | I <sup>2</sup> C2 clock pin.                     |
|        |        |        | CCAP_PIXCLK           | I    | MFP10 | Camera capture interface pix clock input pin.    |
|        |        |        | EPWM1_CH2             | I/O  | MFP11 | EPWM1 channel 2 output/capture input.            |
|        |        |        | ETM_TRACE_DATA2       | I    | MFP12 | ETM receiver Trace Data 2 input pin              |
|        |        |        | TM2_EXT               | I/O  | MFP13 | Timer2 external capture input/toggle output pin. |
| 31     | 44     | 56     | PB.12                 | I/O  | MFP0  | General purpose digital I/O pin.                 |
|        |        |        | EADC0_CH12            | A    | MFP1  | EADC0 channel 12 analog input.                   |
|        |        |        | EADC1_CH12            | A    | MFP1  | EADC1 channel 12 analog input.                   |
|        |        |        | DAC0_OUT              | A    | MFP1  | DAC0 channel analog output.                      |
|        |        |        | ACMP0_P2              | A    | MFP1  | Analog comparator 0 positive input 2 pin.        |
|        |        |        | ACMP1_P2              | A    | MFP1  | Analog comparator 1 positive input 2 pin.        |
|        |        |        | EBI_AD15              | I/O  | MFP2  | EBI address/data bus bit 15.                     |
|        |        |        | SPI0_MOSI             | I/O  | MFP4  | SPI0 MOSI (Master Out, Slave In) pin.            |
|        |        |        | UART0_RXD             | I    | MFP6  | UART0 data receiver input pin.                   |
|        |        |        | UART3_nCTS            | I    | MFP7  | UART3 clear to Send input pin.                   |
|        |        |        | I <sup>2</sup> C2_SDA | I/O  | MFP8  | I <sup>2</sup> C2 data input/output pin.         |
|        |        |        | SD0_nCD               | I    | MFP9  | SD/SDIO0 card detect input pin                   |
|        |        |        | CCAP_SCLK             | O    | MFP10 | Camera capture interface sensor clock pin.       |
|        |        |        | EPWM1_CH3             | I/O  | MFP11 | EPWM1 channel 3 output/capture input.            |
|        |        |        | ETM_TRACE_DATA3       | I    | MFP12 | ETM receiver Trace Data 3 input pin              |
|        |        |        | TM3_EXT               | I/O  | MFP13 | Timer3 external capture input/toggle output pin. |

| 32 Pin | 48 Pin | 64 Pin     | Pin Name                | Type  | MFP                                       | Description   |
|--------|--------|------------|-------------------------|-------|---|---|
| 32     | 45     | 57         | AV <sub>DD</sub>        | P     | MFP0                                      | Power supply for internal analog circuit.   |
|        |        | 58         | V <sub>REF</sub>        | A     | MFP0                                      | ADC reference voltage input.<br><b>Note:</b> This pin needs to be connected with a 1uF capacitor. |
|        | 46     | 59         | AV <sub>SS</sub>        | P     | MFP0                                      | Ground pin for analog circuit.  |
|        |        | 60         | PB.11                   | I/O   | MFP0                                      | General purpose digital I/O pin.  |
|        |        |            | EADC0_CH11              | A     | MFP1                                      | EADC0 channel 11 analog input.  |
|        |        |            | EBI_ADR16               | O     | MFP2                                      | EBI address bus bit 16.   |
|        |        |            | UART0_nCTS              | I     | MFP5                                      | UART0 clear to Send input pin.  |
|        |        |            | UART4_TXD               | O     | MFP6                                      | UART4 data transmitter output pin.  |
|        |        |            | I <sup>2</sup> C1_SCL   | I/O   | MFP7                                      | I <sup>2</sup> C1 clock pin.  |
|        |        |            | CAN0_TXD                | O     | MFP8                                      | CAN0 bus transmitter output.  |
|        |        |            | SPI0_I2SMCLK            | I/O   | MFP9                                      | SPI0 I <sup>2</sup> S master clock output pin   |
|        |        |            | BPWM1_CH0               | I/O   | MFP10                                     | BPWM1 channel 0 output/capture input.   |
|        |        |            | CCAP_SFIELD             | I     | MFP12                                     | Camera capture interface SFIELD input pin.  |
|        |        | 61         | PB.10                   | I/O   | MFP0                                      | General purpose digital I/O pin.  |
|        |        |            | EADC0_CH10              | A     | MFP1                                      | EADC0 channel 10 analog input.  |
|        |        |            | EBI_ADR17               | O     | MFP2                                      | EBI address bus bit 17.   |
|        |        |            | UART0_nRTS              | O     | MFP5                                      | UART0 request to Send output pin.   |
|        |        |            | UART4_RXD               | I     | MFP6                                      | UART4 data receiver input pin.  |
|        |        |            | I <sup>2</sup> C1_SDA   | I/O   | MFP7                                      | I <sup>2</sup> C1 data input/output pin.  |
|        |        |            | CAN0_RXD                | I     | MFP8                                      | CAN0 bus receiver input.  |
|        |        |            | BPWM1_CH1               | I/O   | MFP10                                     | BPWM1 channel 1 output/capture input.   |
|        |        | CCAP_VSYNC | I                       | MFP12 | Camera capture interface vsync input pin. |   |
|        |        | 62         | PB.9                    | I/O   | MFP0                                      | General purpose digital I/O pin.  |
|        |        |            | EADC0_CH9               | A     | MFP1                                      | EADC0 channel 9 analog input.   |
|        |        |            | EBI_ADR18               | O     | MFP2                                      | EBI address bus bit 18.   |
|        |        |            | UART0_TXD               | O     | MFP5                                      | UART0 data transmitter output pin.  |
|        |        |            | UART1_nCTS              | I     | MFP6                                      | UART1 clear to Send input pin.  |
|        |        |            | I <sup>2</sup> C1_SMBAL | O     | MFP7                                      | I <sup>2</sup> C1 SMBus SMBALTER pin  |
|        |        |            | UART7_TXD               | O     | MFP8                                      | UART7 data transmitter output pin.  |
|        |        |            | I <sup>2</sup> C0_SCL   | I/O   | MFP9                                      | I <sup>2</sup> C0 clock pin.  |
|        |        |            | BPWM1_CH2               | I/O   | MFP10                                     | BPWM1 channel 2 output/capture input.   |
|        |        |            | CAN2_TXD                | O     | MFP12                                     | CAN2 bus transmitter output.  |
|        |        |            | INT7                    | I     | MFP13                                     | External interrupt 7 input pin.   |

| 32 Pin | 48 Pin | 64 Pin | Pin Name                | Type | MFP   | Description   |
|--------|--------|--------|-------------------------|------|-------|---|
|        |        |        | CCAP_HSYNC              | I    | MFP14 | Camera capture interface hsync input pin.             |
|        |        | 63     | PB.8                    | I/O  | MFP0  | General purpose digital I/O pin.                      |
|        |        |        | EADC0_CH8               | A    | MFP1  | EADC0 channel 8 analog input.                         |
|        |        |        | EBI_ADR19               | O    | MFP2  | EBI address bus bit 19.                               |
|        |        |        | UART0_RXD               | I    | MFP5  | UART0 data receiver input pin.                        |
|        |        |        | UART1_nRTS              | O    | MFP6  | UART1 request to Send output pin.                     |
|        |        |        | I <sup>2</sup> C1_SMBUS | O    | MFP7  | I <sup>2</sup> C1 SMBus SMBUS pin (PMBus CONTROL pin) |
|        |        |        | UART7_RXD               | I    | MFP8  | UART7 data receiver input pin.                        |
|        |        |        | I <sup>2</sup> C0_SDA   | I/O  | MFP9  | I <sup>2</sup> C0 data input/output pin.              |
|        |        |        | BPWM1_CH3               | I/O  | MFP10 | BPWM1 channel 3 output/capture input.                 |
|        |        |        | CAN2_RXD                | I    | MFP12 | CAN2 bus receiver input.                              |
|        |        |        | INT6                    | I    | MFP13 | External interrupt 6 input pin.                       |
|        | 47     | 64     | PB.7                    | I/O  | MFP0  | General purpose digital I/O pin.                      |
|        |        |        | EADC0_CH7               | A    | MFP1  | EADC0 channel 7 analog input.                         |
|        |        |        | EBI_nWRL                | O    | MFP2  | EBI low byte write enable output pin.                 |
|        |        |        | CAN1_TXD                | O    | MFP5  | CAN1 bus transmitter output.                          |
|        |        |        | UART1_TXD               | O    | MFP6  | UART1 data transmitter output pin.                    |
|        |        |        | EBI_nCS0                | O    | MFP8  | EBI chip select 0 output pin.                         |
|        |        |        | BPWM1_CH4               | I/O  | MFP10 | BPWM1 channel 4 output/capture input.                 |
|        |        |        | EPWM1_BRAKE0            | I    | MFP11 | EPWM1 Brake 0 input pin.                              |
|        |        |        | EPWM1_CH4               | I/O  | MFP12 | EPWM1 channel 4 output/capture input.                 |
|        |        |        | INT5                    | I    | MFP13 | External interrupt 5 input pin.                       |
|        |        |        | USB_VBUS_ST             | I    | MFP14 | USB external VBUS regulator status pin.               |
|        |        |        | ACMP0_O                 | O    | MFP15 | Analog comparator 0 output pin.                       |

4.3.2 M482 Series Pin Description

Note: PA.15 MFP can only be as USB\_OTG\_ID when enable full-Speed USB.

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name               | Type | MFP   | Description                                   |
|--------|--------|--------|---------|------------------------|------|-------|---|
| 1      | 1      | 2      | 1       | PB.5                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EADC0_CH5              | A    | MFP1  | EADC0 channel 5 analog input.                 |
|        |        |        |         | ACMP1_N                | A    | MFP1  | Analog comparator 1 negative input pin.       |
|        |        |        |         | EBI_ADR0               | O    | MFP2  | EBI address bus bit 0.                        |
|        |        |        |         | SD0_DAT3               | I/O  | MFP3  | SD/SDIO0 data line bit 3.                     |
|        |        |        |         | SPI1_MISO              | I/O  | MFP5  | SPI1 MISO (Master In, Slave Out) pin.         |
|        |        |        |         | I <sup>2</sup> C0_SCL  | I/O  | MFP6  | I <sup>2</sup> C0 clock pin.                  |
|        |        |        |         | UART5_TXD              | O    | MFP7  | UART5 data transmitter output pin.            |
|        |        |        |         | SC0_CLK                | O    | MFP9  | Smart Card 0 clock pin.                       |
|        |        |        |         | I <sup>2</sup> S0_BCLK | O    | MFP10 | I <sup>2</sup> S0 bit clock output pin.       |
|        |        |        |         | EPWM0_CH0              | I/O  | MFP11 | EPWM0 channel 0 output/capture input.         |
|        |        |        |         | UART2_TXD              | O    | MFP12 | UART2 data transmitter output pin.            |
|        |        |        |         | TM0                    | I/O  | MFP14 | Timer0 event counter input/toggle output pin. |
|        |        |        |         | INT0                   | I    | MFP15 | External interrupt 0 input pin.               |
| 2      | 2      | 3      | 2       | PB.4                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EADC0_CH4              | A    | MFP1  | EADC0 channel 4 analog input.                 |
|        |        |        |         | ACMP1_P1               | A    | MFP1  | Analog comparator 1 positive input 1 pin.     |
|        |        |        |         | EBI_ADR1               | O    | MFP2  | EBI address bus bit 1.                        |
|        |        |        |         | SD0_DAT2               | I/O  | MFP3  | SD/SDIO0 data line bit 2.                     |
|        |        |        |         | SPI1_MOSI              | I/O  | MFP5  | SPI1 MOSI (Master Out, Slave In) pin.         |
|        |        |        |         | I <sup>2</sup> C0_SDA  | I/O  | MFP6  | I <sup>2</sup> C0 data input/output pin.      |
|        |        |        |         | UART5_RXD              | I    | MFP7  | UART5 data receiver input pin.                |
|        |        |        |         | SC0_DAT                | I/O  | MFP9  | Smart Card 0 data pin.                        |
|        |        |        |         | I <sup>2</sup> S0_MCLK | O    | MFP10 | I <sup>2</sup> S0 master clock output pin.    |
|        |        |        |         | EPWM0_CH1              | I/O  | MFP11 | EPWM0 channel 1 output/capture input.         |
|        |        |        |         | UART2_RXD              | I    | MFP12 | UART2 data receiver input pin.                |
|        |        |        |         | TM1                    | I/O  | MFP14 | Timer1 event counter input/toggle output pin. |
|        |        |        |         | INT1                   | I    | MFP15 | External interrupt 1 input pin.               |
| 3      | 3      | 4      | 3       | PB.3                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EADC0_CH3              | A    | MFP1  | EADC0 channel 3 analog input.                 |
|        |        |        |         | EADC1_CH11             | A    | MFP1  | EADC1 channel 11 analog input.                |
|        |        |        |         | ACMP0_N                | A    | MFP1  | Analog comparator 0 negative input pin.       |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name              | Type | MFP   | Description                                   |
|--------|--------|--------|---------|-----------------------|------|-------|---|
|        |        |        |         | EBI_ADR2              | O    | MFP2  | EBI address bus bit 2.                        |
|        |        |        |         | SD0_DAT1              | I/O  | MFP3  | SD/SDIO0 data line bit 1.                     |
|        |        |        |         | SPI1_CLK              | I/O  | MFP5  | SPI1 serial clock pin.                        |
|        |        |        |         | UART1_TXD             | O    | MFP6  | UART1 data transmitter output pin.            |
|        |        |        |         | UART5_nRTS            | O    | MFP7  | UART5 request to Send output pin.             |
|        |        |        |         | SC0_RST               | O    | MFP9  | Smart Card 0 reset pin.                       |
|        |        |        |         | I <sup>2</sup> S0_DI  | I    | MFP10 | I <sup>2</sup> S0 data input pin.             |
|        |        |        |         | EPWM0_CH2             | I/O  | MFP11 | EPWM0 channel 2 output/capture input.         |
|        |        |        |         | I <sup>2</sup> C1_SCL | I/O  | MFP12 | I <sup>2</sup> C1 clock pin.                  |
|        |        |        |         | TM2                   | I/O  | MFP14 | Timer2 event counter input/toggle output pin. |
|        |        |        |         | INT2                  | I    | MFP15 | External interrupt 2 input pin.               |
| 4      | 4      | 5      | 4       | PB.2                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EADC0_CH2             | A    | MFP1  | EADC0 channel 2 analog input.                 |
|        |        |        |         | EADC1_CH10            | A    | MFP1  | EADC1 channel 10 analog input.                |
|        |        |        |         | ACMP0_P1              | A    | MFP1  | Analog comparator 0 positive input 1 pin.     |
|        |        |        |         | EBI_ADR3              | O    | MFP2  | EBI address bus bit 3.                        |
|        |        |        |         | SD0_DAT0              | I/O  | MFP3  | SD/SDIO0 data line bit 0.                     |
|        |        |        |         | SPI1_SS               | I/O  | MFP5  | SPI1 slave select pin.                        |
|        |        |        |         | UART1_RXD             | I    | MFP6  | UART1 data receiver input pin.                |
|        |        |        |         | UART5_nCTS            | I    | MFP7  | UART5 clear to Send input pin.                |
|        |        |        |         | SC0_PWR               | O    | MFP9  | Smart Card 0 power pin.                       |
|        |        |        |         | I <sup>2</sup> S0_DO  | O    | MFP10 | I <sup>2</sup> S0 data output pin.            |
|        |        |        |         | EPWM0_CH3             | I/O  | MFP11 | EPWM0 channel 3 output/capture input.         |
|        |        |        |         | I <sup>2</sup> C1_SDA | I/O  | MFP12 | I <sup>2</sup> C1 data input/output pin.      |
|        |        |        |         | TM3                   | I/O  | MFP14 | Timer3 event counter input/toggle output pin. |
|        |        |        |         | INT3                  | I    | MFP15 | External interrupt 3 input pin.               |
|        |        |        | 5       | PC.12                 | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EBI_ADR4              | O    | MFP2  | EBI address bus bit 4.                        |
|        |        |        |         | UART0_TXD             | O    | MFP3  | UART0 data transmitter output pin.            |
|        |        |        |         | I <sup>2</sup> C0_SCL | I/O  | MFP4  | I <sup>2</sup> C0 clock pin.                  |
|        |        |        |         | UART6_TXD             | O    | MFP5  | UART6 data transmitter output pin.            |
|        |        |        |         | SC0_nCD               | I    | MFP9  | Smart Card 0 card detect pin.                 |
|        |        |        |         | ECAP1_IC2             | I    | MFP11 | Enhanced capture unit 1 input 2 pin.          |
|        |        |        |         | EPWM1_CH0             | I/O  | MFP12 | EPWM1 channel 0 output/capture input.         |



| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name               | Type | MFP   | Description  |
|--------|--------|--------|---------|------------------------|------|-------|--|
|        |        |        |         | ACMP0_O                | O    | MFP14 | Analog comparator 0 output pin.                        |
|        |        |        | 6       | PC.11                  | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_ADR5               | O    | MFP2  | EBI address bus bit 5.                                 |
|        |        |        |         | UART0_RXD              | I    | MFP3  | UART0 data receiver input pin.                         |
|        |        |        |         | I <sup>2</sup> C0_SDA  | I/O  | MFP4  | I <sup>2</sup> C0 data input/output pin.               |
|        |        |        |         | UART6_RXD              | I    | MFP5  | UART6 data receiver input pin.                         |
|        |        |        |         | ECAP1_IC1              | I    | MFP11 | Enhanced capture unit 1 input 1 pin.                   |
|        |        |        |         | EPWM1_CH1              | I/O  | MFP12 | EPWM1 channel 1 output/capture input.                  |
|        |        |        |         | ACMP1_O                | O    | MFP14 | Analog comparator 1 output pin.                        |
|        |        |        | 7       | PC.10                  | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_ADR6               | O    | MFP2  | EBI address bus bit 6.                                 |
|        |        |        |         | UART6_nRTS             | O    | MFP5  | UART6 request to Send output pin.                      |
|        |        |        |         | UART3_TXD              | O    | MFP7  | UART3 data transmitter output pin.                     |
|        |        |        |         | CAN1_TXD               | O    | MFP9  | CAN1 bus transmitter output.                           |
|        |        |        |         | ECAP1_IC0              | I    | MFP11 | Enhanced capture unit 1 input 0 pin.                   |
|        |        |        |         | EPWM1_CH2              | I/O  | MFP12 | EPWM1 channel 2 output/capture input.                  |
|        |        |        |         | EADC1_ST               | I    | MFP14 | EADC1 external trigger input.                          |
|        |        |        | 8       | PC.9                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_ADR7               | O    | MFP2  | EBI address bus bit 7.                                 |
|        |        |        |         | UART6_nCTS             | I    | MFP5  | UART6 clear to Send input pin.                         |
|        |        |        |         | UART3_RXD              | I    | MFP7  | UART3 data receiver input pin.                         |
|        |        |        |         | CAN1_RXD               | I    | MFP9  | CAN1 bus receiver input.                               |
|        |        |        |         | EPWM1_CH3              | I/O  | MFP12 | EPWM1 channel 3 output/capture input.                  |
|        |        |        |         | EADC1_ST               | I    | MFP14 | EADC1 external trigger input.                          |
| 5      | 5      | 6      | 9       | PB.1                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EADC0_CH1              | A    | MFP1  | EADC0 channel 1 analog input.                          |
|        |        |        |         | EADC1_CH9              | A    | MFP1  | EADC1 channel 9 analog input.                          |
|        |        |        |         | EBI_ADR8               | O    | MFP2  | EBI address bus bit 8.                                 |
|        |        |        |         | SD0_CLK                | O    | MFP3  | SD/SDIO0 clock output pin                              |
|        |        |        |         | SPI1_I2SMCLK           | I/O  | MFP5  | SPI1 I <sup>2</sup> S master clock output pin          |
|        |        |        |         | UART2_TXD              | O    | MFP7  | UART2 data transmitter output pin.                     |
|        |        |        |         | I <sup>2</sup> C1_SCL  | I/O  | MFP9  | I <sup>2</sup> C1 clock pin.                           |
|        |        |        |         | I <sup>2</sup> S0_LRCK | O    | MFP10 | I <sup>2</sup> S0 left right channel clock output pin. |
|        |        |        |         | EPWM0_CH4              | I/O  | MFP11 | EPWM0 channel 4 output/capture input.                  |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name              | Type | MFP   | Description   |
|--------|--------|--------|---------|-----------------------|------|-------|---|
|        |        |        |         | EPWM1_CH4             | I/O  | MFP12 | EPWM1 channel 4 output/capture input.   |
|        |        |        |         | EPWM0_BRAKE0          | I    | MFP13 | EPWM0 Brake 0 input pin.  |
| 6      | 6      | 7      | 10      | PB.0                  | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EADC0_CH0             | A    | MFP1  | EADC0 channel 0 analog input.   |
|        |        |        |         | EADC1_CH8             | A    | MFP1  | EADC1 channel 8 analog input.   |
|        |        |        |         | EBI_ADR9              | O    | MFP2  | EBI address bus bit 9.  |
|        |        |        |         | SD0_CMD               | I/O  | MFP3  | SD/SDIO0 command/response pin   |
|        |        |        |         | SPI2_I2SMCLK          | I/O  | MFP4  | SPI2 I <sup>2</sup> S master clock output pin                                   |
|        |        |        |         | UART2_RXD             | I    | MFP7  | UART2 data receiver input pin.  |
|        |        |        |         | SPI0_I2SMCLK          | I/O  | MFP8  | SPI0 I <sup>2</sup> S master clock output pin                                   |
|        |        |        |         | I <sup>2</sup> C1_SDA | I/O  | MFP9  | I <sup>2</sup> C1 data input/output pin.  |
|        |        |        |         | EPWM0_CH5             | I/O  | MFP11 | EPWM0 channel 5 output/capture input.   |
|        |        |        |         | EPWM1_CH5             | I/O  | MFP12 | EPWM1 channel 5 output/capture input.   |
|        |        |        |         | EPWM0_BRAKE1          | I    | MFP13 | EPWM0 Brake 1 input pin.  |
|        |        |        | 11      | V <sub>SS</sub>       | P    | MFP0  | Ground pin for digital circuit.   |
|        |        |        | 12      | V <sub>DD</sub>       | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
|        | 7      | 8      | 13      | PA.11                 | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EADC1_CH7             | A    | MFP1  | EADC1 channel 7 analog input.   |
|        |        |        |         | ACMP0_P0              | A    | MFP1  | Analog comparator 0 positive input 0 pin.                                       |
|        |        |        |         | EBI_nRD               | O    | MFP2  | EBI read enable output pin.   |
|        |        |        |         | SPI2_SS               | I/O  | MFP4  | SPI2 slave select pin.  |
|        |        |        |         | I <sup>2</sup> C2_SCL | I/O  | MFP7  | I <sup>2</sup> C2 clock pin.  |
|        |        |        |         | UART6_TXD             | O    | MFP8  | UART6 data transmitter output pin.  |
|        |        |        |         | BPWM0_CH0             | I/O  | MFP9  | BPWM0 channel 0 output/capture input.   |
|        |        |        |         | EPWM0_SYNC_OUT        | O    | MFP10 | EPWM0 counter synchronous trigger output pin.                                   |
|        |        |        |         | TM0_EXT               | I/O  | MFP13 | Timer0 external capture input/toggle output pin.                                |
|        | 8      | 9      | 14      | PA.10                 | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EADC1_CH6             | A    | MFP1  | EADC1 channel 6 analog input.   |
|        |        |        |         | ACMP1_P0              | A    | MFP1  | Analog comparator 1 positive input 0 pin.                                       |
|        |        |        |         | EBI_nWR               | O    | MFP2  | EBI write enable output pin.  |
|        |        |        |         | SPI2_CLK              | I/O  | MFP4  | SPI2 serial clock pin.  |
|        |        |        |         | I <sup>2</sup> C2_SDA | I/O  | MFP7  | I <sup>2</sup> C2 data input/output pin.  |
|        |        |        |         | UART6_RXD             | I    | MFP8  | UART6 data receiver input pin.  |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name     | Type | MFP   | Description                                      |
|--------|--------|--------|---------|--------------|------|-------|--|
|        |        |        |         | BPWM0_CH1    | I/O  | MFP9  | BPWM0 channel 1 output/capture input.            |
|        |        |        |         | QE11_INDEX   | I    | MFP10 | Quadrature encoder 1 index input                 |
|        |        |        |         | ECAP0_IC0    | I    | MFP11 | Enhanced capture unit 0 input 0 pin.             |
|        |        |        |         | TM1_EXT      | I/O  | MFP13 | Timer1 external capture input/toggle output pin. |
|        |        |        |         | DAC0_ST      | I    | MFP14 | DAC0 external trigger input.                     |
|        |        |        |         |              |      |       |  |
|        | 9      | 10     | 15      | PA.9         | I/O  | MFP0  | General purpose digital I/O pin.                 |
|        |        |        |         | EADC1_CH5    | A    | MFP1  | EADC1 channel 5 analog input.                    |
|        |        |        |         | EBI_MCLK     | O    | MFP2  | EBI external clock output pin.                   |
|        |        |        |         | SPI2_MISO    | I/O  | MFP4  | SPI2 MISO (Master In, Slave Out) pin.            |
|        |        |        |         | UART1_TXD    | O    | MFP7  | UART1 data transmitter output pin.               |
|        |        |        |         | UART7_TXD    | O    | MFP8  | UART7 data transmitter output pin.               |
|        |        |        |         | BPWM0_CH2    | I/O  | MFP9  | BPWM0 channel 2 output/capture input.            |
|        |        |        |         | QE11_A       | I    | MFP10 | Quadrature encoder 1 phase A input               |
|        |        |        |         | ECAP0_IC1    | I    | MFP11 | Enhanced capture unit 0 input 1 pin.             |
|        |        |        |         | TM2_EXT      | I/O  | MFP13 | Timer2 external capture input/toggle output pin. |
|        |        |        |         |              |      |       |  |
|        | 10     | 11     | 16      | PA.8         | I/O  | MFP0  | General purpose digital I/O pin.                 |
|        |        |        |         | EADC1_CH4    | A    | MFP1  | EADC1 channel 4 analog input.                    |
|        |        |        |         | EBI_ALE      | O    | MFP2  | EBI address latch enable output pin.             |
|        |        |        |         | SPI2_MOSI    | I/O  | MFP4  | SPI2 MOSI (Master Out, Slave In) pin.            |
|        |        |        |         | UART1_RXD    | I    | MFP7  | UART1 data receiver input pin.                   |
|        |        |        |         | UART7_RXD    | I    | MFP8  | UART7 data receiver input pin.                   |
|        |        |        |         | BPWM0_CH3    | I/O  | MFP9  | BPWM0 channel 3 output/capture input.            |
|        |        |        |         | QE11_B       | I    | MFP10 | Quadrature encoder 1 phase B input               |
|        |        |        |         | ECAP0_IC2    | I    | MFP11 | Enhanced capture unit 0 input 2 pin.             |
|        |        |        |         | TM3_EXT      | I/O  | MFP13 | Timer3 external capture input/toggle output pin. |
|        |        |        |         | INT4         | I    | MFP15 | External interrupt 4 input pin.                  |
|        |        |        | 17      | PC.13        | I/O  | MFP0  | General purpose digital I/O pin.                 |
|        |        |        |         | EADC1_CH3    | A    | MFP1  | EADC1 channel 3 analog input.                    |
|        |        |        |         | EBI_ADR10    | O    | MFP2  | EBI address bus bit 10.                          |
|        |        |        |         | SPI2_I2SMCLK | I/O  | MFP4  | SPI2 I <sup>2</sup> S master clock output pin    |
|        |        |        |         | CAN1_TXD     | O    | MFP5  | CAN1 bus transmitter output.                     |
|        |        |        |         | UART2_TXD    | O    | MFP7  | UART2 data transmitter output pin.               |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name                | Type | MFP   | Description                                   |
|--------|--------|--------|---------|-------------------------|------|-------|---|
|        |        |        |         | BPWM0_CH4               | I/O  | MFP9  | BPWM0 channel 4 output/capture input.         |
|        |        |        |         | CLKO                    | O    | MFP13 | Clock Out                                     |
|        |        |        |         | EADC0_ST                | I    | MFP14 | EADC0 external trigger input.                 |
|        |        |        | 18      | PD.12                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EADC1_CH2               | A    | MFP1  | EADC1 channel 2 analog input.                 |
|        |        |        |         | EBI_nCS0                | O    | MFP2  | EBI chip select 0 output pin.                 |
|        |        |        |         | CAN1_RXD                | I    | MFP5  | CAN1 bus receiver input.                      |
|        |        |        |         | UART2_RXD               | I    | MFP7  | UART2 data receiver input pin.                |
|        |        |        |         | BPWM0_CH5               | I/O  | MFP9  | BPWM0 channel 5 output/capture input.         |
|        |        |        |         | QEIO_INDEX              | I    | MFP10 | Quadrature encoder 0 index input              |
|        |        |        |         | CLKO                    | O    | MFP13 | Clock Out                                     |
|        |        |        |         | EADC0_ST                | I    | MFP14 | EADC0 external trigger input.                 |
|        |        |        |         | INT5                    | I    | MFP15 | External interrupt 5 input pin.               |
|        |        |        | 19      | PD.11                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EADC1_CH1               | A    | MFP1  | EADC1 channel 1 analog input.                 |
|        |        |        |         | EBI_nCS1                | O    | MFP2  | EBI chip select 1 output pin.                 |
|        |        |        |         | UART1_TXD               | O    | MFP3  | UART1 data transmitter output pin.            |
|        |        |        |         | CAN0_TXD                | O    | MFP4  | CAN0 bus transmitter output.                  |
|        |        |        |         | QEIO_A                  | I    | MFP10 | Quadrature encoder 0 phase A input            |
|        |        |        |         | INT6                    | I    | MFP15 | External interrupt 6 input pin.               |
|        |        |        | 20      | PD.10                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EADC1_CH0               | A    | MFP1  | EADC1 channel 0 analog input.                 |
|        |        |        |         | EBI_nCS2                | O    | MFP2  | EBI chip select 2 output pin.                 |
|        |        |        |         | UART1_RXD               | I    | MFP3  | UART1 data receiver input pin.                |
|        |        |        |         | CAN0_RXD                | I    | MFP4  | CAN0 bus receiver input.                      |
|        |        |        |         | QEIO_B                  | I    | MFP10 | Quadrature encoder 0 phase B input            |
|        |        |        |         | INT7                    | I    | MFP15 | External interrupt 7 input pin.               |
|        |        |        | 21      | PG.2                    | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EBI_ADR11               | O    | MFP2  | EBI address bus bit 11.                       |
|        |        |        |         | SPI2_SS                 | I/O  | MFP3  | SPI2 slave select pin.                        |
|        |        |        |         | I <sup>2</sup> C0_SMBAL | O    | MFP4  | I <sup>2</sup> C0 SMBus SMBALTER pin          |
|        |        |        |         | I <sup>2</sup> C1_SCL   | I/O  | MFP5  | I <sup>2</sup> C1 clock pin.                  |
|        |        |        |         | CCAP_DATA7              | I    | MFP7  | Camera capture data input bus bit 7.          |
|        |        |        |         | TM0                     | I/O  | MFP13 | Timer0 event counter input/toggle output pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name                 | Type | MFP   | Description  |
|--------|--------|--------|---------|--------------------------|------|-------|--|
|        |        |        | 22      | PG.3                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_ADR12                | O    | MFP2  | EBI address bus bit 12.                                |
|        |        |        |         | SPI2_CLK                 | I/O  | MFP3  | SPI2 serial clock pin.                                 |
|        |        |        |         | I <sup>2</sup> C0_SMBSUS | O    | MFP4  | I <sup>2</sup> C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
|        |        |        |         | I <sup>2</sup> C1_SDA    | I/O  | MFP5  | I <sup>2</sup> C1 data input/output pin.               |
|        |        |        |         | CCAP_DATA6               | I    | MFP7  | Camera capture data input bus bit 6.                   |
|        |        |        |         | TM1                      | I/O  | MFP13 | Timer1 event counter input/toggle output pin.          |
|        |        |        | 23      | PG.4                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_ADR13                | O    | MFP2  | EBI address bus bit 13.                                |
|        |        |        |         | SPI2_MISO                | I/O  | MFP3  | SPI2 MISO (Master In, Slave Out) pin.                  |
|        |        |        |         | CCAP_DATA5               | I    | MFP7  | Camera capture data input bus bit 5.                   |
|        |        |        |         | TM2                      | I/O  | MFP13 | Timer2 event counter input/toggle output pin.          |
|        |        |        | 24      | PF.11                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_ADR14                | O    | MFP2  | EBI address bus bit 14.                                |
|        |        |        |         | SPI2_MOSI                | I/O  | MFP3  | SPI2 MOSI (Master Out, Slave In) pin.                  |
|        |        |        |         | UART5_TXD                | O    | MFP6  | UART5 data transmitter output pin.                     |
|        |        |        |         | CCAP_DATA4               | I    | MFP7  | Camera capture data input bus bit 4.                   |
|        |        |        |         | TM3                      | I/O  | MFP13 | Timer3 event counter input/toggle output pin.          |
|        |        |        | 25      | PF.10                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_ADR15                | O    | MFP2  | EBI address bus bit 15.                                |
|        |        |        |         | SC0_nCD                  | I    | MFP3  | Smart Card 0 card detect pin.                          |
|        |        |        |         | I <sup>2</sup> S0_BCLK   | O    | MFP4  | I <sup>2</sup> S0 bit clock output pin.                |
|        |        |        |         | SPI0_I2SMCLK             | I/O  | MFP5  | SPI0 I <sup>2</sup> S master clock output pin          |
|        |        |        |         | UART5_RXD                | I    | MFP6  | UART5 data receiver input pin.                         |
|        |        |        |         | CCAP_DATA3               | I    | MFP7  | Camera capture data input bus bit 3.                   |
|        |        |        | 26      | PF.9                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_ADR16                | O    | MFP2  | EBI address bus bit 16.                                |
|        |        |        |         | SC0_PWR                  | O    | MFP3  | Smart Card 0 power pin.                                |
|        |        |        |         | I <sup>2</sup> S0_MCLK   | O    | MFP4  | I <sup>2</sup> S0 master clock output pin.             |
|        |        |        |         | SPI0_SS                  | I/O  | MFP5  | SPI0 slave select pin.                                 |
|        |        |        |         | UART5_nRTS               | O    | MFP6  | UART5 request to Send output pin.                      |
|        |        |        |         | CCAP_DATA2               | I    | MFP7  | Camera capture data input bus bit 2.                   |
|        |        |        |         | CAN1_TXD                 | O    | MFP8  | CAN1 bus transmitter output.                           |
|        |        |        | 27      | PF.8                     | I/O  | MFP0  | General purpose digital I/O pin.                       |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name               | Type | MFP   | Description  |
|--------|--------|--------|---------|------------------------|------|-------|--|
|        |        |        |         | EBI_ADR17              | O    | MFP2  | EBI address bus bit 17.                                |
|        |        |        |         | SC0_RST                | O    | MFP3  | Smart Card 0 reset pin.                                |
|        |        |        |         | I <sup>2</sup> S0_DI   | I    | MFP4  | I <sup>2</sup> S0 data input pin.                      |
|        |        |        |         | SPI0_CLK               | I/O  | MFP5  | SPI0 serial clock pin.                                 |
|        |        |        |         | UART5_nCTS             | I    | MFP6  | UART5 clear to Send input pin.                         |
|        |        |        |         | CCAP_DATA1             | I    | MFP7  | Camera capture data input bus bit 1.                   |
|        |        |        |         | CAN1_RXD               | I    | MFP8  | CAN1 bus receiver input.                               |
|        |        |        |         | TAMPER2                | I/O  | MFP10 | TAMPER detector loop pin 2.                            |
|        |        |        | 28      | PF.7                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_ADR18              | O    | MFP2  | EBI address bus bit 18.                                |
|        |        |        |         | SC0_DAT                | I/O  | MFP3  | Smart Card 0 data pin.                                 |
|        |        |        |         | I <sup>2</sup> S0_DO   | O    | MFP4  | I <sup>2</sup> S0 data output pin.                     |
|        |        |        |         | SPI0_MISO              | I/O  | MFP5  | SPI0 MISO (Master In, Slave Out) pin.                  |
|        |        |        |         | UART4_TXD              | O    | MFP6  | UART4 data transmitter output pin.                     |
|        |        |        |         | CCAP_DATA0             | I    | MFP7  | Camera capture data input bus bit 0.                   |
|        |        |        |         | CAN2_TXD               | O    | MFP8  | CAN2 bus transmitter output.                           |
|        |        |        |         | TAMPER1                | I/O  | MFP10 | TAMPER detector loop pin 1.                            |
|        |        | 12     | 29      | PF.6                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_ADR19              | O    | MFP2  | EBI address bus bit 19.                                |
|        |        |        |         | SC0_CLK                | O    | MFP3  | Smart Card 0 clock pin.                                |
|        |        |        |         | I <sup>2</sup> S0_LRCK | O    | MFP4  | I <sup>2</sup> S0 left right channel clock output pin. |
|        |        |        |         | SPI0_MOSI              | I/O  | MFP5  | SPI0 MOSI (Master Out, Slave In) pin.                  |
|        |        |        |         | UART4_RXD              | I    | MFP6  | UART4 data receiver input pin.                         |
|        |        |        |         | EBI_nCS0               | O    | MFP7  | EBI chip select 0 output pin.                          |
|        |        |        |         | CAN2_RXD               | I    | MFP8  | CAN2 bus receiver input.                               |
|        |        |        |         | TAMPER0                | I/O  | MFP10 | TAMPER detector loop pin 0.                            |
|        |        | 13     | 30      | V <sub>BAT</sub>       | P    | MFP0  | Power supply by batteries for RTC.                     |
| 7      | 11     | 14     | 31      | PF.5                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | UART2_RXD              | I    | MFP2  | UART2 data receiver input pin.                         |
|        |        |        |         | UART2_nCTS             | I    | MFP4  | UART2 clear to Send input pin.                         |
|        |        |        |         | EPWM0_CH0              | I/O  | MFP7  | EPWM0 channel 0 output/capture input.                  |
|        |        |        |         | BPWM0_CH4              | I/O  | MFP8  | BPWM0 channel 4 output/capture input.                  |
|        |        |        |         | EPWM0_SYNC_OUT         | O    | MFP9  | EPWM0 counter synchronous trigger output pin.          |
|        |        |        |         | X32_IN                 | I    | MFP10 | External 32.768 kHz crystal input pin.                 |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name              | Type | MFP   | Description                                       |
|--------|--------|--------|---------|-----------------------|------|-------|---|
|        |        |        |         | EADC0_ST              | I    | MFP11 | EADC0 external trigger input.                     |
| 8      | 12     | 15     | 32      | PF.4                  | I/O  | MFP0  | General purpose digital I/O pin.                  |
|        |        |        |         | UART2_TXD             | O    | MFP2  | UART2 data transmitter output pin.                |
|        |        |        |         | UART2_nRTS            | O    | MFP4  | UART2 request to Send output pin.                 |
|        |        |        |         | EPWM0_CH1             | I/O  | MFP7  | EPWM0 channel 1 output/capture input.             |
|        |        |        |         | BPWM0_CH5             | I/O  | MFP8  | BPWM0 channel 5 output/capture input.             |
|        |        |        |         | X32_OUT               | O    | MFP10 | External 32.768 kHz crystal output pin.           |
|        |        |        |         | EADC1_ST              | I    | MFP11 | EADC1 external trigger input.                     |
|        |        |        | 33      | PH.4                  | I/O  | MFP0  | General purpose digital I/O pin.                  |
|        |        |        |         | EBI_ADR3              | O    | MFP2  | EBI address bus bit 3.                            |
|        |        |        |         | SPI1_MISO             | I/O  | MFP3  | SPI1 MISO (Master In, Slave Out) pin.             |
|        |        |        |         | UART7_nRTS            | O    | MFP4  | UART7 request to Send output pin.                 |
|        |        |        |         | UART6_TXD             | O    | MFP5  | UART6 data transmitter output pin.                |
|        |        |        | 34      | PH.5                  | I/O  | MFP0  | General purpose digital I/O pin.                  |
|        |        |        |         | EBI_ADR2              | O    | MFP2  | EBI address bus bit 2.                            |
|        |        |        |         | SPI1_MOSI             | I/O  | MFP3  | SPI1 MOSI (Master Out, Slave In) pin.             |
|        |        |        |         | UART7_nCTS            | I    | MFP4  | UART7 clear to Send input pin.                    |
|        |        |        |         | UART6_RXD             | I    | MFP5  | UART6 data receiver input pin.                    |
|        |        |        | 35      | PH.6                  | I/O  | MFP0  | General purpose digital I/O pin.                  |
|        |        |        |         | EBI_ADR1              | O    | MFP2  | EBI address bus bit 1.                            |
|        |        |        |         | SPI1_CLK              | I/O  | MFP3  | SPI1 serial clock pin.                            |
|        |        |        |         | UART7_TXD             | O    | MFP4  | UART7 data transmitter output pin.                |
|        |        |        | 36      | PH.7                  | I/O  | MFP0  | General purpose digital I/O pin.                  |
|        |        |        |         | EBI_ADR0              | O    | MFP2  | EBI address bus bit 0.                            |
|        |        |        |         | SPI1_SS               | I/O  | MFP3  | SPI1 slave select pin.                            |
|        |        |        |         | UART7_RXD             | I    | MFP4  | UART7 data receiver input pin.                    |
| 9      | 13     | 16     | 37      | PF.3                  | I/O  | MFP0  | General purpose digital I/O pin.                  |
|        |        |        |         | EBI_nCS0              | O    | MFP2  | EBI chip select 0 output pin.                     |
|        |        |        |         | UART0_TXD             | O    | MFP3  | UART0 data transmitter output pin.                |
|        |        |        |         | I <sup>2</sup> C0_SCL | I/O  | MFP4  | I <sup>2</sup> C0 clock pin.                      |
|        |        |        |         | XT1_IN                | I    | MFP10 | External 4~24 MHz (high speed) crystal input pin. |
|        |        |        |         | BPWM1_CH0             | I/O  | MFP11 | BPWM1 channel 0 output/capture input.             |
| 10     | 14     | 17     | 38      | PF.2                  | I/O  | MFP0  | General purpose digital I/O pin.                  |
|        |        |        |         | EBI_nCS1              | O    | MFP2  | EBI chip select 1 output pin.                     |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name               | Type | MFP   | Description   |
|--------|--------|--------|---------|------------------------|------|-------|---|
|        |        |        |         | UART0_RXD              | I    | MFP3  | UART0 data receiver input pin.  |
|        |        |        |         | I <sup>2</sup> C0_SDA  | I/O  | MFP4  | I <sup>2</sup> C0 data input/output pin.  |
|        |        |        |         | QSPI0_CLK              | I/O  | MFP5  | Quad SPI0 serial clock pin.   |
|        |        |        |         | XT1_OUT                | O    | MFP10 | External 4~24 MHz (high speed) crystal output pin.                              |
|        |        |        |         | BPWM1_CH1              | I/O  | MFP11 | BPWM1 channel 1 output/capture input.   |
|        |        |        | 39      | V <sub>SS</sub>        | P    | MFP0  | Ground pin for digital circuit.   |
|        |        |        | 40      | V <sub>DD</sub>        | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
|        |        |        | 41      | PE.8                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EBI_ADR10              | O    | MFP2  | EBI address bus bit 10.   |
|        |        |        |         | I <sup>2</sup> S0_BCLK | O    | MFP4  | I <sup>2</sup> S0 bit clock output pin.   |
|        |        |        |         | SPI2_CLK               | I/O  | MFP5  | SPI2 serial clock pin.  |
|        |        |        |         | UART2_TXD              | O    | MFP7  | UART2 data transmitter output pin.  |
|        |        |        |         | EPWM0_CH0              | I/O  | MFP10 | EPWM0 channel 0 output/capture input.   |
|        |        |        |         | EPWM0_BRAKE0           | I    | MFP11 | EPWM0 Brake 0 input pin.  |
|        |        |        |         | ECAP0_IC0              | I    | MFP12 | Enhanced capture unit 0 input 0 pin.  |
|        |        |        |         | TRACE_DATA3            | O    | MFP14 | ETM Trace Data 3 output pin   |
|        |        |        | 42      | PE.9                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EBI_ADR11              | O    | MFP2  | EBI address bus bit 11.   |
|        |        |        |         | I <sup>2</sup> S0_MCLK | O    | MFP4  | I <sup>2</sup> S0 master clock output pin.                                      |
|        |        |        |         | SPI2_MISO              | I/O  | MFP5  | SPI2 MISO (Master In, Slave Out) pin.   |
|        |        |        |         | UART2_RXD              | I    | MFP7  | UART2 data receiver input pin.  |
|        |        |        |         | EPWM0_CH1              | I/O  | MFP10 | EPWM0 channel 1 output/capture input.   |
|        |        |        |         | EPWM0_BRAKE1           | I    | MFP11 | EPWM0 Brake 1 input pin.  |
|        |        |        |         | ECAP0_IC1              | I    | MFP12 | Enhanced capture unit 0 input 1 pin.  |
|        |        |        |         | TRACE_DATA2            | O    | MFP14 | ETM Trace Data 2 output pin   |
|        |        |        | 43      | PE.10                  | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EBI_ADR12              | O    | MFP2  | EBI address bus bit 12.   |
|        |        |        |         | I <sup>2</sup> S0_DI   | I    | MFP4  | I <sup>2</sup> S0 data input pin.   |
|        |        |        |         | SPI2_MOSI              | I/O  | MFP5  | SPI2 MOSI (Master Out, Slave In) pin.   |
|        |        |        |         | UART3_TXD              | O    | MFP7  | UART3 data transmitter output pin.  |
|        |        |        |         | EPWM0_CH2              | I/O  | MFP10 | EPWM0 channel 2 output/capture input.   |
|        |        |        |         | EPWM1_BRAKE0           | I    | MFP11 | EPWM1 Brake 0 input pin.  |
|        |        |        |         | ECAP0_IC2              | I    | MFP12 | Enhanced capture unit 0 input 2 pin.  |



| 32 Pin | 48 Pin | 64 Pin | 128 Pin     | Pin Name               | Type  | MFP                         | Description  |
|--------|--------|--------|-------------|------------------------|-------|-----------------------------|--|
|        |        |        |             | TRACE_DATA1            | O     | MFP14                       | ETM Trace Data 1 output pin                            |
|        |        |        | 44          | PE.11                  | I/O   | MFP0                        | General purpose digital I/O pin.                       |
|        |        |        |             | EBI_ADR13              | O     | MFP2                        | EBI address bus bit 13.                                |
|        |        |        |             | I <sup>2</sup> S0_DO   | O     | MFP4                        | I <sup>2</sup> S0 data output pin.                     |
|        |        |        |             | SPI2_SS                | I/O   | MFP5                        | SPI2 slave select pin.                                 |
|        |        |        |             | UART3_RXD              | I     | MFP7                        | UART3 data receiver input pin.                         |
|        |        |        |             | UART1_nCTS             | I     | MFP8                        | UART1 clear to Send input pin.                         |
|        |        |        |             | EPWM0_CH3              | I/O   | MFP10                       | EPWM0 channel 3 output/capture input.                  |
|        |        |        |             | EPWM1_BRAKE1           | I     | MFP11                       | EPWM1 Brake 1 input pin.                               |
|        |        |        |             | ECAP1_IC2              | I     | MFP13                       | Enhanced capture unit 1 input 2 pin.                   |
|        |        |        | TRACE_DATA0 | O                      | MFP14 | ETM Trace Data 0 output pin |  |
|        |        |        | 45          | PE.12                  | I/O   | MFP0                        | General purpose digital I/O pin.                       |
|        |        |        |             | EBI_ADR14              | O     | MFP2                        | EBI address bus bit 14.                                |
|        |        |        |             | I <sup>2</sup> S0_LRCK | O     | MFP4                        | I <sup>2</sup> S0 left right channel clock output pin. |
|        |        |        |             | SPI2_I2SMCLK           | I/O   | MFP5                        | SPI2 I <sup>2</sup> S master clock output pin          |
|        |        |        |             | UART1_nRTS             | O     | MFP8                        | UART1 request to Send output pin.                      |
|        |        |        |             | EPWM0_CH4              | I/O   | MFP10                       | EPWM0 channel 4 output/capture input.                  |
|        |        |        |             | ECAP1_IC1              | I     | MFP13                       | Enhanced capture unit 1 input 1 pin.                   |
|        |        |        |             | TRACE_CLK              | O     | MFP14                       | ETM Trace Clock output pin                             |
|        |        |        | 46          | PE.13                  | I/O   | MFP0                        | General purpose digital I/O pin.                       |
|        |        |        |             | EBI_ADR15              | O     | MFP2                        | EBI address bus bit 15.                                |
|        |        |        |             | I <sup>2</sup> C0_SCL  | I/O   | MFP4                        | I <sup>2</sup> C0 clock pin.                           |
|        |        |        |             | UART4_nRTS             | O     | MFP5                        | UART4 request to Send output pin.                      |
|        |        |        |             | UART1_TXD              | O     | MFP8                        | UART1 data transmitter output pin.                     |
|        |        |        |             | EPWM0_CH5              | I/O   | MFP10                       | EPWM0 channel 5 output/capture input.                  |
|        |        |        |             | EPWM1_CH0              | I/O   | MFP11                       | EPWM1 channel 0 output/capture input.                  |
|        |        |        |             | BPWM1_CH5              | I/O   | MFP12                       | BPWM1 channel 5 output/capture input.                  |
|        |        |        |             | ECAP1_IC0              | I     | MFP13                       | Enhanced capture unit 1 input 0 pin.                   |
|        |        |        | 47          | PC.8                   | I/O   | MFP0                        | General purpose digital I/O pin.                       |
|        |        |        |             | EBI_ADR16              | O     | MFP2                        | EBI address bus bit 16.                                |
|        |        |        |             | I <sup>2</sup> C0_SDA  | I/O   | MFP4                        | I <sup>2</sup> C0 data input/output pin.               |
|        |        |        |             | UART4_nCTS             | I     | MFP5                        | UART4 clear to Send input pin.                         |
|        |        |        |             | UART1_RXD              | I     | MFP8                        | UART1 data receiver input pin.                         |
|        |        |        |             | EPWM1_CH1              | I/O   | MFP11                       | EPWM1 channel 1 output/capture input.                  |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name                 | Type | MFP   | Description  |
|--------|--------|--------|---------|--------------------------|------|-------|--|
|        |        |        |         | BPWM1_CH4                | I/O  | MFP12 | BPWM1 channel 4 output/capture input.                  |
|        |        | 18     | 48      | PC.7                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_AD9                  | I/O  | MFP2  | EBI address/data bus bit 9.                            |
|        |        |        |         | SPI1_MISO                | I/O  | MFP4  | SPI1 MISO (Master In, Slave Out) pin.                  |
|        |        |        |         | UART4_TXD                | O    | MFP5  | UART4 data transmitter output pin.                     |
|        |        |        |         | UART0_nCTS               | I    | MFP7  | UART0 clear to Send input pin.                         |
|        |        |        |         | I <sup>2</sup> C1_SMBAL  | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBALTER pin                   |
|        |        |        |         | UART6_TXD                | O    | MFP9  | UART6 data transmitter output pin.                     |
|        |        |        |         | EPWM1_CH2                | I/O  | MFP11 | EPWM1 channel 2 output/capture input.                  |
|        |        |        |         | BPWM1_CH0                | I/O  | MFP12 | BPWM1 channel 0 output/capture input.                  |
|        |        |        |         | TM0                      | I/O  | MFP14 | Timer0 event counter input/toggle output pin.          |
|        |        |        |         | INT3                     | I    | MFP15 | External interrupt 3 input pin.                        |
|        |        | 19     | 49      | PC.6                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_AD8                  | I/O  | MFP2  | EBI address/data bus bit 8.                            |
|        |        |        |         | SPI1_MOSI                | I/O  | MFP4  | SPI1 MOSI (Master Out, Slave In) pin.                  |
|        |        |        |         | UART4_RXD                | I    | MFP5  | UART4 data receiver input pin.                         |
|        |        |        |         | UART0_nRTS               | O    | MFP7  | UART0 request to Send output pin.                      |
|        |        |        |         | I <sup>2</sup> C1_SMBSUS | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
|        |        |        |         | UART6_RXD                | I    | MFP9  | UART6 data receiver input pin.                         |
|        |        |        |         | EPWM1_CH3                | I/O  | MFP11 | EPWM1 channel 3 output/capture input.                  |
|        |        |        |         | BPWM1_CH1                | I/O  | MFP12 | BPWM1 channel 1 output/capture input.                  |
|        |        |        |         | TM1                      | I/O  | MFP14 | Timer1 event counter input/toggle output pin.          |
|        |        |        |         | INT2                     | I    | MFP15 | External interrupt 2 input pin.                        |
|        | 15     | 20     | 50      | PA.7                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_AD7                  | I/O  | MFP2  | EBI address/data bus bit 7.                            |
|        |        |        |         | SPI1_CLK                 | I/O  | MFP4  | SPI1 serial clock pin.                                 |
|        |        |        |         | UART0_TXD                | O    | MFP7  | UART0 data transmitter output pin.                     |
|        |        |        |         | I <sup>2</sup> C1_SCL    | I/O  | MFP8  | I <sup>2</sup> C1 clock pin.                           |
|        |        |        |         | QSPI1_MISO1              | I/O  | MFP9  | Quad SPI1 MISO1 (Master In, Slave Out) pin.            |
|        |        |        |         | EPWM1_CH4                | I/O  | MFP11 | EPWM1 channel 4 output/capture input.                  |
|        |        |        |         | BPWM1_CH2                | I/O  | MFP12 | BPWM1 channel 2 output/capture input.                  |
|        |        |        |         | ACMP0_WLAT               | I    | MFP13 | Analog comparator 0 window latch input pin             |
|        |        |        |         | TM2                      | I/O  | MFP14 | Timer2 event counter input/toggle output pin.          |
|        |        |        |         | INT1                     | I    | MFP15 | External interrupt 1 input pin.                        |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name              | Type | MFP   | Description  |
|--------|--------|--------|---------|-----------------------|------|-------|--|
|        | 16     | 21     | 51      | PA.6                  | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |        |        |         | EBI_AD6               | I/O  | MFP2  | EBI address/data bus bit 6.  |
|        |        |        |         | SPI1_SS               | I/O  | MFP4  | SPI1 slave select pin.   |
|        |        |        |         | UART0_RXD             | I    | MFP7  | UART0 data receiver input pin.   |
|        |        |        |         | I <sup>2</sup> C1_SDA | I/O  | MFP8  | I <sup>2</sup> C1 data input/output pin.   |
|        |        |        |         | QSPI1_MOSI1           | I/O  | MFP9  | Quad SPI1 MOSI1 (Master Out, Slave In) pin.  |
|        |        |        |         | EPWM1_CH5             | I/O  | MFP11 | EPWM1 channel 5 output/capture input.  |
|        |        |        |         | BPWM1_CH3             | I/O  | MFP12 | BPWM1 channel 3 output/capture input.  |
|        |        |        |         | ACMP1_WLAT            | I    | MFP13 | Analog comparator 1 window latch input pin   |
|        |        |        |         | TM3                   | I/O  | MFP14 | Timer3 event counter input/toggle output pin.  |
|        |        |        |         | INT0                  | I    | MFP15 | External interrupt 0 input pin.  |
|        |        | 22     | 52      | V <sub>SS</sub>       | P    | MFP0  | Ground pin for digital circuit.  |
|        |        | 23     | 53      | V <sub>DD</sub>       | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit.            |
|        |        | 24     | 54      | LDO_CAP               | A    | MFP0  | LDO output pin.<br><b>Note:</b> This pin needs to be connected with an external capacitor. |
|        | 17     | 25     | 55      | PA.5                  | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |        |        |         | QSPI0_MISO1           | I/O  | MFP3  | Quad SPI0 MISO1 (Master In, Slave Out) pin.  |
|        |        |        |         | SPI1_I2SMCLK          | I/O  | MFP4  | SPI1 I <sup>2</sup> S master clock output pin  |
|        |        |        |         | UART0_nCTS            | I    | MFP7  | UART0 clear to Send input pin.   |
|        |        |        |         | UART5_TXD             | O    | MFP8  | UART5 data transmitter output pin.   |
|        |        |        |         | I <sup>2</sup> C0_SCL | I/O  | MFP9  | I <sup>2</sup> C0 clock pin.   |
|        |        |        |         | CAN0_TXD              | O    | MFP10 | CAN0 bus transmitter output.   |
|        |        |        |         | UART0_TXD             | O    | MFP11 | UART0 data transmitter output pin.   |
|        |        |        |         | BPWM0_CH5             | I/O  | MFP12 | BPWM0 channel 5 output/capture input.  |
|        |        |        |         | EPWM0_CH0             | I/O  | MFP13 | EPWM0 channel 0 output/capture input.  |
|        |        |        |         | QEIO_INDEX            | I    | MFP14 | Quadrature encoder 0 index input   |
|        | 18     | 26     | 56      | PA.4                  | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |        |        |         | QSPI0_MOSI1           | I/O  | MFP3  | Quad SPI0 MOSI1 (Master Out, Slave In) pin.  |
|        |        |        |         | SPI0_I2SMCLK          | I/O  | MFP4  | SPI0 I <sup>2</sup> S master clock output pin  |
|        |        |        |         | SC0_nCD               | I    | MFP6  | Smart Card 0 card detect pin.  |
|        |        |        |         | UART0_nRTS            | O    | MFP7  | UART0 request to Send output pin.  |
|        |        |        |         | UART5_RXD             | I    | MFP8  | UART5 data receiver input pin.   |
|        |        |        |         | I <sup>2</sup> C0_SDA | I/O  | MFP9  | I <sup>2</sup> C0 data input/output pin.   |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name                 | Type | MFP   | Description  |
|--------|--------|--------|---------|--------------------------|------|-------|--|
|        |        |        |         | CAN0_RXD                 | I    | MFP10 | CAN0 bus receiver input.                               |
|        |        |        |         | UART0_RXD                | I    | MFP11 | UART0 data receiver input pin.                         |
|        |        |        |         | BPWM0_CH4                | I/O  | MFP12 | BPWM0 channel 4 output/capture input.                  |
|        |        |        |         | EPWM0_CH1                | I/O  | MFP13 | EPWM0 channel 1 output/capture input.                  |
|        |        |        |         | QEIO_A                   | I    | MFP14 | Quadrature encoder 0 phase A input                     |
| 11     | 19     | 27     | 57      | PA.3                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | QSPIO_SS                 | I/O  | MFP3  | Quad SPI0 slave select pin.                            |
|        |        |        |         | SPIO_SS                  | I/O  | MFP4  | SPIO slave select pin.                                 |
|        |        |        |         | SC0_PWR                  | O    | MFP6  | Smart Card 0 power pin.                                |
|        |        |        |         | UART4_TXD                | O    | MFP7  | UART4 data transmitter output pin.                     |
|        |        |        |         | UART1_TXD                | O    | MFP8  | UART1 data transmitter output pin.                     |
|        |        |        |         | I <sup>2</sup> C1_SCL    | I/O  | MFP9  | I <sup>2</sup> C1 clock pin.                           |
|        |        |        |         | I <sup>2</sup> C0_SMBAL  | O    | MFP10 | I <sup>2</sup> C0 SMBus SMBALTER pin                   |
|        |        |        |         | BPWM0_CH3                | I/O  | MFP12 | BPWM0 channel 3 output/capture input.                  |
|        |        |        |         | EPWM0_CH2                | I/O  | MFP13 | EPWM0 channel 2 output/capture input.                  |
|        |        |        |         | QEIO_B                   | I    | MFP14 | Quadrature encoder 0 phase B input                     |
|        |        |        |         | EPWM1_BRAKE1             | I    | MFP15 | EPWM1 Brake 1 input pin.                               |
| 12     | 20     | 28     | 58      | PA.2                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | QSPIO_CLK                | I/O  | MFP3  | Quad SPI0 serial clock pin.                            |
|        |        |        |         | SPIO_CLK                 | I/O  | MFP4  | SPIO serial clock pin.                                 |
|        |        |        |         | SC0_RST                  | O    | MFP6  | Smart Card 0 reset pin.                                |
|        |        |        |         | UART4_RXD                | I    | MFP7  | UART4 data receiver input pin.                         |
|        |        |        |         | UART1_RXD                | I    | MFP8  | UART1 data receiver input pin.                         |
|        |        |        |         | I <sup>2</sup> C1_SDA    | I/O  | MFP9  | I <sup>2</sup> C1 data input/output pin.               |
|        |        |        |         | I <sup>2</sup> C0_SMBSUS | O    | MFP10 | I <sup>2</sup> C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
|        |        |        |         | BPWM0_CH2                | I/O  | MFP12 | BPWM0 channel 2 output/capture input.                  |
|        |        |        |         | EPWM0_CH3                | I/O  | MFP13 | EPWM0 channel 3 output/capture input.                  |
| 13     | 21     | 29     | 59      | PA.1                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | QSPIO_MISO0              | I/O  | MFP3  | Quad SPI0 MISO0 (Master In, Slave Out) pin.            |
|        |        |        |         | SPIO_MISO                | I/O  | MFP4  | SPIO MISO (Master In, Slave Out) pin.                  |
|        |        |        |         | SC0_DAT                  | I/O  | MFP6  | Smart Card 0 data pin.                                 |
|        |        |        |         | UART0_TXD                | O    | MFP7  | UART0 data transmitter output pin.                     |
|        |        |        |         | UART1_nCTS               | I    | MFP8  | UART1 clear to Send input pin.                         |
|        |        |        |         | I <sup>2</sup> C2_SCL    | I/O  | MFP9  | I <sup>2</sup> C2 clock pin.                           |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name              | Type | MFP   | Description   |
|--------|--------|--------|---------|-----------------------|------|-------|---|
|        |        |        |         | CCAP_DATA7            | I    | MFP10 | Camera capture data input bus bit 7.  |
|        |        |        |         | BPWM0_CH1             | I/O  | MFP12 | BPWM0 channel 1 output/capture input.   |
|        |        |        |         | EPWM0_CH4             | I/O  | MFP13 | EPWM0 channel 4 output/capture input.   |
| 14     | 22     | 30     | 60      | PA.0                  | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | QSPI0_MOSI0           | I/O  | MFP3  | Quad SPI0 MOSI0 (Master Out, Slave In) pin.   |
|        |        |        |         | SPI0_MOSI             | I/O  | MFP4  | SPI0 MOSI (Master Out, Slave In) pin.   |
|        |        |        |         | SC0_CLK               | O    | MFP6  | Smart Card 0 clock pin.   |
|        |        |        |         | UART0_RXD             | I    | MFP7  | UART0 data receiver input pin.  |
|        |        |        |         | UART1_nRTS            | O    | MFP8  | UART1 request to Send output pin.   |
|        |        |        |         | I <sup>2</sup> C2_SDA | I/O  | MFP9  | I <sup>2</sup> C2 data input/output pin.  |
|        |        |        |         | CCAP_DATA6            | I    | MFP10 | Camera capture data input bus bit 6.  |
|        |        |        |         | BPWM0_CH0             | I/O  | MFP12 | BPWM0 channel 0 output/capture input.   |
|        |        |        |         | EPWM0_CH5             | I/O  | MFP13 | EPWM0 channel 5 output/capture input.   |
|        |        |        |         | DAC0_ST               | I    | MFP15 | DAC0 external trigger input.  |
| 15     | 23     | 31     | 61      | V <sub>DDIO</sub>     | P    | MFP0  | Power supply for PA.0~PA.5.   |
|        |        |        | 62      | PE.14                 | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EBI_AD8               | I/O  | MFP2  | EBI address/data bus bit 8.   |
|        |        |        |         | UART2_TXD             | O    | MFP3  | UART2 data transmitter output pin.  |
|        |        |        |         | CAN0_TXD              | O    | MFP4  | CAN0 bus transmitter output.  |
|        |        |        |         | UART6_TXD             | O    | MFP6  | UART6 data transmitter output pin.  |
|        |        |        | 63      | PE.15                 | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EBI_AD9               | I/O  | MFP2  | EBI address/data bus bit 9.   |
|        |        |        |         | UART2_RXD             | I    | MFP3  | UART2 data receiver input pin.  |
|        |        |        |         | CAN0_RXD              | I    | MFP4  | CAN0 bus receiver input.  |
|        |        |        |         | UART6_RXD             | I    | MFP6  | UART6 data receiver input pin.  |
| 16     | 24     | 32     | 64      | nRESET                | I    | MFP0  | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.<br><b>Note:</b> It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin. |
| 17     | 25     | 33     | 65      | PF.0                  | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | UART1_TXD             | O    | MFP2  | UART1 data transmitter output pin.  |
|        |        |        |         | I <sup>2</sup> C1_SCL | I/O  | MFP3  | I <sup>2</sup> C1 clock pin.  |
|        |        |        |         | UART0_TXD             | O    | MFP4  | UART0 data transmitter output pin.  |
|        |        |        |         | BPWM1_CH0             | I/O  | MFP12 | BPWM1 channel 0 output/capture input.   |
|        |        |        |         | ICE_DAT               | I/O  | MFP14 | Serial wired debugger data pin.<br><b>Note:</b> It is recommended to use 100 kΩ pull-up resistor on   |

| 32 Pin   | 48 Pin | 64 Pin | 128 Pin                     | Pin Name               | Type | MFP   | Description   |
|----------|--------|--------|-----------------------------|------------------------|------|-------|---|
|          |        |        |                             |                        |      |       | ICE_DAT pin.  |
| 18       | 26     | 34     | 66                          | PF.1                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|          |        |        |                             | UART1_RXD              | I    | MFP2  | UART1 data receiver input pin.  |
|          |        |        |                             | I <sup>2</sup> C1_SDA  | I/O  | MFP3  | I <sup>2</sup> C1 data input/output pin.  |
|          |        |        |                             | UART0_RXD              | I    | MFP4  | UART0 data receiver input pin.  |
|          |        |        |                             | BPWM1_CH1              | I/O  | MFP12 | BPWM1 channel 1 output/capture input.   |
|          |        |        |                             | ICE_CLK                | I/O  | MFP14 | Serial wired debugger clock pin.<br><b>Note:</b> It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin. |
|          |        |        | 67                          | PD.9                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|          |        |        |                             | EBI_AD7                | I/O  | MFP2  | EBI address/data bus bit 7.   |
|          |        |        |                             | I <sup>2</sup> C2_SCL  | I/O  | MFP3  | I <sup>2</sup> C2 clock pin.  |
|          |        |        |                             | UART2_nCTS             | I    | MFP4  | UART2 clear to Send input pin.  |
|          |        |        |                             | UART7_TXD              | O    | MFP5  | UART7 data transmitter output pin.  |
|          |        |        |                             | CAN2_TXD               | O    | MFP6  | CAN2 bus transmitter output.  |
|          |        |        | 68                          | PD.8                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|          |        |        |                             | EBI_AD6                | I/O  | MFP2  | EBI address/data bus bit 6.   |
|          |        |        |                             | I <sup>2</sup> C2_SDA  | I/O  | MFP3  | I <sup>2</sup> C2 data input/output pin.  |
|          |        |        |                             | UART2_nRTS             | O    | MFP4  | UART2 request to Send output pin.   |
|          |        |        |                             | UART7_RXD              | I    | MFP5  | UART7 data receiver input pin.  |
|          |        |        |                             | CAN2_RXD               | I    | MFP6  | CAN2 bus receiver input.  |
|          | 27     | 35     | 69                          | PC.5                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|          |        |        |                             | EBI_AD5                | I/O  | MFP2  | EBI address/data bus bit 5.   |
|          |        |        |                             | QSPIO_MISO1            | I/O  | MFP4  | Quad SPI0 MISO1 (Master In, Slave Out) pin.   |
|          |        |        |                             | UART2_TXD              | O    | MFP8  | UART2 data transmitter output pin.  |
|          |        |        |                             | I <sup>2</sup> C1_SCL  | I/O  | MFP9  | I <sup>2</sup> C1 clock pin.  |
|          |        |        |                             | CAN0_TXD               | O    | MFP10 | CAN0 bus transmitter output.  |
|          |        |        |                             | UART4_TXD              | O    | MFP11 | UART4 data transmitter output pin.  |
|          |        |        |                             | EPWM1_CH0              | I/O  | MFP12 | EPWM1 channel 0 output/capture input.   |
|          |        |        |                             | CCAP_DATA5             | I    | MFP13 | Camera capture data input bus bit 5.  |
| QSPI1_SS | I/O    | MFP14  | Quad SPI1 slave select pin. |                        |      |       |   |
|          | 28     | 36     | 70                          | PC.4                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|          |        |        |                             | EBI_AD4                | I/O  | MFP2  | EBI address/data bus bit 4.   |
|          |        |        |                             | QSPIO_MOSI1            | I/O  | MFP4  | Quad SPI0 MOSI1 (Master Out, Slave In) pin.   |
|          |        |        |                             | I <sup>2</sup> S0_BCLK | O    | MFP6  | I <sup>2</sup> S0 bit clock output pin.   |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name                 | Type | MFP   | Description  |
|--------|--------|--------|---------|--------------------------|------|-------|--|
|        |        |        |         | SPI1_I2SMCLK             | I/O  | MFP7  | SPI1 I <sup>2</sup> S master clock output pin          |
|        |        |        |         | UART2_RXD                | I    | MFP8  | UART2 data receiver input pin.                         |
|        |        |        |         | I <sup>2</sup> C1_SDA    | I/O  | MFP9  | I <sup>2</sup> C1 data input/output pin.               |
|        |        |        |         | CAN0_RXD                 | I    | MFP10 | CAN0 bus receiver input.                               |
|        |        |        |         | UART4_RXD                | I    | MFP11 | UART4 data receiver input pin.                         |
|        |        |        |         | EPWM1_CH1                | I/O  | MFP12 | EPWM1 channel 1 output/capture input.                  |
|        |        |        |         | CCAP_DATA4               | I    | MFP13 | Camera capture data input bus bit 4.                   |
|        |        |        |         | QSPI1_CLK                | I/O  | MFP14 | Quad SPI1 serial clock pin.                            |
|        | 29     | 37     | 71      | PC.3                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_AD3                  | I/O  | MFP2  | EBI address/data bus bit 3.                            |
|        |        |        |         | QSPI0_SS                 | I/O  | MFP4  | Quad SPI0 slave select pin.                            |
|        |        |        |         | I <sup>2</sup> S0_MCLK   | O    | MFP6  | I <sup>2</sup> S0 master clock output pin.             |
|        |        |        |         | SPI1_MISO                | I/O  | MFP7  | SPI1 MISO (Master In, Slave Out) pin.                  |
|        |        |        |         | UART2_nRTS               | O    | MFP8  | UART2 request to Send output pin.                      |
|        |        |        |         | I <sup>2</sup> C0_SMBAL  | O    | MFP9  | I <sup>2</sup> C0 SMBus SMBALTER pin                   |
|        |        |        |         | CAN1_TXD                 | O    | MFP10 | CAN1 bus transmitter output.                           |
|        |        |        |         | UART3_TXD                | O    | MFP11 | UART3 data transmitter output pin.                     |
|        |        |        |         | EPWM1_CH2                | I/O  | MFP12 | EPWM1 channel 2 output/capture input.                  |
|        |        |        |         | CCAP_DATA3               | I    | MFP13 | Camera capture data input bus bit 3.                   |
|        |        |        |         | QSPI1_MISO0              | I/O  | MFP14 | Quad SPI1 MISO0 (Master In, Slave Out) pin.            |
|        | 30     | 38     | 72      | PC.2                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_AD2                  | I/O  | MFP2  | EBI address/data bus bit 2.                            |
|        |        |        |         | QSPI0_CLK                | I/O  | MFP4  | Quad SPI0 serial clock pin.                            |
|        |        |        |         | I <sup>2</sup> S0_DI     | I    | MFP6  | I <sup>2</sup> S0 data input pin.                      |
|        |        |        |         | SPI1_MOSI                | I/O  | MFP7  | SPI1 MOSI (Master Out, Slave In) pin.                  |
|        |        |        |         | UART2_nCTS               | I    | MFP8  | UART2 clear to Send input pin.                         |
|        |        |        |         | I <sup>2</sup> C0_SMBSUS | O    | MFP9  | I <sup>2</sup> C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
|        |        |        |         | CAN1_RXD                 | I    | MFP10 | CAN1 bus receiver input.                               |
|        |        |        |         | UART3_RXD                | I    | MFP11 | UART3 data receiver input pin.                         |
|        |        |        |         | EPWM1_CH3                | I/O  | MFP12 | EPWM1 channel 3 output/capture input.                  |
|        |        |        |         | CCAP_DATA2               | I    | MFP13 | Camera capture data input bus bit 2.                   |
|        |        |        |         | QSPI1_MOSI0              | I/O  | MFP14 | Quad SPI1 MOSI0 (Master Out, Slave In) pin.            |
| 19     | 31     | 39     | 73      | PC.1                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_AD1                  | I/O  | MFP2  | EBI address/data bus bit 1.                            |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name               | Type | MFP   | Description   |
|--------|--------|--------|---------|------------------------|------|-------|---|
|        |        |        |         | QSPI0_MISO0            | I/O  | MFP4  | Quad SPI0 MISO0 (Master In, Slave Out) pin.                                     |
|        |        |        |         | I <sup>2</sup> S0_DO   | O    | MFP6  | I <sup>2</sup> S0 data output pin.  |
|        |        |        |         | SPI1_CLK               | I/O  | MFP7  | SPI1 serial clock pin.  |
|        |        |        |         | UART2_TXD              | O    | MFP8  | UART2 data transmitter output pin.  |
|        |        |        |         | I <sup>2</sup> C0_SCL  | I/O  | MFP9  | I <sup>2</sup> C0 clock pin.  |
|        |        |        |         | CAN2_TXD               | O    | MFP10 | CAN2 bus transmitter output.  |
|        |        |        |         | EPWM1_CH4              | I/O  | MFP12 | EPWM1 channel 4 output/capture input.   |
|        |        |        |         | CCAP_DATA1             | I    | MFP13 | Camera capture data input bus bit 1.  |
|        |        |        |         | ACMP0_O                | O    | MFP14 | Analog comparator 0 output pin.   |
|        |        |        |         | EADC0_ST               | I    | MFP15 | EADC0 external trigger input.   |
| 20     | 32     | 40     | 74      | PC.0                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EBI_AD0                | I/O  | MFP2  | EBI address/data bus bit 0.   |
|        |        |        |         | QSPI0_MOSI0            | I/O  | MFP4  | Quad SPI0 MOSI0 (Master Out, Slave In) pin.                                     |
|        |        |        |         | I <sup>2</sup> S0_LRCK | O    | MFP6  | I <sup>2</sup> S0 left right channel clock output pin.                          |
|        |        |        |         | SPI1_SS                | I/O  | MFP7  | SPI1 slave select pin.  |
|        |        |        |         | UART2_RXD              | I    | MFP8  | UART2 data receiver input pin.  |
|        |        |        |         | I <sup>2</sup> C0_SDA  | I/O  | MFP9  | I <sup>2</sup> C0 data input/output pin.  |
|        |        |        |         | CAN2_RXD               | I    | MFP10 | CAN2 bus receiver input.  |
|        |        |        |         | EPWM1_CH5              | I/O  | MFP12 | EPWM1 channel 5 output/capture input.   |
|        |        |        |         | CCAP_DATA0             | I    | MFP13 | Camera capture data input bus bit 0.  |
|        |        |        |         | ACMP1_O                | O    | MFP14 | Analog comparator 1 output pin.   |
|        |        |        |         | EADC1_ST               | I    | MFP15 | EADC1 external trigger input.   |
|        |        |        | 75      | V <sub>SS</sub>        | P    | MFP0  | Ground pin for digital circuit.   |
|        |        |        | 76      | V <sub>DD</sub>        | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
|        |        |        | 77      | PG.9                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EBI_AD0                | I/O  | MFP2  | EBI address/data bus bit 0.   |
|        |        |        |         | QSPI1_MISO1            | I/O  | MFP5  | Quad SPI1 MISO1 (Master In, Slave Out) pin.                                     |
|        |        |        |         | CCAP_PIXCLK            | I    | MFP7  | Camera capture interface pix clock input pin.                                   |
|        |        |        |         | BPWM0_CH5              | I/O  | MFP12 | BPWM0 channel 5 output/capture input.   |
|        |        |        | 78      | PG.10                  | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EBI_AD1                | I/O  | MFP2  | EBI address/data bus bit 1.   |
|        |        |        |         | QSPI1_MOSI1            | I/O  | MFP5  | Quad SPI1 MOSI1 (Master Out, Slave In) pin.                                     |
|        |        |        |         | CCAP_SCLK              | O    | MFP7  | Camera capture interface sensor clock pin.                                      |



| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name    | Type | MFP   | Description                                 |
|--------|--------|--------|---------|-------------|------|-------|---|
|        |        |        |         | BPWM0_CH4   | I/O  | MFP12 | BPWM0 channel 4 output/capture input.       |
|        |        |        | 79      | PG.11       | I/O  | MFP0  | General purpose digital I/O pin.            |
|        |        |        |         | EBI_AD2     | I/O  | MFP2  | EBI address/data bus bit 2.                 |
|        |        |        |         | QSPI1_SS    | I/O  | MFP5  | Quad SPI1 slave select pin.                 |
|        |        |        |         | UART7_TXD   | O    | MFP6  | UART7 data transmitter output pin.          |
|        |        |        |         | CCAP_SFIELD | I    | MFP7  | Camera capture interface SFIELD input pin.  |
|        |        |        |         | BPWM0_CH3   | I/O  | MFP12 | BPWM0 channel 3 output/capture input.       |
|        |        |        | 80      | PG.12       | I/O  | MFP0  | General purpose digital I/O pin.            |
|        |        |        |         | EBI_AD3     | I/O  | MFP2  | EBI address/data bus bit 3.                 |
|        |        |        |         | QSPI1_CLK   | I/O  | MFP5  | Quad SPI1 serial clock pin.                 |
|        |        |        |         | UART7_RXD   | I    | MFP6  | UART7 data receiver input pin.              |
|        |        |        |         | CCAP_VSYNC  | I    | MFP7  | Camera capture interface vsync input pin.   |
|        |        |        |         | BPWM0_CH2   | I/O  | MFP12 | BPWM0 channel 2 output/capture input.       |
|        |        |        | 81      | PG.13       | I/O  | MFP0  | General purpose digital I/O pin.            |
|        |        |        |         | EBI_AD4     | I/O  | MFP2  | EBI address/data bus bit 4.                 |
|        |        |        |         | QSPI1_MISO0 | I/O  | MFP5  | Quad SPI1 MISO0 (Master In, Slave Out) pin. |
|        |        |        |         | UART6_TXD   | O    | MFP6  | UART6 data transmitter output pin.          |
|        |        |        |         | CCAP_HSYNC  | I    | MFP7  | Camera capture interface hsync input pin.   |
|        |        |        |         | BPWM0_CH1   | I/O  | MFP12 | BPWM0 channel 1 output/capture input.       |
|        |        |        | 82      | PG.14       | I/O  | MFP0  | General purpose digital I/O pin.            |
|        |        |        |         | EBI_AD5     | I/O  | MFP2  | EBI address/data bus bit 5.                 |
|        |        |        |         | QSPI1_MOSI0 | I/O  | MFP5  | Quad SPI1 MOSI0 (Master Out, Slave In) pin. |
|        |        |        |         | UART6_RXD   | I    | MFP6  | UART6 data receiver input pin.              |
|        |        |        |         | BPWM0_CH0   | I/O  | MFP12 | BPWM0 channel 0 output/capture input.       |
|        |        |        | 83      | PG.15       | I/O  | MFP0  | General purpose digital I/O pin.            |
|        |        |        |         | CLKO        | O    | MFP14 | Clock Out                                   |
|        |        |        |         | EADC0_ST    | I    | MFP15 | EADC0 external trigger input.               |
|        |        | 41     |         | PD.3        | I/O  | MFP0  | General purpose digital I/O pin.            |
|        |        |        |         | EBI_AD10    | I/O  | MFP2  | EBI address/data bus bit 10.                |
|        |        |        |         | SPI0_SS     | I/O  | MFP4  | SPI0 slave select pin.                      |
|        |        |        |         | UART3_nRTS  | O    | MFP5  | UART3 request to Send output pin.           |
|        |        |        |         | UART0_TXD   | O    | MFP9  | UART0 data transmitter output pin.          |
|        |        | 42     |         | PD.2        | I/O  | MFP0  | General purpose digital I/O pin.            |
|        |        |        |         | EBI_AD11    | I/O  | MFP2  | EBI address/data bus bit 11.                |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name               | Type | MFP   | Description                                   |
|--------|--------|--------|---------|------------------------|------|-------|---|
|        |        |        |         | SPI0_CLK               | I/O  | MFP4  | SPI0 serial clock pin.                        |
|        |        |        |         | UART3_nCTS             | I    | MFP5  | UART3 clear to Send input pin.                |
|        |        |        |         | UART0_RXD              | I    | MFP9  | UART0 data receiver input pin.                |
|        |        | 43     |         | PD.1                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EBI_AD12               | I/O  | MFP2  | EBI address/data bus bit 12.                  |
|        |        |        |         | SPI0_MISO              | I/O  | MFP4  | SPI0 MISO (Master In, Slave Out) pin.         |
|        |        |        |         | UART3_TXD              | O    | MFP5  | UART3 data transmitter output pin.            |
|        |        |        |         | I <sup>2</sup> C2_SCL  | I/O  | MFP6  | I <sup>2</sup> C2 clock pin.                  |
|        |        | 44     |         | PD.0                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EBI_AD13               | I/O  | MFP2  | EBI address/data bus bit 13.                  |
|        |        |        |         | SPI0_MOSI              | I/O  | MFP4  | SPI0 MOSI (Master Out, Slave In) pin.         |
|        |        |        |         | UART3_RXD              | I    | MFP5  | UART3 data receiver input pin.                |
|        |        |        |         | I <sup>2</sup> C2_SDA  | I/O  | MFP6  | I <sup>2</sup> C2 data input/output pin.      |
|        |        |        |         | TM2                    | I/O  | MFP14 | Timer2 event counter input/toggle output pin. |
|        |        |        | 84      | PD.13                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EBI_AD10               | I/O  | MFP2  | EBI address/data bus bit 10.                  |
|        |        |        |         | SD0_nCD                | I    | MFP3  | SD/SDIO0 card detect input pin                |
|        |        |        |         | SPI0_I2SMCLK           | I/O  | MFP4  | SPI0 I <sup>2</sup> S master clock output pin |
|        |        |        |         | SPI1_I2SMCLK           | I/O  | MFP5  | SPI1 I <sup>2</sup> S master clock output pin |
| 21     | 33     | 45     | 85      | PA.12                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | I <sup>2</sup> S0_BCLK | O    | MFP2  | I <sup>2</sup> S0 bit clock output pin.       |
|        |        |        |         | UART4_TXD              | O    | MFP3  | UART4 data transmitter output pin.            |
|        |        |        |         | I <sup>2</sup> C1_SCL  | I/O  | MFP4  | I <sup>2</sup> C1 clock pin.                  |
|        |        |        |         | SPI2_SS                | I/O  | MFP5  | SPI2 slave select pin.                        |
|        |        |        |         | CAN0_TXD               | O    | MFP6  | CAN0 bus transmitter output.                  |
|        |        |        |         | BPWM1_CH2              | I/O  | MFP11 | BPWM1 channel 2 output/capture input.         |
|        |        |        |         | QE11_INDEX             | I    | MFP12 | Quadrature encoder 1 index input              |
|        |        |        |         | USB_VBUS               | P    | MFP14 | Power supply from USB host or HUB.            |
| 22     | 34     | 46     | 86      | PA.13                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | I <sup>2</sup> S0_MCLK | O    | MFP2  | I <sup>2</sup> S0 master clock output pin.    |
|        |        |        |         | UART4_RXD              | I    | MFP3  | UART4 data receiver input pin.                |
|        |        |        |         | I <sup>2</sup> C1_SDA  | I/O  | MFP4  | I <sup>2</sup> C1 data input/output pin.      |
|        |        |        |         | SPI2_CLK               | I/O  | MFP5  | SPI2 serial clock pin.                        |
|        |        |        |         | CAN0_RXD               | I    | MFP6  | CAN0 bus receiver input.                      |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name              | Type | MFP   | Description                                  |
|--------|--------|--------|---------|-----------------------|------|-------|--|
|        |        |        |         | BPWM1_CH3             | I/O  | MFP11 | BPWM1 channel 3 output/capture input.        |
|        |        |        |         | QE11_A                | I    | MFP12 | Quadrature encoder 1 phase A input           |
|        |        |        |         | USB_D-                | A    | MFP14 | USB differential signal D-.                  |
| 23     | 35     | 47     | 87      | PA.14                 | I/O  | MFP0  | General purpose digital I/O pin.             |
|        |        |        |         | I <sup>2</sup> S0_DI  | I    | MFP2  | I <sup>2</sup> S0 data input pin.            |
|        |        |        |         | UART0_TXD             | O    | MFP3  | UART0 data transmitter output pin.           |
|        |        |        |         | SPI2_MISO             | I/O  | MFP5  | SPI2 MISO (Master In, Slave Out) pin.        |
|        |        |        |         | I <sup>2</sup> C2_SCL | I/O  | MFP6  | I <sup>2</sup> C2 clock pin.                 |
|        |        |        |         | BPWM1_CH4             | I/O  | MFP11 | BPWM1 channel 4 output/capture input.        |
|        |        |        |         | QE11_B                | I    | MFP12 | Quadrature encoder 1 phase B input           |
|        |        |        |         | USB_D+                | A    | MFP14 | USB differential signal D+.                  |
| 24     | 36     | 48     | 88      | PA.15                 | I/O  | MFP0  | General purpose digital I/O pin.             |
|        |        |        |         | I <sup>2</sup> S0_DO  | O    | MFP2  | I <sup>2</sup> S0 data output pin.           |
|        |        |        |         | UART0_RXD             | I    | MFP3  | UART0 data receiver input pin.               |
|        |        |        |         | SPI2_MOSI             | I/O  | MFP5  | SPI2 MOSI (Master Out, Slave In) pin.        |
|        |        |        |         | I <sup>2</sup> C2_SDA | I/O  | MFP6  | I <sup>2</sup> C2 data input/output pin.     |
|        |        |        |         | BPWM1_CH5             | I/O  | MFP11 | BPWM1 channel 5 output/capture input.        |
|        |        |        |         | EPWM0_SYNC_IN         | I    | MFP12 | EPWM0 counter synchronous trigger input pin. |
|        |        |        |         | USB_OTG_ID            | I    | MFP14 | USB_ identification.                         |
|        |        |        | 89      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        |        |        | 90      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        |        |        | 91      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        |        |        | 92      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        |        |        | 93      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        |        |        | 94      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        |        |        | 95      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        |        |        | 96      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        |        |        | 97      | PE.7                  | I/O  | MFP0  | General purpose digital I/O pin.             |
|        |        |        |         | SD0_CMD               | I/O  | MFP3  | SD/SDIO0 command/response pin                |
|        |        |        |         | UART5_TXD             | O    | MFP8  | UART5 data transmitter output pin.           |
|        |        |        |         | CAN1_TXD              | O    | MFP9  | CAN1 bus transmitter output.                 |
|        |        |        |         | QE11_INDEX            | I    | MFP11 | Quadrature encoder 1 index input             |
|        |        |        |         | EPWM0_CH0             | I/O  | MFP12 | EPWM0 channel 0 output/capture input.        |
|        |        |        |         | BPWM0_CH5             | I/O  | MFP13 | BPWM0 channel 5 output/capture input.        |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name   | Type | MFP   | Description                           |
|--------|--------|--------|---------|------------|------|-------|---------------------------------------|
|        |        |        | 98      | PE.6       | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |        |        |         | SD0_CLK    | O    | MFP3  | SD/SDIO0 clock output pin             |
|        |        |        |         | SC0_nCD    | I    | MFP6  | Smart Card 0 card detect pin.         |
|        |        |        |         | UART5_RXD  | I    | MFP8  | UART5 data receiver input pin.        |
|        |        |        |         | CAN1_RXD   | I    | MFP9  | CAN1 bus receiver input.              |
|        |        |        |         | QE11_A     | I    | MFP11 | Quadrature encoder 1 phase A input    |
|        |        |        |         | EPWM0_CH1  | I/O  | MFP12 | EPWM0 channel 1 output/capture input. |
|        |        |        |         | BPWM0_CH4  | I/O  | MFP13 | BPWM0 channel 4 output/capture input. |
|        |        |        | 99      | PE.5       | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |        |        |         | EBI_nRD    | O    | MFP2  | EBI read enable output pin.           |
|        |        |        |         | SD0_DAT3   | I/O  | MFP3  | SD/SDIO0 data line bit 3.             |
|        |        |        |         | SC0_PWR    | O    | MFP6  | Smart Card 0 power pin.               |
|        |        |        |         | UART6_TXD  | O    | MFP8  | UART6 data transmitter output pin.    |
|        |        |        |         | UART7_nRTS | O    | MFP9  | UART7 request to Send output pin.     |
|        |        |        |         | QE11_B     | I    | MFP11 | Quadrature encoder 1 phase B input    |
|        |        |        |         | EPWM0_CH2  | I/O  | MFP12 | EPWM0 channel 2 output/capture input. |
|        |        |        |         | BPWM0_CH3  | I/O  | MFP13 | BPWM0 channel 3 output/capture input. |
|        |        |        | 100     | PE.4       | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |        |        |         | EBI_nWR    | O    | MFP2  | EBI write enable output pin.          |
|        |        |        |         | SD0_DAT2   | I/O  | MFP3  | SD/SDIO0 data line bit 2.             |
|        |        |        |         | SC0_RST    | O    | MFP6  | Smart Card 0 reset pin.               |
|        |        |        |         | UART6_RXD  | I    | MFP8  | UART6 data receiver input pin.        |
|        |        |        |         | UART7_nCTS | I    | MFP9  | UART7 clear to Send input pin.        |
|        |        |        |         | QE10_INDEX | I    | MFP11 | Quadrature encoder 0 index input      |
|        |        |        |         | EPWM0_CH3  | I/O  | MFP12 | EPWM0 channel 3 output/capture input. |
|        |        |        |         | BPWM0_CH2  | I/O  | MFP13 | BPWM0 channel 2 output/capture input. |
|        |        |        | 101     | PE.3       | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |        |        |         | EBI_MCLK   | O    | MFP2  | EBI external clock output pin.        |
|        |        |        |         | SD0_DAT1   | I/O  | MFP3  | SD/SDIO0 data line bit 1.             |
|        |        |        |         | SC0_DAT    | I/O  | MFP6  | Smart Card 0 data pin.                |
|        |        |        |         | UART6_nRTS | O    | MFP8  | UART6 request to Send output pin.     |
|        |        |        |         | UART7_TXD  | O    | MFP9  | UART7 data transmitter output pin.    |
|        |        |        |         | QE10_A     | I    | MFP11 | Quadrature encoder 0 phase A input    |
|        |        |        |         | EPWM0_CH4  | I/O  | MFP12 | EPWM0 channel 4 output/capture input. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name               | Type | MFP   | Description   |
|--------|--------|--------|---------|------------------------|------|-------|---|
|        |        |        |         | BPWM0_CH1              | I/O  | MFP13 | BPWM0 channel 1 output/capture input.   |
|        |        |        | 102     | PE.2                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EBI_ALE                | O    | MFP2  | EBI address latch enable output pin.  |
|        |        |        |         | SD0_DAT0               | I/O  | MFP3  | SD/SDIO0 data line bit 0.   |
|        |        |        |         | SC0_CLK                | O    | MFP6  | Smart Card 0 clock pin.   |
|        |        |        |         | UART6_nCTS             | I    | MFP8  | UART6 clear to Send input pin.  |
|        |        |        |         | UART7_RXD              | I    | MFP9  | UART7 data receiver input pin.  |
|        |        |        |         | QEI0_B                 | I    | MFP11 | Quadrature encoder 0 phase B input  |
|        |        |        |         | EPWM0_CH5              | I/O  | MFP12 | EPWM0 channel 5 output/capture input.   |
|        |        |        |         | BPWM0_CH0              | I/O  | MFP13 | BPWM0 channel 0 output/capture input.   |
|        |        |        | 103     | V <sub>SS</sub>        | P    | MFP0  | Ground pin for digital circuit.   |
|        |        |        | 104     | V <sub>DD</sub>        | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
|        |        |        | 105     | PE.1                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EBI_AD10               | I/O  | MFP2  | EBI address/data bus bit 10.  |
|        |        |        |         | QSPI0_MISO0            | I/O  | MFP3  | Quad SPI0 MISO0 (Master In, Slave Out) pin.                                     |
|        |        |        |         | I <sup>2</sup> S0_BCLK | O    | MFP5  | I <sup>2</sup> S0 bit clock output pin.   |
|        |        |        |         | SPI1_MISO              | I/O  | MFP6  | SPI1 MISO (Master In, Slave Out) pin.   |
|        |        |        |         | UART3_TXD              | O    | MFP7  | UART3 data transmitter output pin.  |
|        |        |        |         | I <sup>2</sup> C1_SCL  | I/O  | MFP8  | I <sup>2</sup> C1 clock pin.  |
|        |        |        |         | UART4_nCTS             | I    | MFP9  | UART4 clear to Send input pin.  |
|        |        |        | 106     | PE.0                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EBI_AD11               | I/O  | MFP2  | EBI address/data bus bit 11.  |
|        |        |        |         | QSPI0_MOSI0            | I/O  | MFP3  | Quad SPI0 MOSI0 (Master Out, Slave In) pin.                                     |
|        |        |        |         | I <sup>2</sup> S0_MCLK | O    | MFP5  | I <sup>2</sup> S0 master clock output pin.                                      |
|        |        |        |         | SPI1_MOSI              | I/O  | MFP6  | SPI1 MOSI (Master Out, Slave In) pin.   |
|        |        |        |         | UART3_RXD              | I    | MFP7  | UART3 data receiver input pin.  |
|        |        |        |         | I <sup>2</sup> C1_SDA  | I/O  | MFP8  | I <sup>2</sup> C1 data input/output pin.  |
|        |        |        |         | UART4_nRTS             | O    | MFP9  | UART4 request to Send output pin.   |
|        |        |        | 107     | PH.8                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |        |        |         | EBI_AD12               | I/O  | MFP2  | EBI address/data bus bit 12.  |
|        |        |        |         | QSPI0_CLK              | I/O  | MFP3  | Quad SPI0 serial clock pin.   |
|        |        |        |         | I <sup>2</sup> S0_DI   | I    | MFP5  | I <sup>2</sup> S0 data input pin.   |
|        |        |        |         | SPI1_CLK               | I/O  | MFP6  | SPI1 serial clock pin.  |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name                 | Type | MFP   | Description  |
|--------|--------|--------|---------|--------------------------|------|-------|--|
|        |        |        |         | UART3_nRTS               | O    | MFP7  | UART3 request to Send output pin.  |
|        |        |        |         | I <sup>2</sup> C1_SMBAL  | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBALTER pin   |
|        |        |        |         | I <sup>2</sup> C2_SCL    | I/O  | MFP9  | I <sup>2</sup> C2 clock pin.   |
|        |        |        |         | UART1_TXD                | O    | MFP10 | UART1 data transmitter output pin.   |
|        |        |        | 108     | PH.9                     | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |        |        |         | EBI_AD13                 | I/O  | MFP2  | EBI address/data bus bit 13.   |
|        |        |        |         | QSPI0_SS                 | I/O  | MFP3  | Quad SPI0 slave select pin.  |
|        |        |        |         | I <sup>2</sup> S0_DO     | O    | MFP5  | I <sup>2</sup> S0 data output pin.   |
|        |        |        |         | SPI1_SS                  | I/O  | MFP6  | SPI1 slave select pin.   |
|        |        |        |         | UART3_nCTS               | I    | MFP7  | UART3 clear to Send input pin.   |
|        |        |        |         | I <sup>2</sup> C1_SMBSUS | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBSUS pin (PMBus CONTROL pin)                                     |
|        |        |        |         | I <sup>2</sup> C2_SDA    | I/O  | MFP9  | I <sup>2</sup> C2 data input/output pin.   |
|        |        |        |         | UART1_RXD                | I    | MFP10 | UART1 data receiver input pin.   |
|        |        |        | 109     | PH.10                    | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |        |        |         | EBI_AD14                 | I/O  | MFP2  | EBI address/data bus bit 14.   |
|        |        |        |         | QSPI0_MISO1              | I/O  | MFP3  | Quad SPI0 MISO1 (Master In, Slave Out) pin.  |
|        |        |        |         | I <sup>2</sup> S0_LRCK   | O    | MFP5  | I <sup>2</sup> S0 left right channel clock output pin.                                     |
|        |        |        |         | SPI1_I2SMCLK             | I/O  | MFP6  | SPI1 I <sup>2</sup> S master clock output pin  |
|        |        |        |         | UART4_TXD                | O    | MFP7  | UART4 data transmitter output pin.   |
|        |        |        |         | UART0_TXD                | O    | MFP8  | UART0 data transmitter output pin.   |
|        |        |        | 110     | PH.11                    | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |        |        |         | EBI_AD15                 | I/O  | MFP2  | EBI address/data bus bit 15.   |
|        |        |        |         | QSPI0_MOSI1              | I/O  | MFP3  | Quad SPI0 MOSI1 (Master Out, Slave In) pin.  |
|        |        |        |         | UART4_RXD                | I    | MFP7  | UART4 data receiver input pin.   |
|        |        |        |         | UART0_RXD                | I    | MFP8  | UART0 data receiver input pin.   |
|        |        |        |         | EPWM0_CH5                | I/O  | MFP11 | EPWM0 channel 5 output/capture input.  |
|        |        |        | 111     | PD.14                    | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |        |        |         | EBI_nCS0                 | O    | MFP2  | EBI chip select 0 output pin.  |
|        |        |        |         | SPI0_I2SMCLK             | I/O  | MFP5  | SPI0 I <sup>2</sup> S master clock output pin  |
|        |        |        |         | EPWM0_CH4                | I/O  | MFP11 | EPWM0 channel 4 output/capture input.  |
| 25     | 37     | 49     | 112     | V <sub>SS</sub>          | P    | MFP0  | Ground pin for digital circuit.  |
| 26     | 38     | 50     | 113     | LDO_CAP                  | A    | MFP0  | LDO output pin.<br><b>Note:</b> This pin needs to be connected with an external capacitor. |
| 27     | 39     | 51     | 114     | V <sub>DD</sub>          | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL                                 |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name                 | Type | MFP   | Description  |
|--------|--------|--------|---------|--------------------------|------|-------|--|
|        |        |        |         |                          |      |       | and digital circuit.                                   |
|        | 40     | 52     | 115     | PC.14                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EBI_AD11                 | I/O  | MFP2  | EBI address/data bus bit 11.                           |
|        |        |        |         | SPI0_I2SMCLK             | I/O  | MFP4  | SPI0 I <sup>2</sup> S master clock output pin          |
|        |        |        |         | QSPI0_CLK                | I/O  | MFP6  | Quad SPI0 serial clock pin.                            |
|        |        |        |         | EPWM0_SYNC_IN            | I    | MFP11 | EPWM0 counter synchronous trigger input pin.           |
|        |        |        |         | ETM_TRACE_CLK            | I    | MFP12 | ETM receiver Trace Clock input pin                     |
|        |        |        |         | TM1                      | I/O  | MFP13 | Timer1 event counter input/toggle output pin.          |
|        |        |        |         | USB_VBUS_ST              | I    | MFP14 | USB external VBUS regulator status pin.                |
| 28     | 41     | 53     | 116     | PB.15                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EADC0_CH15               | A    | MFP1  | EADC0 channel 15 analog input.                         |
|        |        |        |         | EADC1_CH15               | A    | MFP1  | EADC1 channel 15 analog input.                         |
|        |        |        |         | EBI_AD12                 | I/O  | MFP2  | EBI address/data bus bit 12.                           |
|        |        |        |         | SPI0_SS                  | I/O  | MFP4  | SPI0 slave select pin.                                 |
|        |        |        |         | UART0_nCTS               | I    | MFP6  | UART0 clear to Send input pin.                         |
|        |        |        |         | UART3_TXD                | O    | MFP7  | UART3 data transmitter output pin.                     |
|        |        |        |         | I <sup>2</sup> C2_SMBAL  | O    | MFP8  | I <sup>2</sup> C2 SMBus SMBALTER pin                   |
|        |        |        |         | EPWM0_BRAKE1             | I    | MFP10 | EPWM0 Brake 1 input pin.                               |
|        |        |        |         | EPWM1_CH0                | I/O  | MFP11 | EPWM1 channel 0 output/capture input.                  |
|        |        |        |         | ETM_TRACE_DATA0          | I    | MFP12 | ETM receiver Trace Data 0 input pin                    |
|        |        |        |         | TM0_EXT                  | I/O  | MFP13 | Timer0 external capture input/toggle output pin.       |
|        |        |        |         | USB_VBUS_EN              | O    | MFP14 | USB external VBUS regulator enable pin.                |
| 29     | 42     | 54     | 117     | PB.14                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EADC0_CH14               | A    | MFP1  | EADC0 channel 14 analog input.                         |
|        |        |        |         | EADC1_CH14               | A    | MFP1  | EADC1 channel 14 analog input.                         |
|        |        |        |         | EBI_AD13                 | I/O  | MFP2  | EBI address/data bus bit 13.                           |
|        |        |        |         | SPI0_CLK                 | I/O  | MFP4  | SPI0 serial clock pin.                                 |
|        |        |        |         | UART0_nRTS               | O    | MFP6  | UART0 request to Send output pin.                      |
|        |        |        |         | UART3_RXD                | I    | MFP7  | UART3 data receiver input pin.                         |
|        |        |        |         | I <sup>2</sup> C2_SMBSUS | O    | MFP8  | I <sup>2</sup> C2 SMBus SMBSUS pin (PMBus CONTROL pin) |
|        |        |        |         | EPWM1_CH1                | I/O  | MFP11 | EPWM1 channel 1 output/capture input.                  |
|        |        |        |         | ETM_TRACE_DATA1          | I    | MFP12 | ETM receiver Trace Data 1 input pin                    |
|        |        |        |         | TM1_EXT                  | I/O  | MFP13 | Timer1 external capture input/toggle output pin.       |
|        |        |        |         | CLKO                     | O    | MFP14 | Clock Out  |

| 32 Pin          | 48 Pin | 64 Pin | 128 Pin  | Pin Name              | Type | MFP   | Description   |
|-----------------|--------|--------|--|-----------------------|------|-------|---|
|                 |        |        |  | USB_VBUS_ST           | I    | MFP15 | USB external VBUS regulator status pin.   |
| 30              | 43     | 55     | 118  | PB.13                 | I/O  | MFP0  | General purpose digital I/O pin.  |
|                 |        |        |  | EADC0_CH13            | A    | MFP1  | EADC0 channel 13 analog input.  |
|                 |        |        |  | EADC1_CH13            | A    | MFP1  | EADC1 channel 13 analog input.  |
|                 |        |        |  | ACMP0_P3              | A    | MFP1  | Analog comparator 0 positive input 3 pin.   |
|                 |        |        |  | ACMP1_P3              | A    | MFP1  | Analog comparator 1 positive input 3 pin.   |
|                 |        |        |  | EBI_AD14              | I/O  | MFP2  | EBI address/data bus bit 14.  |
|                 |        |        |  | SPI0_MISO             | I/O  | MFP4  | SPI0 MISO (Master In, Slave Out) pin.   |
|                 |        |        |  | UART0_TXD             | O    | MFP6  | UART0 data transmitter output pin.  |
|                 |        |        |  | UART3_nRTS            | O    | MFP7  | UART3 request to Send output pin.   |
|                 |        |        |  | I <sup>2</sup> C_SCL  | I/O  | MFP8  | I <sup>2</sup> C2 clock pin.  |
|                 |        |        |  | CCAP_PIXCLK           | I    | MFP10 | Camera capture interface pix clock input pin.   |
|                 |        |        |  | EPWM1_CH2             | I/O  | MFP11 | EPWM1 channel 2 output/capture input.   |
|                 |        |        |  | ETM_TRACE_DATA2       | I    | MFP12 | ETM receiver Trace Data 2 input pin   |
|                 |        |        |  | TM2_EXT               | I/O  | MFP13 | Timer2 external capture input/toggle output pin.  |
| 31              | 44     | 56     | 119  | PB.12                 | I/O  | MFP0  | General purpose digital I/O pin.  |
|                 |        |        |  | EADC0_CH12            | A    | MFP1  | EADC0 channel 12 analog input.  |
|                 |        |        |  | EADC1_CH12            | A    | MFP1  | EADC1 channel 12 analog input.  |
|                 |        |        |  | DAC0_OUT              | A    | MFP1  | DAC0 channel analog output.   |
|                 |        |        |  | ACMP0_P2              | A    | MFP1  | Analog comparator 0 positive input 2 pin.   |
|                 |        |        |  | ACMP1_P2              | A    | MFP1  | Analog comparator 1 positive input 2 pin.   |
|                 |        |        |  | EBI_AD15              | I/O  | MFP2  | EBI address/data bus bit 15.  |
|                 |        |        |  | SPI0_MOSI             | I/O  | MFP4  | SPI0 MOSI (Master Out, Slave In) pin.   |
|                 |        |        |  | UART0_RXD             | I    | MFP6  | UART0 data receiver input pin.  |
|                 |        |        |  | UART3_nCTS            | I    | MFP7  | UART3 clear to Send input pin.  |
|                 |        |        |  | I <sup>2</sup> C2_SDA | I/O  | MFP8  | I <sup>2</sup> C2 data input/output pin.  |
|                 |        |        |  | SD0_nCD               | I    | MFP9  | SD/SDIO0 card detect input pin  |
|                 |        |        |  | CCAP_SCLK             | O    | MFP10 | Camera capture interface sensor clock pin.  |
|                 |        |        |  | EPWM1_CH3             | I/O  | MFP11 | EPWM1 channel 3 output/capture input.   |
| ETM_TRACE_DATA3 | I      | MFP12  | ETM receiver Trace Data 3 input pin              |                       |      |       |   |
| TM3_EXT         | I/O    | MFP13  | Timer3 external capture input/toggle output pin. |                       |      |       |   |
| 32              | 45     | 57     | 120  | AV <sub>DD</sub>      | P    | MFP0  | Power supply for internal analog circuit.   |
|                 |        | 58     | 121  | V <sub>REF</sub>      | A    | MFP0  | ADC reference voltage input.<br><b>Note:</b> This pin needs to be connected with a 1uF capacitor. |



| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name                | Type | MFP   | Description                                   |
|--------|--------|--------|---------|-------------------------|------|-------|---|
|        | 46     | 59     | 122     | AV <sub>SS</sub>        | P    | MFP0  | Ground pin for analog circuit.                |
|        |        | 60     | 123     | PB.11                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EADC0_CH11              | A    | MFP1  | EADC0 channel 11 analog input.                |
|        |        |        |         | EBI_ADR16               | O    | MFP2  | EBI address bus bit 16.                       |
|        |        |        |         | UART0_nCTS              | I    | MFP5  | UART0 clear to Send input pin.                |
|        |        |        |         | UART4_TXD               | O    | MFP6  | UART4 data transmitter output pin.            |
|        |        |        |         | I <sup>2</sup> C1_SCL   | I/O  | MFP7  | I <sup>2</sup> C1 clock pin.                  |
|        |        |        |         | CAN0_TXD                | O    | MFP8  | CAN0 bus transmitter output.                  |
|        |        |        |         | SPI0_I2SMCLK            | I/O  | MFP9  | SPI0 I <sup>2</sup> S master clock output pin |
|        |        |        |         | BPWM1_CH0               | I/O  | MFP10 | BPWM1 channel 0 output/capture input.         |
|        |        |        |         | CCAP_SFIELD             | I    | MFP12 | Camera capture interface SFIELD input pin.    |
|        |        | 61     | 124     | PB.10                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EADC0_CH10              | A    | MFP1  | EADC0 channel 10 analog input.                |
|        |        |        |         | EBI_ADR17               | O    | MFP2  | EBI address bus bit 17.                       |
|        |        |        |         | UART0_nRTS              | O    | MFP5  | UART0 request to Send output pin.             |
|        |        |        |         | UART4_RXD               | I    | MFP6  | UART4 data receiver input pin.                |
|        |        |        |         | I <sup>2</sup> C1_SDA   | I/O  | MFP7  | I <sup>2</sup> C1 data input/output pin.      |
|        |        |        |         | CAN0_RXD                | I    | MFP8  | CAN0 bus receiver input.                      |
|        |        |        |         | BPWM1_CH1               | I/O  | MFP10 | BPWM1 channel 1 output/capture input.         |
|        |        |        |         | CCAP_VSYNC              | I    | MFP12 | Camera capture interface vsync input pin.     |
|        |        | 62     | 125     | PB.9                    | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EADC0_CH9               | A    | MFP1  | EADC0 channel 9 analog input.                 |
|        |        |        |         | EBI_ADR18               | O    | MFP2  | EBI address bus bit 18.                       |
|        |        |        |         | UART0_TXD               | O    | MFP5  | UART0 data transmitter output pin.            |
|        |        |        |         | UART1_nCTS              | I    | MFP6  | UART1 clear to Send input pin.                |
|        |        |        |         | I <sup>2</sup> C1_SMBAL | O    | MFP7  | I <sup>2</sup> C1 SMBus SMBALTER pin          |
|        |        |        |         | UART7_TXD               | O    | MFP8  | UART7 data transmitter output pin.            |
|        |        |        |         | I <sup>2</sup> C0_SCL   | I/O  | MFP9  | I <sup>2</sup> C0 clock pin.                  |
|        |        |        |         | BPWM1_CH2               | I/O  | MFP10 | BPWM1 channel 2 output/capture input.         |
|        |        |        |         | CAN2_TXD                | O    | MFP12 | CAN2 bus transmitter output.                  |
|        |        |        |         | INT7                    | I    | MFP13 | External interrupt 7 input pin.               |
|        |        |        |         | CCAP_HSYNC              | I    | MFP14 | Camera capture interface hsync input pin.     |
|        |        | 63     | 126     | PB.8                    | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |        |        |         | EADC0_CH8               | A    | MFP1  | EADC0 channel 8 analog input.                 |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name                 | Type | MFP   | Description  |
|--------|--------|--------|---------|--------------------------|------|-------|--|
|        |        |        |         | EBI_ADR19                | O    | MFP2  | EBI address bus bit 19.                                |
|        |        |        |         | UART0_RXD                | I    | MFP5  | UART0 data receiver input pin.                         |
|        |        |        |         | UART1_nRTS               | O    | MFP6  | UART1 request to Send output pin.                      |
|        |        |        |         | I <sup>2</sup> C1_SMBSUS | O    | MFP7  | I <sup>2</sup> C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
|        |        |        |         | UART7_RXD                | I    | MFP8  | UART7 data receiver input pin.                         |
|        |        |        |         | I <sup>2</sup> C0_SDA    | I/O  | MFP9  | I <sup>2</sup> C0 data input/output pin.               |
|        |        |        |         | BPWM1_CH3                | I/O  | MFP10 | BPWM1 channel 3 output/capture input.                  |
|        |        |        |         | CAN2_RXD                 | I    | MFP12 | CAN2 bus receiver input.                               |
|        |        |        |         | INT6                     | I    | MFP13 | External interrupt 6 input pin.                        |
|        | 47     | 64     | 127     | PB.7                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EADC0_CH7                | A    | MFP1  | EADC0 channel 7 analog input.                          |
|        |        |        |         | EBI_nWRL                 | O    | MFP2  | EBI low byte write enable output pin.                  |
|        |        |        |         | CAN1_TXD                 | O    | MFP5  | CAN1 bus transmitter output.                           |
|        |        |        |         | UART1_TXD                | O    | MFP6  | UART1 data transmitter output pin.                     |
|        |        |        |         | EBI_nCS0                 | O    | MFP8  | EBI chip select 0 output pin.                          |
|        |        |        |         | BPWM1_CH4                | I/O  | MFP10 | BPWM1 channel 4 output/capture input.                  |
|        |        |        |         | EPWM1_BRAKE0             | I    | MFP11 | EPWM1 Brake 0 input pin.                               |
|        |        |        |         | EPWM1_CH4                | I/O  | MFP12 | EPWM1 channel 4 output/capture input.                  |
|        |        |        |         | INT5                     | I    | MFP13 | External interrupt 5 input pin.                        |
|        |        |        |         | USB_VBUS_ST              | I    | MFP14 | USB external VBUS regulator status pin.                |
|        |        |        |         | ACMP0_O                  | O    | MFP15 | Analog comparator 0 output pin.                        |
|        | 48     | 1      | 128     | PB.6                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |        |        |         | EADC0_CH6                | A    | MFP1  | EADC0 channel 6 analog input.                          |
|        |        |        |         | EBI_nWRH                 | O    | MFP2  | EBI high byte write enable output pin                  |
|        |        |        |         | CAN1_RXD                 | I    | MFP5  | CAN1 bus receiver input.                               |
|        |        |        |         | UART1_RXD                | I    | MFP6  | UART1 data receiver input pin.                         |
|        |        |        |         | EBI_nCS1                 | O    | MFP8  | EBI chip select 1 output pin.                          |
|        |        |        |         | BPWM1_CH5                | I/O  | MFP10 | BPWM1 channel 5 output/capture input.                  |
|        |        |        |         | EPWM1_BRAKE1             | I    | MFP11 | EPWM1 Brake 1 input pin.                               |
|        |        |        |         | EPWM1_CH5                | I/O  | MFP12 | EPWM1 channel 5 output/capture input.                  |
|        |        |        |         | INT4                     | I    | MFP13 | External interrupt 4 input pin.                        |
|        |        |        |         | USB_VBUS_EN              | O    | MFP14 | USB external VBUS regulator enable pin.                |
|        |        |        |         | ACMP1_O                  | O    | MFP15 | Analog comparator 1 output pin.                        |

4.3.3 M483 Series Pin Description

Note: PA.15 MFP can only be as USB\_OTG\_ID when enable full-Speed USB.

| 64 Pin | 128 Pin | Pin Name               | Type                            | MFP   | Description                                   |
|--------|---------|------------------------|---------------------------------|-------|---|
| 2      | 1       | PB.5                   | I/O                             | MFP0  | General purpose digital I/O pin.              |
|        |         | EADC0_CH5              | A                               | MFP1  | EADC0 channel 5 analog input.                 |
|        |         | ACMP1_N                | A                               | MFP1  | Analog comparator 1 negative input pin.       |
|        |         | EBI_ADR0               | O                               | MFP2  | EBI address bus bit 0.                        |
|        |         | SD0_DAT3               | I/O                             | MFP3  | SD/SDIO0 data line bit 3.                     |
|        |         | SPI1_MISO              | I/O                             | MFP5  | SPI1 MISO (Master In, Slave Out) pin.         |
|        |         | I <sup>2</sup> C0_SCL  | I/O                             | MFP6  | I <sup>2</sup> C0 clock pin.                  |
|        |         | UART5_TXD              | O                               | MFP7  | UART5 data transmitter output pin.            |
|        |         | SC0_CLK                | O                               | MFP9  | Smart Card 0 clock pin.                       |
|        |         | I <sup>2</sup> S0_BCLK | O                               | MFP10 | I <sup>2</sup> S0 bit clock output pin.       |
|        |         | EPWM0_CH0              | I/O                             | MFP11 | EPWM0 channel 0 output/capture input.         |
|        |         | UART2_TXD              | O                               | MFP12 | UART2 data transmitter output pin.            |
|        |         | TM0                    | I/O                             | MFP14 | Timer0 event counter input/toggle output pin. |
| INT0   | I       | MFP15                  | External interrupt 0 input pin. |       |   |
| 3      | 2       | PB.4                   | I/O                             | MFP0  | General purpose digital I/O pin.              |
|        |         | EADC0_CH4              | A                               | MFP1  | EADC0 channel 4 analog input.                 |
|        |         | ACMP1_P1               | A                               | MFP1  | Analog comparator 1 positive input 1 pin.     |
|        |         | EBI_ADR1               | O                               | MFP2  | EBI address bus bit 1.                        |
|        |         | SD0_DAT2               | I/O                             | MFP3  | SD/SDIO0 data line bit 2.                     |
|        |         | SPI1_MOSI              | I/O                             | MFP5  | SPI1 MOSI (Master Out, Slave In) pin.         |
|        |         | I <sup>2</sup> C0_SDA  | I/O                             | MFP6  | I <sup>2</sup> C0 data input/output pin.      |
|        |         | UART5_RXD              | I                               | MFP7  | UART5 data receiver input pin.                |
|        |         | SC0_DAT                | I/O                             | MFP9  | Smart Card 0 data pin.                        |
|        |         | I <sup>2</sup> S0_MCLK | O                               | MFP10 | I <sup>2</sup> S0 master clock output pin.    |
|        |         | EPWM0_CH1              | I/O                             | MFP11 | EPWM0 channel 1 output/capture input.         |
|        |         | UART2_RXD              | I                               | MFP12 | UART2 data receiver input pin.                |
|        |         | TM1                    | I/O                             | MFP14 | Timer1 event counter input/toggle output pin. |
| INT1   | I       | MFP15                  | External interrupt 1 input pin. |       |   |
| 4      | 3       | PB.3                   | I/O                             | MFP0  | General purpose digital I/O pin.              |
|        |         | EADC0_CH3              | A                               | MFP1  | EADC0 channel 3 analog input.                 |
|        |         | EADC1_CH11             | A                               | MFP1  | EADC1 channel 11 analog input.                |
|        |         | ACMP0_N                | A                               | MFP1  | Analog comparator 0 negative input pin.       |

| 64 Pin | 128 Pin | Pin Name              | Type | MFP   | Description                                   |
|--------|---------|-----------------------|------|-------|---|
|        |         | EBI_ADR2              | O    | MFP2  | EBI address bus bit 2.                        |
|        |         | SD0_DAT1              | I/O  | MFP3  | SD/SDIO0 data line bit 1.                     |
|        |         | SPI1_CLK              | I/O  | MFP5  | SPI1 serial clock pin.                        |
|        |         | UART1_TXD             | O    | MFP6  | UART1 data transmitter output pin.            |
|        |         | UART5_nRTS            | O    | MFP7  | UART5 request to Send output pin.             |
|        |         | SC0_RST               | O    | MFP9  | Smart Card 0 reset pin.                       |
|        |         | I <sup>2</sup> S0_DI  | I    | MFP10 | I <sup>2</sup> S0 data input pin.             |
|        |         | EPWM0_CH2             | I/O  | MFP11 | EPWM0 channel 2 output/capture input.         |
|        |         | I <sup>2</sup> C1_SCL | I/O  | MFP12 | I <sup>2</sup> C1 clock pin.                  |
|        |         | TM2                   | I/O  | MFP14 | Timer2 event counter input/toggle output pin. |
|        |         | INT2                  | I    | MFP15 | External interrupt 2 input pin.               |
| 5      | 4       | PB.2                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         | EADC0_CH2             | A    | MFP1  | EADC0 channel 2 analog input.                 |
|        |         | EADC1_CH10            | A    | MFP1  | EADC1 channel 10 analog input.                |
|        |         | ACMP0_P1              | A    | MFP1  | Analog comparator 0 positive input 1 pin.     |
|        |         | EBI_ADR3              | O    | MFP2  | EBI address bus bit 3.                        |
|        |         | SD0_DAT0              | I/O  | MFP3  | SD/SDIO0 data line bit 0.                     |
|        |         | SPI1_SS               | I/O  | MFP5  | SPI1 slave select pin.                        |
|        |         | UART1_RXD             | I    | MFP6  | UART1 data receiver input pin.                |
|        |         | UART5_nCTS            | I    | MFP7  | UART5 clear to Send input pin.                |
|        |         | SC0_PWR               | O    | MFP9  | Smart Card 0 power pin.                       |
|        |         | I <sup>2</sup> S0_DO  | O    | MFP10 | I <sup>2</sup> S0 data output pin.            |
|        |         | EPWM0_CH3             | I/O  | MFP11 | EPWM0 channel 3 output/capture input.         |
|        |         | I <sup>2</sup> C1_SDA | I/O  | MFP12 | I <sup>2</sup> C1 data input/output pin.      |
|        |         | TM3                   | I/O  | MFP14 | Timer3 event counter input/toggle output pin. |
|        |         | INT3                  | I    | MFP15 | External interrupt 3 input pin.               |
|        | 5       | PC.12                 | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         | EBI_ADR4              | O    | MFP2  | EBI address bus bit 4.                        |
|        |         | UART0_TXD             | O    | MFP3  | UART0 data transmitter output pin.            |
|        |         | I <sup>2</sup> C0_SCL | I/O  | MFP4  | I <sup>2</sup> C0 clock pin.                  |
|        |         | UART6_TXD             | O    | MFP5  | UART6 data transmitter output pin.            |
|        |         | SC0_nCD               | I    | MFP9  | Smart Card 0 card detect pin.                 |
|        |         | ECAP1_IC2             | I    | MFP11 | Enhanced capture unit 1 input 2 pin.          |
|        |         | EPWM1_CH0             | I/O  | MFP12 | EPWM1 channel 0 output/capture input.         |

| 64 Pin | 128 Pin                    | Pin Name              | Type | MFP   | Description  |
|--------|----------------------------|-----------------------|------|-------|--|
|        |                            | ACMP0_O               | O    | MFP14 | Analog comparator 0 output pin.                        |
|        | 6                          | PC.11                 | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |                            | EBI_ADR5              | O    | MFP2  | EBI address bus bit 5.                                 |
|        |                            | UART0_RXD             | I    | MFP3  | UART0 data receiver input pin.                         |
|        |                            | I <sup>2</sup> C0_SDA | I/O  | MFP4  | I <sup>2</sup> C0 data input/output pin.               |
|        |                            | UART6_RXD             | I    | MFP5  | UART6 data receiver input pin.                         |
|        |                            | ECAP1_IC1             | I    | MFP11 | Enhanced capture unit 1 input 1 pin.                   |
|        |                            | EPWM1_CH1             | I/O  | MFP12 | EPWM1 channel 1 output/capture input.                  |
|        |                            | ACMP1_O               | O    | MFP14 | Analog comparator 1 output pin.                        |
|        | 7                          | PC.10                 | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |                            | EBI_ADR6              | O    | MFP2  | EBI address bus bit 6.                                 |
|        |                            | UART6_nRTS            | O    | MFP5  | UART6 request to Send output pin.                      |
|        |                            | UART3_TXD             | O    | MFP7  | UART3 data transmitter output pin.                     |
|        |                            | CAN1_TXD              | O    | MFP9  | CAN1 bus transmitter output.                           |
|        |                            | ECAP1_IC0             | I    | MFP11 | Enhanced capture unit 1 input 0 pin.                   |
|        |                            | EPWM1_CH2             | I/O  | MFP12 | EPWM1 channel 2 output/capture input.                  |
|        |                            | EADC1_ST              | I    | MFP14 | EADC1 external trigger input.                          |
|        | 8                          | PC.9                  | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |                            | EBI_ADR7              | O    | MFP2  | EBI address bus bit 7.                                 |
|        |                            | UART6_nCTS            | I    | MFP5  | UART6 clear to Send input pin.                         |
|        |                            | UART3_RXD             | I    | MFP7  | UART3 data receiver input pin.                         |
|        |                            | CAN1_RXD              | I    | MFP9  | CAN1 bus receiver input.                               |
|        |                            | EPWM1_CH3             | I/O  | MFP12 | EPWM1 channel 3 output/capture input.                  |
|        |                            | EADC1_ST              | I    | MFP14 | EADC1 external trigger input.                          |
|        |                            | 9                     | PB.1 | I/O   | MFP0   |
|        | EADC0_CH1                  |                       | A    | MFP1  | EADC0 channel 1 analog input.                          |
|        | EADC1_CH9                  |                       | A    | MFP1  | EADC1 channel 9 analog input.                          |
|        | EBI_ADR8                   |                       | O    | MFP2  | EBI address bus bit 8.                                 |
|        | SD0_CLK                    |                       | O    | MFP3  | SD/SDIO0 clock output pin                              |
|        | SPI1_I <sup>2</sup> S_MCLK |                       | I/O  | MFP5  | SPI1 I <sup>2</sup> S master clock output pin          |
|        | UART2_TXD                  |                       | O    | MFP7  | UART2 data transmitter output pin.                     |
|        | I <sup>2</sup> C1_SCL      |                       | I/O  | MFP9  | I <sup>2</sup> C1 clock pin.                           |
|        | I <sup>2</sup> S0_LRCK     |                       | O    | MFP10 | I <sup>2</sup> S0 left right channel clock output pin. |
|        | EPWM0_CH4                  |                       | I/O  | MFP11 | EPWM0 channel 4 output/capture input.                  |

| 64 Pin | 128 Pin | Pin Name              | Type | MFP   | Description   |
|--------|---------|-----------------------|------|-------|---|
|        |         | EPWM1_CH4             | I/O  | MFP12 | EPWM1 channel 4 output/capture input.   |
|        |         | EPWM0_BRAKE0          | I    | MFP13 | EPWM0 Brake 0 input pin.  |
| 7      | 10      | PB.0                  | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EADC0_CH0             | A    | MFP1  | EADC0 channel 0 analog input.   |
|        |         | EADC1_CH8             | A    | MFP1  | EADC1 channel 8 analog input.   |
|        |         | EBI_ADR9              | O    | MFP2  | EBI address bus bit 9.  |
|        |         | SD0_CMD               | I/O  | MFP3  | SD/SDIO0 command/response pin   |
|        |         | SPI2_I2SMCLK          | I/O  | MFP4  | SPI2 I <sup>2</sup> S master clock output pin                                   |
|        |         | UART2_RXD             | I    | MFP7  | UART2 data receiver input pin.  |
|        |         | SPI0_I2SMCLK          | I/O  | MFP8  | SPI0 I <sup>2</sup> S master clock output pin                                   |
|        |         | I <sup>2</sup> C1_SDA | I/O  | MFP9  | I <sup>2</sup> C1 data input/output pin.  |
|        |         | EPWM0_CH5             | I/O  | MFP11 | EPWM0 channel 5 output/capture input.   |
|        |         | EPWM1_CH5             | I/O  | MFP12 | EPWM1 channel 5 output/capture input.   |
|        |         | EPWM0_BRAKE1          | I    | MFP13 | EPWM0 Brake 1 input pin.  |
|        | 11      | V <sub>SS</sub>       | P    | MFP0  | Ground pin for digital circuit.   |
|        | 12      | V <sub>DD</sub>       | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 8      | 13      | PA.11                 | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EADC1_CH7             | A    | MFP1  | EADC1 channel 7 analog input.   |
|        |         | ACMP0_P0              | A    | MFP1  | Analog comparator 0 positive input 0 pin.                                       |
|        |         | EBI_nRD               | O    | MFP2  | EBI read enable output pin.   |
|        |         | SPI2_SS               | I/O  | MFP4  | SPI2 slave select pin.  |
|        |         | I <sup>2</sup> C2_SCL | I/O  | MFP7  | I <sup>2</sup> C2 clock pin.  |
|        |         | UART6_TXD             | O    | MFP8  | UART6 data transmitter output pin.  |
|        |         | BPWM0_CH0             | I/O  | MFP9  | BPWM0 channel 0 output/capture input.   |
|        |         | EPWM0_SYNC_OUT        | O    | MFP10 | EPWM0 counter synchronous trigger output pin.                                   |
|        |         | TM0_EXT               | I/O  | MFP13 | Timer0 external capture input/toggle output pin.                                |
| 9      | 14      | PA.10                 | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EADC1_CH6             | A    | MFP1  | EADC1 channel 6 analog input.   |
|        |         | ACMP1_P0              | A    | MFP1  | Analog comparator 1 positive input 0 pin.                                       |
|        |         | EBI_nWR               | O    | MFP2  | EBI write enable output pin.  |
|        |         | SPI2_CLK              | I/O  | MFP4  | SPI2 serial clock pin.  |
|        |         | I <sup>2</sup> C2_SDA | I/O  | MFP7  | I <sup>2</sup> C2 data input/output pin.  |
|        |         | UART6_RXD             | I    | MFP8  | UART6 data receiver input pin.  |

| 64 Pin | 128 Pin | Pin Name     | Type | MFP   | Description                                      |
|--------|---------|--------------|------|-------|--|
|        |         | BPWM0_CH1    | I/O  | MFP9  | BPWM0 channel 1 output/capture input.            |
|        |         | QE11_INDEX   | I    | MFP10 | Quadrature encoder 1 index input                 |
|        |         | ECAP0_IC0    | I    | MFP11 | Enhanced capture unit 0 input 0 pin.             |
|        |         | TM1_EXT      | I/O  | MFP13 | Timer1 external capture input/toggle output pin. |
|        |         | DAC0_ST      | I    | MFP14 | DAC0 external trigger input.                     |
|        |         |              |      |       |  |
| 10     | 15      | PA.9         | I/O  | MFP0  | General purpose digital I/O pin.                 |
|        |         | EADC1_CH5    | A    | MFP1  | EADC1 channel 5 analog input.                    |
|        |         | EBI_MCLK     | O    | MFP2  | EBI external clock output pin.                   |
|        |         | SPI2_MISO    | I/O  | MFP4  | SPI2 MISO (Master In, Slave Out) pin.            |
|        |         | UART1_TXD    | O    | MFP7  | UART1 data transmitter output pin.               |
|        |         | UART7_TXD    | O    | MFP8  | UART7 data transmitter output pin.               |
|        |         | BPWM0_CH2    | I/O  | MFP9  | BPWM0 channel 2 output/capture input.            |
|        |         | QE11_A       | I    | MFP10 | Quadrature encoder 1 phase A input               |
|        |         | ECAP0_IC1    | I    | MFP11 | Enhanced capture unit 0 input 1 pin.             |
|        |         | TM2_EXT      | I/O  | MFP13 | Timer2 external capture input/toggle output pin. |
|        |         |              |      |       |  |
| 11     | 16      | PA.8         | I/O  | MFP0  | General purpose digital I/O pin.                 |
|        |         | EADC1_CH4    | A    | MFP1  | EADC1 channel 4 analog input.                    |
|        |         | EBI_ALE      | O    | MFP2  | EBI address latch enable output pin.             |
|        |         | SPI2_MOSI    | I/O  | MFP4  | SPI2 MOSI (Master Out, Slave In) pin.            |
|        |         | UART1_RXD    | I    | MFP7  | UART1 data receiver input pin.                   |
|        |         | UART7_RXD    | I    | MFP8  | UART7 data receiver input pin.                   |
|        |         | BPWM0_CH3    | I/O  | MFP9  | BPWM0 channel 3 output/capture input.            |
|        |         | QE11_B       | I    | MFP10 | Quadrature encoder 1 phase B input               |
|        |         | ECAP0_IC2    | I    | MFP11 | Enhanced capture unit 0 input 2 pin.             |
|        |         | TM3_EXT      | I/O  | MFP13 | Timer3 external capture input/toggle output pin. |
|        |         | INT4         | I    | MFP15 | External interrupt 4 input pin.                  |
|        | 17      | PC.13        | I/O  | MFP0  | General purpose digital I/O pin.                 |
|        |         | EADC1_CH3    | A    | MFP1  | EADC1 channel 3 analog input.                    |
|        |         | EBI_ADR10    | O    | MFP2  | EBI address bus bit 10.                          |
|        |         | SPI2_I2SMCLK | I/O  | MFP4  | SPI2 I <sup>2</sup> S master clock output pin    |
|        |         | CAN1_TXD     | O    | MFP5  | CAN1 bus transmitter output.                     |
|        |         | UART2_TXD    | O    | MFP7  | UART2 data transmitter output pin.               |

| 64 Pin | 128 Pin | Pin Name                | Type | MFP   | Description                                   |
|--------|---------|-------------------------|------|-------|---|
|        |         | BPWM0_CH4               | I/O  | MFP9  | BPWM0 channel 4 output/capture input.         |
|        |         | CLKO                    | O    | MFP13 | Clock Out                                     |
|        |         | EADC0_ST                | I    | MFP14 | EADC0 external trigger input.                 |
|        | 18      | PD.12                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         | EADC1_CH2               | A    | MFP1  | EADC1 channel 2 analog input.                 |
|        |         | EBI_nCS0                | O    | MFP2  | EBI chip select 0 output pin.                 |
|        |         | CAN1_RXD                | I    | MFP5  | CAN1 bus receiver input.                      |
|        |         | UART2_RXD               | I    | MFP7  | UART2 data receiver input pin.                |
|        |         | BPWM0_CH5               | I/O  | MFP9  | BPWM0 channel 5 output/capture input.         |
|        |         | QE10_INDEX              | I    | MFP10 | Quadrature encoder 0 index input              |
|        |         | CLKO                    | O    | MFP13 | Clock Out                                     |
|        |         | EADC0_ST                | I    | MFP14 | EADC0 external trigger input.                 |
|        |         | INT5                    | I    | MFP15 | External interrupt 5 input pin.               |
|        | 19      | PD.11                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         | EADC1_CH1               | A    | MFP1  | EADC1 channel 1 analog input.                 |
|        |         | EBI_nCS1                | O    | MFP2  | EBI chip select 1 output pin.                 |
|        |         | UART1_TXD               | O    | MFP3  | UART1 data transmitter output pin.            |
|        |         | CAN0_TXD                | O    | MFP4  | CAN0 bus transmitter output.                  |
|        |         | QE10_A                  | I    | MFP10 | Quadrature encoder 0 phase A input            |
|        |         | INT6                    | I    | MFP15 | External interrupt 6 input pin.               |
|        | 20      | PD.10                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         | EADC1_CH0               | A    | MFP1  | EADC1 channel 0 analog input.                 |
|        |         | EBI_nCS2                | O    | MFP2  | EBI chip select 2 output pin.                 |
|        |         | UART1_RXD               | I    | MFP3  | UART1 data receiver input pin.                |
|        |         | CAN0_RXD                | I    | MFP4  | CAN0 bus receiver input.                      |
|        |         | QE10_B                  | I    | MFP10 | Quadrature encoder 0 phase B input            |
|        |         | INT7                    | I    | MFP15 | External interrupt 7 input pin.               |
|        | 21      | PG.2                    | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         | EBI_ADR11               | O    | MFP2  | EBI address bus bit 11.                       |
|        |         | SPI2_SS                 | I/O  | MFP3  | SPI2 slave select pin.                        |
|        |         | I <sup>2</sup> C0_SMBAL | O    | MFP4  | I <sup>2</sup> C0 SMBus SMBALTER pin          |
|        |         | I <sup>2</sup> C1_SCL   | I/O  | MFP5  | I <sup>2</sup> C1 clock pin.                  |
|        |         | CCAP_DATA7              | I    | MFP7  | Camera capture data input bus bit 7.          |
|        |         | TM0                     | I/O  | MFP13 | Timer0 event counter input/toggle output pin. |



| 64 Pin | 128 Pin | Pin Name                | Type | MFP   | Description  |
|--------|---------|-------------------------|------|-------|--|
|        | 22      | PG.3                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EBI_ADR12               | O    | MFP2  | EBI address bus bit 12.                                |
|        |         | SPI2_CLK                | I/O  | MFP3  | SPI2 serial clock pin.                                 |
|        |         | I <sup>2</sup> C0_SMBUS | O    | MFP4  | I <sup>2</sup> C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
|        |         | I <sup>2</sup> C1_SDA   | I/O  | MFP5  | I <sup>2</sup> C1 data input/output pin.               |
|        |         | CCAP_DATA6              | I    | MFP7  | Camera capture data input bus bit 6.                   |
|        |         | TM1                     | I/O  | MFP13 | Timer1 event counter input/toggle output pin.          |
|        | 23      | PG.4                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EBI_ADR13               | O    | MFP2  | EBI address bus bit 13.                                |
|        |         | SPI2_MISO               | I/O  | MFP3  | SPI2 MISO (Master In, Slave Out) pin.                  |
|        |         | CCAP_DATA5              | I    | MFP7  | Camera capture data input bus bit 5.                   |
|        |         | TM2                     | I/O  | MFP13 | Timer2 event counter input/toggle output pin.          |
|        | 24      | PF.11                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EBI_ADR14               | O    | MFP2  | EBI address bus bit 14.                                |
|        |         | SPI2_MOSI               | I/O  | MFP3  | SPI2 MOSI (Master Out, Slave In) pin.                  |
|        |         | UART5_TXD               | O    | MFP6  | UART5 data transmitter output pin.                     |
|        |         | CCAP_DATA4              | I    | MFP7  | Camera capture data input bus bit 4.                   |
|        |         | TM3                     | I/O  | MFP13 | Timer3 event counter input/toggle output pin.          |
|        | 25      | PF.10                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EBI_ADR15               | O    | MFP2  | EBI address bus bit 15.                                |
|        |         | SC0_nCD                 | I    | MFP3  | Smart Card 0 card detect pin.                          |
|        |         | I <sup>2</sup> S0_BCLK  | O    | MFP4  | I <sup>2</sup> S0 bit clock output pin.                |
|        |         | SPI0_I2SMCLK            | I/O  | MFP5  | SPI0 I <sup>2</sup> S master clock output pin          |
|        |         | UART5_RXD               | I    | MFP6  | UART5 data receiver input pin.                         |
|        |         | CCAP_DATA3              | I    | MFP7  | Camera capture data input bus bit 3.                   |
|        | 26      | PF.9                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EBI_ADR16               | O    | MFP2  | EBI address bus bit 16.                                |
|        |         | SC0_PWR                 | O    | MFP3  | Smart Card 0 power pin.                                |
|        |         | I <sup>2</sup> S0_MCLK  | O    | MFP4  | I <sup>2</sup> S0 master clock output pin.             |
|        |         | SPI0_SS                 | I/O  | MFP5  | SPI0 slave select pin.                                 |
|        |         | UART5_nRTS              | O    | MFP6  | UART5 request to Send output pin.                      |
|        |         | CCAP_DATA2              | I    | MFP7  | Camera capture data input bus bit 2.                   |
|        |         | CAN1_TXD                | O    | MFP8  | CAN1 bus transmitter output.                           |
|        | 27      | PF.8                    | I/O  | MFP0  | General purpose digital I/O pin.                       |

| 64 Pin | 128 Pin | Pin Name               | Type | MFP   | Description  |
|--------|---------|------------------------|------|-------|--|
|        |         | EBI_ADR17              | O    | MFP2  | EBI address bus bit 17.                                |
|        |         | SC0_RST                | O    | MFP3  | Smart Card 0 reset pin.                                |
|        |         | I <sup>2</sup> S0_DI   | I    | MFP4  | I <sup>2</sup> S0 data input pin.                      |
|        |         | SPI0_CLK               | I/O  | MFP5  | SPI0 serial clock pin.                                 |
|        |         | UART5_nCTS             | I    | MFP6  | UART5 clear to Send input pin.                         |
|        |         | CCAP_DATA1             | I    | MFP7  | Camera capture data input bus bit 1.                   |
|        |         | CAN1_RXD               | I    | MFP8  | CAN1 bus receiver input.                               |
|        |         | TAMPER2                | I/O  | MFP10 | TAMPER detector loop pin 2.                            |
|        | 28      | PF.7                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EBI_ADR18              | O    | MFP2  | EBI address bus bit 18.                                |
|        |         | SC0_DAT                | I/O  | MFP3  | Smart Card 0 data pin.                                 |
|        |         | I <sup>2</sup> S0_DO   | O    | MFP4  | I <sup>2</sup> S0 data output pin.                     |
|        |         | SPI0_MISO              | I/O  | MFP5  | SPI0 MISO (Master In, Slave Out) pin.                  |
|        |         | UART4_TXD              | O    | MFP6  | UART4 data transmitter output pin.                     |
|        |         | CCAP_DATA0             | I    | MFP7  | Camera capture data input bus bit 0.                   |
|        |         | CAN2_TXD               | O    | MFP8  | CAN2 bus transmitter output.                           |
|        |         | TAMPER1                | I/O  | MFP10 | TAMPER detector loop pin 1.                            |
|        | 29      | PF.6                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EBI_ADR19              | O    | MFP2  | EBI address bus bit 19.                                |
|        |         | SC0_CLK                | O    | MFP3  | Smart Card 0 clock pin.                                |
|        |         | I <sup>2</sup> S0_LRCK | O    | MFP4  | I <sup>2</sup> S0 left right channel clock output pin. |
|        |         | SPI0_MOSI              | I/O  | MFP5  | SPI0 MOSI (Master Out, Slave In) pin.                  |
|        |         | UART4_RXD              | I    | MFP6  | UART4 data receiver input pin.                         |
|        |         | EBI_nCS0               | O    | MFP7  | EBI chip select 0 output pin.                          |
|        |         | CAN2_RXD               | I    | MFP8  | CAN2 bus receiver input.                               |
|        |         | TAMPER0                | I/O  | MFP10 | TAMPER detector loop pin 0.                            |
| 13     | 30      | V <sub>BAT</sub>       | P    | MFP0  | Power supply by batteries for RTC.                     |
|        | 31      | PF.5                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | UART2_RXD              | I    | MFP2  | UART2 data receiver input pin.                         |
|        |         | UART2_nCTS             | I    | MFP4  | UART2 clear to Send input pin.                         |
|        |         | EPWM0_CH0              | I/O  | MFP7  | EPWM0 channel 0 output/capture input.                  |
|        |         | BPWM0_CH4              | I/O  | MFP8  | BPWM0 channel 4 output/capture input.                  |
|        |         | EPWM0_SYNC_OUT         | O    | MFP9  | EPWM0 counter synchronous trigger output pin.          |
|        |         | X32_IN                 | I    | MFP10 | External 32.768 kHz crystal input pin.                 |

| 64 Pin | 128 Pin | Pin Name              | Type | MFP   | Description                                       |
|--------|---------|-----------------------|------|-------|---|
|        |         | EADC0_ST              | I    | MFP11 | EADC0 external trigger input.                     |
| 15     | 32      | PF.4                  | I/O  | MFP0  | General purpose digital I/O pin.                  |
|        |         | UART2_TXD             | O    | MFP2  | UART2 data transmitter output pin.                |
|        |         | UART2_nRTS            | O    | MFP4  | UART2 request to Send output pin.                 |
|        |         | EPWM0_CH1             | I/O  | MFP7  | EPWM0 channel 1 output/capture input.             |
|        |         | BPWM0_CH5             | I/O  | MFP8  | BPWM0 channel 5 output/capture input.             |
|        |         | X32_OUT               | O    | MFP10 | External 32.768 kHz crystal output pin.           |
|        |         | EADC1_ST              | I    | MFP11 | EADC1 external trigger input.                     |
|        | 33      | PH.4                  | I/O  | MFP0  | General purpose digital I/O pin.                  |
|        |         | EBI_ADR3              | O    | MFP2  | EBI address bus bit 3.                            |
|        |         | SPI1_MISO             | I/O  | MFP3  | SPI1 MISO (Master In, Slave Out) pin.             |
|        |         | UART7_nRTS            | O    | MFP4  | UART7 request to Send output pin.                 |
|        |         | UART6_TXD             | O    | MFP5  | UART6 data transmitter output pin.                |
|        | 34      | PH.5                  | I/O  | MFP0  | General purpose digital I/O pin.                  |
|        |         | EBI_ADR2              | O    | MFP2  | EBI address bus bit 2.                            |
|        |         | SPI1_MOSI             | I/O  | MFP3  | SPI1 MOSI (Master Out, Slave In) pin.             |
|        |         | UART7_nCTS            | I    | MFP4  | UART7 clear to Send input pin.                    |
|        |         | UART6_RXD             | I    | MFP5  | UART6 data receiver input pin.                    |
|        | 35      | PH.6                  | I/O  | MFP0  | General purpose digital I/O pin.                  |
|        |         | EBI_ADR1              | O    | MFP2  | EBI address bus bit 1.                            |
|        |         | SPI1_CLK              | I/O  | MFP3  | SPI1 serial clock pin.                            |
|        |         | UART7_TXD             | O    | MFP4  | UART7 data transmitter output pin.                |
|        | 36      | PH.7                  | I/O  | MFP0  | General purpose digital I/O pin.                  |
|        |         | EBI_ADR0              | O    | MFP2  | EBI address bus bit 0.                            |
|        |         | SPI1_SS               | I/O  | MFP3  | SPI1 slave select pin.                            |
|        |         | UART7_RXD             | I    | MFP4  | UART7 data receiver input pin.                    |
| 16     | 37      | PF.3                  | I/O  | MFP0  | General purpose digital I/O pin.                  |
|        |         | EBI_nCS0              | O    | MFP2  | EBI chip select 0 output pin.                     |
|        |         | UART0_TXD             | O    | MFP3  | UART0 data transmitter output pin.                |
|        |         | I <sup>2</sup> C0_SCL | I/O  | MFP4  | I <sup>2</sup> C0 clock pin.                      |
|        |         | XT1_IN                | I    | MFP10 | External 4~24 MHz (high speed) crystal input pin. |
|        |         | BPWM1_CH0             | I/O  | MFP11 | BPWM1 channel 0 output/capture input.             |
| 17     | 38      | PF.2                  | I/O  | MFP0  | General purpose digital I/O pin.                  |
|        |         | EBI_nCS1              | O    | MFP2  | EBI chip select 1 output pin.                     |

| 64 Pin | 128 Pin | Pin Name               | Type | MFP   | Description   |
|--------|---------|------------------------|------|-------|---|
|        |         | UART0_RXD              | I    | MFP3  | UART0 data receiver input pin.  |
|        |         | I <sup>2</sup> C0_SDA  | I/O  | MFP4  | I <sup>2</sup> C0 data input/output pin.  |
|        |         | QSPI0_CLK              | I/O  | MFP5  | Quad SPI0 serial clock pin.   |
|        |         | XT1_OUT                | O    | MFP10 | External 4~24 MHz (high speed) crystal output pin.                              |
|        |         | BPWM1_CH1              | I/O  | MFP11 | BPWM1 channel 1 output/capture input.   |
|        | 39      | V <sub>SS</sub>        | P    | MFP0  | Ground pin for digital circuit.   |
|        | 40      | V <sub>DD</sub>        | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
|        | 41      | PE.8                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EBI_ADR10              | O    | MFP2  | EBI address bus bit 10.   |
|        |         | I <sup>2</sup> S0_BCLK | O    | MFP4  | I <sup>2</sup> S0 bit clock output pin.   |
|        |         | SPI2_CLK               | I/O  | MFP5  | SPI2 serial clock pin.  |
|        |         | UART2_TXD              | O    | MFP7  | UART2 data transmitter output pin.  |
|        |         | EPWM0_CH0              | I/O  | MFP10 | EPWM0 channel 0 output/capture input.   |
|        |         | EPWM0_BRAKE0           | I    | MFP11 | EPWM0 Brake 0 input pin.  |
|        |         | ECAP0_IC0              | I    | MFP12 | Enhanced capture unit 0 input 0 pin.  |
|        |         | TRACE_DATA3            | O    | MFP14 | ETM Trace Data 3 output pin   |
|        | 42      | PE.9                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EBI_ADR11              | O    | MFP2  | EBI address bus bit 11.   |
|        |         | I <sup>2</sup> S0_MCLK | O    | MFP4  | I <sup>2</sup> S0 master clock output pin.                                      |
|        |         | SPI2_MISO              | I/O  | MFP5  | SPI2 MISO (Master In, Slave Out) pin.   |
|        |         | UART2_RXD              | I    | MFP7  | UART2 data receiver input pin.  |
|        |         | EPWM0_CH1              | I/O  | MFP10 | EPWM0 channel 1 output/capture input.   |
|        |         | EPWM0_BRAKE1           | I    | MFP11 | EPWM0 Brake 1 input pin.  |
|        |         | ECAP0_IC1              | I    | MFP12 | Enhanced capture unit 0 input 1 pin.  |
|        |         | TRACE_DATA2            | O    | MFP14 | ETM Trace Data 2 output pin   |
|        | 43      | PE.10                  | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EBI_ADR12              | O    | MFP2  | EBI address bus bit 12.   |
|        |         | I <sup>2</sup> S0_DI   | I    | MFP4  | I <sup>2</sup> S0 data input pin.   |
|        |         | SPI2_MOSI              | I/O  | MFP5  | SPI2 MOSI (Master Out, Slave In) pin.   |
|        |         | UART3_TXD              | O    | MFP7  | UART3 data transmitter output pin.  |
|        |         | EPWM0_CH2              | I/O  | MFP10 | EPWM0 channel 2 output/capture input.   |
|        |         | EPWM1_BRAKE0           | I    | MFP11 | EPWM1 Brake 0 input pin.  |
|        |         | ECAP0_IC2              | I    | MFP12 | Enhanced capture unit 0 input 2 pin.  |

| 64 Pin | 128 Pin | Pin Name               | Type | MFP   | Description  |
|--------|---------|------------------------|------|-------|--|
|        |         | TRACE_DATA1            | O    | MFP14 | ETM Trace Data 1 output pin                            |
|        | 44      | PE.11                  | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EBI_ADR13              | O    | MFP2  | EBI address bus bit 13.                                |
|        |         | I <sup>2</sup> S0_DO   | O    | MFP4  | I <sup>2</sup> S0 data output pin.                     |
|        |         | SPI2_SS                | I/O  | MFP5  | SPI2 slave select pin.                                 |
|        |         | UART3_RXD              | I    | MFP7  | UART3 data receiver input pin.                         |
|        |         | UART1_nCTS             | I    | MFP8  | UART1 clear to Send input pin.                         |
|        |         | EPWM0_CH3              | I/O  | MFP10 | EPWM0 channel 3 output/capture input.                  |
|        |         | EPWM1_BRAKE1           | I    | MFP11 | EPWM1 Brake 1 input pin.                               |
|        |         | ECAP1_IC2              | I    | MFP13 | Enhanced capture unit 1 input 2 pin.                   |
|        |         | TRACE_DATA0            | O    | MFP14 | ETM Trace Data 0 output pin                            |
|        | 45      | PE.12                  | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EBI_ADR14              | O    | MFP2  | EBI address bus bit 14.                                |
|        |         | I <sup>2</sup> S0_LRCK | O    | MFP4  | I <sup>2</sup> S0 left right channel clock output pin. |
|        |         | SPI2_I2SMCLK           | I/O  | MFP5  | SPI2 I <sup>2</sup> S master clock output pin          |
|        |         | UART1_nRTS             | O    | MFP8  | UART1 request to Send output pin.                      |
|        |         | EPWM0_CH4              | I/O  | MFP10 | EPWM0 channel 4 output/capture input.                  |
|        |         | ECAP1_IC1              | I    | MFP13 | Enhanced capture unit 1 input 1 pin.                   |
|        |         | TRACE_CLK              | O    | MFP14 | ETM Trace Clock output pin                             |
|        | 46      | PE.13                  | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EBI_ADR15              | O    | MFP2  | EBI address bus bit 15.                                |
|        |         | I <sup>2</sup> C0_SCL  | I/O  | MFP4  | I <sup>2</sup> C0 clock pin.                           |
|        |         | UART4_nRTS             | O    | MFP5  | UART4 request to Send output pin.                      |
|        |         | UART1_TXD              | O    | MFP8  | UART1 data transmitter output pin.                     |
|        |         | EPWM0_CH5              | I/O  | MFP10 | EPWM0 channel 5 output/capture input.                  |
|        |         | EPWM1_CH0              | I/O  | MFP11 | EPWM1 channel 0 output/capture input.                  |
|        |         | BPWM1_CH5              | I/O  | MFP12 | BPWM1 channel 5 output/capture input.                  |
|        |         | ECAP1_IC0              | I    | MFP13 | Enhanced capture unit 1 input 0 pin.                   |
|        | 47      | PC.8                   | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EBI_ADR16              | O    | MFP2  | EBI address bus bit 16.                                |
|        |         | I <sup>2</sup> C0_SDA  | I/O  | MFP4  | I <sup>2</sup> C0 data input/output pin.               |
|        |         | UART4_nCTS             | I    | MFP5  | UART4 clear to Send input pin.                         |
|        |         | UART1_RXD              | I    | MFP8  | UART1 data receiver input pin.                         |
|        |         | EPWM1_CH1              | I/O  | MFP11 | EPWM1 channel 1 output/capture input.                  |

| 64 Pin | 128 Pin | Pin Name                | Type | MFP   | Description  |
|--------|---------|-------------------------|------|-------|--|
|        |         | BPWM1_CH4               | I/O  | MFP12 | BPWM1 channel 4 output/capture input.                  |
| 18     | 48      | PC.7                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EBI_AD9                 | I/O  | MFP2  | EBI address/data bus bit 9.                            |
|        |         | SPI1_MISO               | I/O  | MFP4  | SPI1 MISO (Master In, Slave Out) pin.                  |
|        |         | UART4_TXD               | O    | MFP5  | UART4 data transmitter output pin.                     |
|        |         | UART0_nCTS              | I    | MFP7  | UART0 clear to Send input pin.                         |
|        |         | I <sup>2</sup> C1_SMBAL | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBALTER pin                   |
|        |         | UART6_TXD               | O    | MFP9  | UART6 data transmitter output pin.                     |
|        |         | EPWM1_CH2               | I/O  | MFP11 | EPWM1 channel 2 output/capture input.                  |
|        |         | BPWM1_CH0               | I/O  | MFP12 | BPWM1 channel 0 output/capture input.                  |
|        |         | TM0                     | I/O  | MFP14 | Timer0 event counter input/toggle output pin.          |
|        |         | INT3                    | I    | MFP15 | External interrupt 3 input pin.                        |
| 19     | 49      | PC.6                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EBI_AD8                 | I/O  | MFP2  | EBI address/data bus bit 8.                            |
|        |         | SPI1_MOSI               | I/O  | MFP4  | SPI1 MOSI (Master Out, Slave In) pin.                  |
|        |         | UART4_RXD               | I    | MFP5  | UART4 data receiver input pin.                         |
|        |         | UART0_nRTS              | O    | MFP7  | UART0 request to Send output pin.                      |
|        |         | I <sup>2</sup> C1_SMBUS | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
|        |         | UART6_RXD               | I    | MFP9  | UART6 data receiver input pin.                         |
|        |         | EPWM1_CH3               | I/O  | MFP11 | EPWM1 channel 3 output/capture input.                  |
|        |         | BPWM1_CH1               | I/O  | MFP12 | BPWM1 channel 1 output/capture input.                  |
|        |         | TM1                     | I/O  | MFP14 | Timer1 event counter input/toggle output pin.          |
|        |         | INT2                    | I    | MFP15 | External interrupt 2 input pin.                        |
| 20     | 50      | PA.7                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EBI_AD7                 | I/O  | MFP2  | EBI address/data bus bit 7.                            |
|        |         | SPI1_CLK                | I/O  | MFP4  | SPI1 serial clock pin.                                 |
|        |         | UART0_TXD               | O    | MFP7  | UART0 data transmitter output pin.                     |
|        |         | I <sup>2</sup> C1_SCL   | I/O  | MFP8  | I <sup>2</sup> C1 clock pin.                           |
|        |         | QSPI1_MISO1             | I/O  | MFP9  | Quad SPI1 MISO1 (Master In, Slave Out) pin.            |
|        |         | EPWM1_CH4               | I/O  | MFP11 | EPWM1 channel 4 output/capture input.                  |
|        |         | BPWM1_CH2               | I/O  | MFP12 | BPWM1 channel 2 output/capture input.                  |
|        |         | ACMP0_WLAT              | I    | MFP13 | Analog comparator 0 window latch input pin             |
|        |         | TM2                     | I/O  | MFP14 | Timer2 event counter input/toggle output pin.          |
|        |         | INT1                    | I    | MFP15 | External interrupt 1 input pin.                        |

| 64 Pin | 128 Pin | Pin Name                  | Type | MFP   | Description  |
|--------|---------|---------------------------|------|-------|--|
| 21     | 51      | PA.6                      | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |         | EBI_AD6                   | I/O  | MFP2  | EBI address/data bus bit 6.  |
|        |         | SPI1_SS                   | I/O  | MFP4  | SPI1 slave select pin.   |
|        |         | UART0_RXD                 | I    | MFP7  | UART0 data receiver input pin.   |
|        |         | I <sup>2</sup> C1_SDA     | I/O  | MFP8  | I <sup>2</sup> C1 data input/output pin.   |
|        |         | QSPI1_MOSI1               | I/O  | MFP9  | Quad SPI1 MOSI1 (Master Out, Slave In) pin.  |
|        |         | EPWM1_CH5                 | I/O  | MFP11 | EPWM1 channel 5 output/capture input.  |
|        |         | BPWM1_CH3                 | I/O  | MFP12 | BPWM1 channel 3 output/capture input.  |
|        |         | ACMP1_WLAT                | I    | MFP13 | Analog comparator 1 window latch input pin   |
|        |         | TM3                       | I/O  | MFP14 | Timer3 event counter input/toggle output pin.  |
|        |         | INT0                      | I    | MFP15 | External interrupt 0 input pin.  |
| 22     | 52      | V <sub>SS</sub>           | P    | MFP0  | Ground pin for digital circuit.  |
| 23     | 53      | V <sub>DD</sub>           | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit.            |
| 24     | 54      | LDO_CAP                   | A    | MFP0  | LDO output pin.<br><b>Note:</b> This pin needs to be connected with an external capacitor. |
| 25     | 55      | PA.5                      | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |         | QSPI0_MISO1               | I/O  | MFP3  | Quad SPI0 MISO1 (Master In, Slave Out) pin.  |
|        |         | SPI1_I <sup>2</sup> SMCLK | I/O  | MFP4  | SPI1 I <sup>2</sup> S master clock output pin  |
|        |         | UART0_nCTS                | I    | MFP7  | UART0 clear to Send input pin.   |
|        |         | UART5_TXD                 | O    | MFP8  | UART5 data transmitter output pin.   |
|        |         | I <sup>2</sup> C0_SCL     | I/O  | MFP9  | I <sup>2</sup> C0 clock pin.   |
|        |         | CAN0_TXD                  | O    | MFP10 | CAN0 bus transmitter output.   |
|        |         | UART0_TXD                 | O    | MFP11 | UART0 data transmitter output pin.   |
|        |         | BPWM0_CH5                 | I/O  | MFP12 | BPWM0 channel 5 output/capture input.  |
|        |         | EPWM0_CH0                 | I/O  | MFP13 | EPWM0 channel 0 output/capture input.  |
|        |         | QE10_INDEX                | I    | MFP14 | Quadrature encoder 0 index input   |
| 26     | 56      | PA.4                      | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |         | QSPI0_MOSI1               | I/O  | MFP3  | Quad SPI0 MOSI1 (Master Out, Slave In) pin.  |
|        |         | SPI0_I <sup>2</sup> SMCLK | I/O  | MFP4  | SPI0 I <sup>2</sup> S master clock output pin  |
|        |         | SC0_nCD                   | I    | MFP6  | Smart Card 0 card detect pin.  |
|        |         | UART0_nRTS                | O    | MFP7  | UART0 request to Send output pin.  |
|        |         | UART5_RXD                 | I    | MFP8  | UART5 data receiver input pin.   |
|        |         | I <sup>2</sup> C0_SDA     | I/O  | MFP9  | I <sup>2</sup> C0 data input/output pin.   |
|        |         | CAN0_RXD                  | I    | MFP10 | CAN0 bus receiver input.   |

| 64 Pin | 128 Pin | Pin Name                 | Type | MFP   | Description  |
|--------|---------|--------------------------|------|-------|--|
|        |         | UART0_RXD                | I    | MFP11 | UART0 data receiver input pin.                         |
|        |         | BPWM0_CH4                | I/O  | MFP12 | BPWM0 channel 4 output/capture input.                  |
|        |         | EPWM0_CH1                | I/O  | MFP13 | EPWM0 channel 1 output/capture input.                  |
|        |         | QEIO_A                   | I    | MFP14 | Quadrature encoder 0 phase A input                     |
| 27     | 57      | PA.3                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | QSPIO_SS                 | I/O  | MFP3  | Quad SPI0 slave select pin.                            |
|        |         | SPIO_SS                  | I/O  | MFP4  | SPIO slave select pin.                                 |
|        |         | SC0_PWR                  | O    | MFP6  | Smart Card 0 power pin.                                |
|        |         | UART4_TXD                | O    | MFP7  | UART4 data transmitter output pin.                     |
|        |         | UART1_TXD                | O    | MFP8  | UART1 data transmitter output pin.                     |
|        |         | I <sup>2</sup> C1_SCL    | I/O  | MFP9  | I <sup>2</sup> C1 clock pin.                           |
|        |         | I <sup>2</sup> C0_SMBAL  | O    | MFP10 | I <sup>2</sup> C0 SMBus SMBALTER pin                   |
|        |         | BPWM0_CH3                | I/O  | MFP12 | BPWM0 channel 3 output/capture input.                  |
|        |         | EPWM0_CH2                | I/O  | MFP13 | EPWM0 channel 2 output/capture input.                  |
|        |         | QEIO_B                   | I    | MFP14 | Quadrature encoder 0 phase B input                     |
|        |         | EPWM1_BRAKE1             | I    | MFP15 | EPWM1 Brake 1 input pin.                               |
| 28     | 58      | PA.2                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | QSPIO_CLK                | I/O  | MFP3  | Quad SPI0 serial clock pin.                            |
|        |         | SPIO_CLK                 | I/O  | MFP4  | SPIO serial clock pin.                                 |
|        |         | SC0_RST                  | O    | MFP6  | Smart Card 0 reset pin.                                |
|        |         | UART4_RXD                | I    | MFP7  | UART4 data receiver input pin.                         |
|        |         | UART1_RXD                | I    | MFP8  | UART1 data receiver input pin.                         |
|        |         | I <sup>2</sup> C1_SDA    | I/O  | MFP9  | I <sup>2</sup> C1 data input/output pin.               |
|        |         | I <sup>2</sup> C0_SMBSUS | O    | MFP10 | I <sup>2</sup> C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
|        |         | BPWM0_CH2                | I/O  | MFP12 | BPWM0 channel 2 output/capture input.                  |
|        |         | EPWM0_CH3                | I/O  | MFP13 | EPWM0 channel 3 output/capture input.                  |
| 29     | 59      | PA.1                     | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | QSPIO_MISO0              | I/O  | MFP3  | Quad SPI0 MISO0 (Master In, Slave Out) pin.            |
|        |         | SPIO_MISO                | I/O  | MFP4  | SPIO MISO (Master In, Slave Out) pin.                  |
|        |         | SC0_DAT                  | I/O  | MFP6  | Smart Card 0 data pin.                                 |
|        |         | UART0_TXD                | O    | MFP7  | UART0 data transmitter output pin.                     |
|        |         | UART1_nCTS               | I    | MFP8  | UART1 clear to Send input pin.                         |
|        |         | I <sup>2</sup> C2_SCL    | I/O  | MFP9  | I <sup>2</sup> C2 clock pin.                           |
|        |         | CCAP_DATA7               | I    | MFP10 | Camera capture data input bus bit 7.                   |



| 64 Pin | 128 Pin | Pin Name              | Type | MFP               | Description   |
|--------|---------|-----------------------|------|-------------------|---|
|        |         | BPWM0_CH1             | I/O  | MFP12             | BPWM0 channel 1 output/capture input.   |
|        |         | EPWM0_CH4             | I/O  | MFP13             | EPWM0 channel 4 output/capture input.   |
| 30     | 60      | PA.0                  | I/O  | MFP0              | General purpose digital I/O pin.  |
|        |         | QSPI0_MOSI0           | I/O  | MFP3              | Quad SPI0 MOSI0 (Master Out, Slave In) pin.   |
|        |         | SPI0_MOSI             | I/O  | MFP4              | SPI0 MOSI (Master Out, Slave In) pin.   |
|        |         | SC0_CLK               | O    | MFP6              | Smart Card 0 clock pin.   |
|        |         | UART0_RXD             | I    | MFP7              | UART0 data receiver input pin.  |
|        |         | UART1_nRTS            | O    | MFP8              | UART1 request to Send output pin.   |
|        |         | I <sup>2</sup> C2_SDA | I/O  | MFP9              | I <sup>2</sup> C2 data input/output pin.  |
|        |         | CCAP_DATA6            | I    | MFP10             | Camera capture data input bus bit 6.  |
|        |         | BPWM0_CH0             | I/O  | MFP12             | BPWM0 channel 0 output/capture input.   |
|        |         | EPWM0_CH5             | I/O  | MFP13             | EPWM0 channel 5 output/capture input.   |
|        |         | DAC0_ST               | I    | MFP15             | DAC0 external trigger input.  |
|        |         | 31                    | 61   | V <sub>DDIO</sub> | P   |
|        | 62      | PE.14                 | I/O  | MFP0              | General purpose digital I/O pin.  |
|        |         | EBI_AD8               | I/O  | MFP2              | EBI address/data bus bit 8.   |
|        |         | UART2_TXD             | O    | MFP3              | UART2 data transmitter output pin.  |
|        |         | CAN0_TXD              | O    | MFP4              | CAN0 bus transmitter output.  |
|        |         | UART6_TXD             | O    | MFP6              | UART6 data transmitter output pin.  |
|        | 63      | PE.15                 | I/O  | MFP0              | General purpose digital I/O pin.  |
|        |         | EBI_AD9               | I/O  | MFP2              | EBI address/data bus bit 9.   |
|        |         | UART2_RXD             | I    | MFP3              | UART2 data receiver input pin.  |
|        |         | CAN0_RXD              | I    | MFP4              | CAN0 bus receiver input.  |
|        |         | UART6_RXD             | I    | MFP6              | UART6 data receiver input pin.  |
| 32     | 64      | nRESET                | I    | MFP0              | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.<br><b>Note:</b> It is recommended to use 10 kΩ pull-up resistor and 10 μF capacitor on nRESET pin. |
| 33     | 65      | PF.0                  | I/O  | MFP0              | General purpose digital I/O pin.  |
|        |         | UART1_TXD             | O    | MFP2              | UART1 data transmitter output pin.  |
|        |         | I <sup>2</sup> C1_SCL | I/O  | MFP3              | I <sup>2</sup> C1 clock pin.  |
|        |         | UART0_TXD             | O    | MFP4              | UART0 data transmitter output pin.  |
|        |         | BPWM1_CH0             | I/O  | MFP12             | BPWM1 channel 0 output/capture input.   |
|        |         | ICE_DAT               | I/O  | MFP14             | Serial wired debugger data pin.<br><b>Note:</b> It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.  |

| 64 Pin | 128 Pin | Pin Name               | Type | MFP   | Description   |
|--------|---------|------------------------|------|-------|---|
| 34     | 66      | PF.1                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | UART1_RXD              | I    | MFP2  | UART1 data receiver input pin.  |
|        |         | I <sup>2</sup> C1_SDA  | I/O  | MFP3  | I <sup>2</sup> C1 data input/output pin.  |
|        |         | UART0_RXD              | I    | MFP4  | UART0 data receiver input pin.  |
|        |         | BPWM1_CH1              | I/O  | MFP12 | BPWM1 channel 1 output/capture input.   |
|        |         | ICE_CLK                | I/O  | MFP14 | Serial wired debugger clock pin.<br><b>Note:</b> It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin. |
|        | 67      | PD.9                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EBI_AD7                | I/O  | MFP2  | EBI address/data bus bit 7.   |
|        |         | I <sup>2</sup> C2_SCL  | I/O  | MFP3  | I <sup>2</sup> C2 clock pin.  |
|        |         | UART2_nCTS             | I    | MFP4  | UART2 clear to Send input pin.  |
|        |         | UART7_TXD              | O    | MFP5  | UART7 data transmitter output pin.  |
|        |         | CAN2_TXD               | O    | MFP6  | CAN2 bus transmitter output.  |
|        | 68      | PD.8                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EBI_AD6                | I/O  | MFP2  | EBI address/data bus bit 6.   |
|        |         | I <sup>2</sup> C2_SDA  | I/O  | MFP3  | I <sup>2</sup> C2 data input/output pin.  |
|        |         | UART2_nRTS             | O    | MFP4  | UART2 request to Send output pin.   |
|        |         | UART7_RXD              | I    | MFP5  | UART7 data receiver input pin.  |
|        |         | CAN2_RXD               | I    | MFP6  | CAN2 bus receiver input.  |
| 35     | 69      | PC.5                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EBI_AD5                | I/O  | MFP2  | EBI address/data bus bit 5.   |
|        |         | QSPI0_MISO1            | I/O  | MFP4  | Quad SPI0 MISO1 (Master In, Slave Out) pin.   |
|        |         | UART2_TXD              | O    | MFP8  | UART2 data transmitter output pin.  |
|        |         | I <sup>2</sup> C1_SCL  | I/O  | MFP9  | I <sup>2</sup> C1 clock pin.  |
|        |         | CAN0_TXD               | O    | MFP10 | CAN0 bus transmitter output.  |
|        |         | UART4_TXD              | O    | MFP11 | UART4 data transmitter output pin.  |
|        |         | EPWM1_CH0              | I/O  | MFP12 | EPWM1 channel 0 output/capture input.   |
|        |         | CCAP_DATA5             | I    | MFP13 | Camera capture data input bus bit 5.  |
|        |         | QSPI1_SS               | I/O  | MFP14 | Quad SPI1 slave select pin.   |
| 36     | 70      | PC.4                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EBI_AD4                | I/O  | MFP2  | EBI address/data bus bit 4.   |
|        |         | QSPI0_MOSI1            | I/O  | MFP4  | Quad SPI0 MOSI1 (Master Out, Slave In) pin.   |
|        |         | I <sup>2</sup> S0_BCLK | O    | MFP6  | I <sup>2</sup> S0 bit clock output pin.   |
|        |         | SPI1_I2SMCLK           | I/O  | MFP7  | SPI1 I <sup>2</sup> S master clock output pin   |

| 64 Pin                   | 128 Pin | Pin Name                | Type | MFP     | Description  |      |                                  |
|--------------------------|---------|-------------------------|------|---------|--|------|----------------------------------|
|                          |         | UART2_RXD               | I    | MFP8    | UART2 data receiver input pin.                         |      |                                  |
|                          |         | I <sup>2</sup> C1_SDA   | I/O  | MFP9    | I <sup>2</sup> C1 data input/output pin.               |      |                                  |
|                          |         | CAN0_RXD                | I    | MFP10   | CAN0 bus receiver input.                               |      |                                  |
|                          |         | UART4_RXD               | I    | MFP11   | UART4 data receiver input pin.                         |      |                                  |
|                          |         | EPWM1_CH1               | I/O  | MFP12   | EPWM1 channel 1 output/capture input.                  |      |                                  |
|                          |         | CCAP_DATA4              | I    | MFP13   | Camera capture data input bus bit 4.                   |      |                                  |
|                          |         | QSPI1_CLK               | I/O  | MFP14   | Quad SPI1 serial clock pin.                            |      |                                  |
| 37                       | 71      | PC.3                    | I/O  | MFP0    | General purpose digital I/O pin.                       |      |                                  |
|                          |         | EBI_AD3                 | I/O  | MFP2    | EBI address/data bus bit 3.                            |      |                                  |
|                          |         | QSPI0_SS                | I/O  | MFP4    | Quad SPI0 slave select pin.                            |      |                                  |
|                          |         | I <sup>2</sup> S0_MCLK  | O    | MFP6    | I <sup>2</sup> S0 master clock output pin.             |      |                                  |
|                          |         | SPI1_MISO               | I/O  | MFP7    | SPI1 MISO (Master In, Slave Out) pin.                  |      |                                  |
|                          |         | UART2_nRTS              | O    | MFP8    | UART2 request to Send output pin.                      |      |                                  |
|                          |         | I <sup>2</sup> C0_SMBAL | O    | MFP9    | I <sup>2</sup> C0 SMBus SMBALTER pin                   |      |                                  |
|                          |         | CAN1_TXD                | O    | MFP10   | CAN1 bus transmitter output.                           |      |                                  |
|                          |         | UART3_TXD               | O    | MFP11   | UART3 data transmitter output pin.                     |      |                                  |
|                          |         | EPWM1_CH2               | I/O  | MFP12   | EPWM1 channel 2 output/capture input.                  |      |                                  |
|                          |         | CCAP_DATA3              | I    | MFP13   | Camera capture data input bus bit 3.                   |      |                                  |
|                          |         | QSPI1_MISO0             | I/O  | MFP14   | Quad SPI1 MISO0 (Master In, Slave Out) pin.            |      |                                  |
|                          |         | 38                      | 72   | PC.2    | I/O  | MFP0 | General purpose digital I/O pin. |
|                          |         |                         |      | EBI_AD2 | I/O  | MFP2 | EBI address/data bus bit 2.      |
| QSPI0_CLK                | I/O     |                         |      | MFP4    | Quad SPI0 serial clock pin.                            |      |                                  |
| I <sup>2</sup> S0_DI     | I       |                         |      | MFP6    | I <sup>2</sup> S0 data input pin.                      |      |                                  |
| SPI1_MOSI                | I/O     |                         |      | MFP7    | SPI1 MOSI (Master Out, Slave In) pin.                  |      |                                  |
| UART2_nCTS               | I       |                         |      | MFP8    | UART2 clear to Send input pin.                         |      |                                  |
| I <sup>2</sup> C0_SMBSUS | O       |                         |      | MFP9    | I <sup>2</sup> C0 SMBus SMBSUS pin (PMBus CONTROL pin) |      |                                  |
| CAN1_RXD                 | I       |                         |      | MFP10   | CAN1 bus receiver input.                               |      |                                  |
| UART3_RXD                | I       |                         |      | MFP11   | UART3 data receiver input pin.                         |      |                                  |
| EPWM1_CH3                | I/O     |                         |      | MFP12   | EPWM1 channel 3 output/capture input.                  |      |                                  |
| CCAP_DATA2               | I       |                         |      | MFP13   | Camera capture data input bus bit 2.                   |      |                                  |
| QSPI1_MOSI0              | I/O     |                         |      | MFP14   | Quad SPI1 MOSI0 (Master Out, Slave In) pin.            |      |                                  |
| 39                       | 73      |                         |      | PC.1    | I/O  | MFP0 | General purpose digital I/O pin. |
|                          |         |                         |      | EBI_AD1 | I/O  | MFP2 | EBI address/data bus bit 1.      |
|                          |         | QSPI0_MISO0             | I/O  | MFP4    | Quad SPI0 MISO0 (Master In, Slave Out) pin.            |      |                                  |

| 64 Pin | 128 Pin | Pin Name               | Type | MFP   | Description   |
|--------|---------|------------------------|------|-------|---|
|        |         | I <sup>2</sup> S0_DO   | O    | MFP6  | I <sup>2</sup> S0 data output pin.  |
|        |         | SPI1_CLK               | I/O  | MFP7  | SPI1 serial clock pin.  |
|        |         | UART2_TXD              | O    | MFP8  | UART2 data transmitter output pin.  |
|        |         | I <sup>2</sup> C0_SCL  | I/O  | MFP9  | I <sup>2</sup> C0 clock pin.  |
|        |         | CAN2_TXD               | O    | MFP10 | CAN2 bus transmitter output.  |
|        |         | EPWM1_CH4              | I/O  | MFP12 | EPWM1 channel 4 output/capture input.   |
|        |         | CCAP_DATA1             | I    | MFP13 | Camera capture data input bus bit 1.  |
|        |         | ACMP0_O                | O    | MFP14 | Analog comparator 0 output pin.   |
|        |         | EADC0_ST               | I    | MFP15 | EADC0 external trigger input.   |
| 40     | 74      | PC.0                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EBI_AD0                | I/O  | MFP2  | EBI address/data bus bit 0.   |
|        |         | QSPI0_MOSI0            | I/O  | MFP4  | Quad SPI0 MOSI0 (Master Out, Slave In) pin.                                     |
|        |         | I <sup>2</sup> S0_LRCK | O    | MFP6  | I <sup>2</sup> S0 left right channel clock output pin.                          |
|        |         | SPI1_SS                | I/O  | MFP7  | SPI1 slave select pin.  |
|        |         | UART2_RXD              | I    | MFP8  | UART2 data receiver input pin.  |
|        |         | I <sup>2</sup> C0_SDA  | I/O  | MFP9  | I <sup>2</sup> C0 data input/output pin.  |
|        |         | CAN2_RXD               | I    | MFP10 | CAN2 bus receiver input.  |
|        |         | EPWM1_CH5              | I/O  | MFP12 | EPWM1 channel 5 output/capture input.   |
|        |         | CCAP_DATA0             | I    | MFP13 | Camera capture data input bus bit 0.  |
|        |         | ACMP1_O                | O    | MFP14 | Analog comparator 1 output pin.   |
|        |         | EADC1_ST               | I    | MFP15 | EADC1 external trigger input.   |
|        | 75      | V <sub>SS</sub>        | P    | MFP0  | Ground pin for digital circuit.   |
|        | 76      | V <sub>DD</sub>        | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
|        | 77      | PG.9                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EBI_AD0                | I/O  | MFP2  | EBI address/data bus bit 0.   |
|        |         | QSPI1_MISO1            | I/O  | MFP5  | Quad SPI1 MISO1 (Master In, Slave Out) pin.                                     |
|        |         | CCAP_PIXCLK            | I    | MFP7  | Camera capture interface pix clock input pin.                                   |
|        |         | BPWM0_CH5              | I/O  | MFP12 | BPWM0 channel 5 output/capture input.   |
|        | 78      | PG.10                  | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EBI_AD1                | I/O  | MFP2  | EBI address/data bus bit 1.   |
|        |         | QSPI1_MOSI1            | I/O  | MFP5  | Quad SPI1 MOSI1 (Master Out, Slave In) pin.                                     |
|        |         | CCAP_SCLK              | O    | MFP7  | Camera capture interface sensor clock pin.                                      |
|        |         | BPWM0_CH4              | I/O  | MFP12 | BPWM0 channel 4 output/capture input.   |

| 64 Pin | 128 Pin | Pin Name    | Type | MFP   | Description                                 |
|--------|---------|-------------|------|-------|---|
|        | 79      | PG.11       | I/O  | MFP0  | General purpose digital I/O pin.            |
|        |         | EBI_AD2     | I/O  | MFP2  | EBI address/data bus bit 2.                 |
|        |         | QSPI1_SS    | I/O  | MFP5  | Quad SPI1 slave select pin.                 |
|        |         | UART7_TXD   | O    | MFP6  | UART7 data transmitter output pin.          |
|        |         | CCAP_SFIELD | I    | MFP7  | Camera capture interface SFIELD input pin.  |
|        |         | BPWM0_CH3   | I/O  | MFP12 | BPWM0 channel 3 output/capture input.       |
|        | 80      | PG.12       | I/O  | MFP0  | General purpose digital I/O pin.            |
|        |         | EBI_AD3     | I/O  | MFP2  | EBI address/data bus bit 3.                 |
|        |         | QSPI1_CLK   | I/O  | MFP5  | Quad SPI1 serial clock pin.                 |
|        |         | UART7_RXD   | I    | MFP6  | UART7 data receiver input pin.              |
|        |         | CCAP_VSYNC  | I    | MFP7  | Camera capture interface vsync input pin.   |
|        |         | BPWM0_CH2   | I/O  | MFP12 | BPWM0 channel 2 output/capture input.       |
|        | 81      | PG.13       | I/O  | MFP0  | General purpose digital I/O pin.            |
|        |         | EBI_AD4     | I/O  | MFP2  | EBI address/data bus bit 4.                 |
|        |         | QSPI1_MISO0 | I/O  | MFP5  | Quad SPI1 MISO0 (Master In, Slave Out) pin. |
|        |         | UART6_TXD   | O    | MFP6  | UART6 data transmitter output pin.          |
|        |         | CCAP_HSYNC  | I    | MFP7  | Camera capture interface hsync input pin.   |
|        |         | BPWM0_CH1   | I/O  | MFP12 | BPWM0 channel 1 output/capture input.       |
|        | 82      | PG.14       | I/O  | MFP0  | General purpose digital I/O pin.            |
|        |         | EBI_AD5     | I/O  | MFP2  | EBI address/data bus bit 5.                 |
|        |         | QSPI1_MOSI0 | I/O  | MFP5  | Quad SPI1 MOSI0 (Master Out, Slave In) pin. |
|        |         | UART6_RXD   | I    | MFP6  | UART6 data receiver input pin.              |
|        |         | BPWM0_CH0   | I/O  | MFP12 | BPWM0 channel 0 output/capture input.       |
|        | 83      | PG.15       | I/O  | MFP0  | General purpose digital I/O pin.            |
|        |         | CLKO        | O    | MFP14 | Clock Out                                   |
|        |         | EADC0_ST    | I    | MFP15 | EADC0 external trigger input.               |
| 41     |         | PD.3        | I/O  | MFP0  | General purpose digital I/O pin.            |
|        |         | EBI_AD10    | I/O  | MFP2  | EBI address/data bus bit 10.                |
|        |         | SPI0_SS     | I/O  | MFP4  | SPI0 slave select pin.                      |
|        |         | UART3_nRTS  | O    | MFP5  | UART3 request to Send output pin.           |
|        |         | UART0_TXD   | O    | MFP9  | UART0 data transmitter output pin.          |
| 42     |         | PD.2        | I/O  | MFP0  | General purpose digital I/O pin.            |
|        |         | EBI_AD11    | I/O  | MFP2  | EBI address/data bus bit 11.                |
|        |         | SPI0_CLK    | I/O  | MFP4  | SPI0 serial clock pin.                      |

| 64 Pin | 128 Pin | Pin Name               | Type | MFP   | Description                                   |
|--------|---------|------------------------|------|-------|---|
|        |         | UART3_nCTS             | I    | MFP5  | UART3 clear to Send input pin.                |
|        |         | UART0_RXD              | I    | MFP9  | UART0 data receiver input pin.                |
| 43     |         | PD.1                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         | EBI_AD12               | I/O  | MFP2  | EBI address/data bus bit 12.                  |
|        |         | SPI0_MISO              | I/O  | MFP4  | SPI0 MISO (Master In, Slave Out) pin.         |
|        |         | UART3_TXD              | O    | MFP5  | UART3 data transmitter output pin.            |
|        |         | I2C2_SCL               | I/O  | MFP6  | I2C2 clock pin.                               |
| 44     |         | PD.0                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         | EBI_AD13               | I/O  | MFP2  | EBI address/data bus bit 13.                  |
|        |         | SPI0_MOSI              | I/O  | MFP4  | SPI0 MOSI (Master Out, Slave In) pin.         |
|        |         | UART3_RXD              | I    | MFP5  | UART3 data receiver input pin.                |
|        |         | I2C2_SDA               | I/O  | MFP6  | I2C2 data input/output pin.                   |
|        |         | TM2                    | I/O  | MFP14 | Timer2 event counter input/toggle output pin. |
|        | 84      | PD.13                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         | EBI_AD10               | I/O  | MFP2  | EBI address/data bus bit 10.                  |
|        |         | SD0_nCD                | I    | MFP3  | SD/SDIO0 card detect input pin                |
|        |         | SPI0_I2SMCLK           | I/O  | MFP4  | SPI0 I <sup>2</sup> S master clock output pin |
|        |         | SPI1_I2SMCLK           | I/O  | MFP5  | SPI1 I <sup>2</sup> S master clock output pin |
| 45     | 85      | PA.12                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         | I <sup>2</sup> S0_BCLK | O    | MFP2  | I <sup>2</sup> S0 bit clock output pin.       |
|        |         | UART4_TXD              | O    | MFP3  | UART4 data transmitter output pin.            |
|        |         | I <sup>2</sup> C1_SCL  | I/O  | MFP4  | I <sup>2</sup> C1 clock pin.                  |
|        |         | SPI2_SS                | I/O  | MFP5  | SPI2 slave select pin.                        |
|        |         | CAN0_TXD               | O    | MFP6  | CAN0 bus transmitter output.                  |
|        |         | BPWM1_CH2              | I/O  | MFP11 | BPWM1 channel 2 output/capture input.         |
|        |         | QE1_INDEX              | I    | MFP12 | Quadrature encoder 1 index input              |
|        |         | USB_VBUS               | P    | MFP14 | Power supply from USB host or HUB.            |
| 46     | 86      | PA.13                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         | I <sup>2</sup> S0_MCLK | O    | MFP2  | I <sup>2</sup> S0 master clock output pin.    |
|        |         | UART4_RXD              | I    | MFP3  | UART4 data receiver input pin.                |
|        |         | I <sup>2</sup> C1_SDA  | I/O  | MFP4  | I <sup>2</sup> C1 data input/output pin.      |
|        |         | SPI2_CLK               | I/O  | MFP5  | SPI2 serial clock pin.                        |
|        |         | CAN0_RXD               | I    | MFP6  | CAN0 bus receiver input.                      |
|        |         | BPWM1_CH3              | I/O  | MFP11 | BPWM1 channel 3 output/capture input.         |

| 64 Pin | 128 Pin | Pin Name              | Type | MFP   | Description                                  |
|--------|---------|-----------------------|------|-------|--|
|        |         | QE11_A                | I    | MFP12 | Quadrature encoder 1 phase A input           |
|        |         | USB_D-                | A    | MFP14 | USB differential signal D-.                  |
| 47     | 87      | PA.14                 | I/O  | MFP0  | General purpose digital I/O pin.             |
|        |         | I <sup>2</sup> S0_DI  | I    | MFP2  | I <sup>2</sup> S0 data input pin.            |
|        |         | UART0_TXD             | O    | MFP3  | UART0 data transmitter output pin.           |
|        |         | SPI2_MISO             | I/O  | MFP5  | SPI2 MISO (Master In, Slave Out) pin.        |
|        |         | I <sup>2</sup> C2_SCL | I/O  | MFP6  | I <sup>2</sup> C2 clock pin.                 |
|        |         | BPWM1_CH4             | I/O  | MFP11 | BPWM1 channel 4 output/capture input.        |
|        |         | QE11_B                | I    | MFP12 | Quadrature encoder 1 phase B input           |
|        |         | USB_D+                | A    | MFP14 | USB differential signal D+.                  |
| 48     | 88      | PA.15                 | I/O  | MFP0  | General purpose digital I/O pin.             |
|        |         | I <sup>2</sup> S0_DO  | O    | MFP2  | I <sup>2</sup> S0 data output pin.           |
|        |         | UART0_RXD             | I    | MFP3  | UART0 data receiver input pin.               |
|        |         | SPI2_MOSI             | I/O  | MFP5  | SPI2 MOSI (Master Out, Slave In) pin.        |
|        |         | I <sup>2</sup> C2_SDA | I/O  | MFP6  | I <sup>2</sup> C2 data input/output pin.     |
|        |         | BPWM1_CH5             | I/O  | MFP11 | BPWM1 channel 5 output/capture input.        |
|        |         | EPWM0_SYNC_IN         | I    | MFP12 | EPWM0 counter synchronous trigger input pin. |
|        |         | USB_OTG_ID            | I    | MFP14 | USB_ identification.                         |
|        | 89      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        | 90      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        | 91      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        | 92      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        | 93      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        | 94      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        | 95      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        | 96      | NC                    | -    | MFP0  | No connect pin, leave floating.              |
|        | 97      | PE.7                  | I/O  | MFP0  | General purpose digital I/O pin.             |
|        |         | SD0_CMD               | I/O  | MFP3  | SD/SDIO0 command/response pin                |
|        |         | UART5_TXD             | O    | MFP8  | UART5 data transmitter output pin.           |
|        |         | CAN1_TXD              | O    | MFP9  | CAN1 bus transmitter output.                 |
|        |         | QE11_INDEX            | I    | MFP11 | Quadrature encoder 1 index input             |
|        |         | EPWM0_CH0             | I/O  | MFP12 | EPWM0 channel 0 output/capture input.        |
|        |         | BPWM0_CH5             | I/O  | MFP13 | BPWM0 channel 5 output/capture input.        |
|        | 98      | PE.6                  | I/O  | MFP0  | General purpose digital I/O pin.             |

| 64 Pin | 128 Pin | Pin Name   | Type | MFP   | Description                           |
|--------|---------|------------|------|-------|---------------------------------------|
|        |         | SD0_CLK    | O    | MFP3  | SD/SDIO0 clock output pin             |
|        |         | SC0_nCD    | I    | MFP6  | Smart Card 0 card detect pin.         |
|        |         | UART5_RXD  | I    | MFP8  | UART5 data receiver input pin.        |
|        |         | CAN1_RXD   | I    | MFP9  | CAN1 bus receiver input.              |
|        |         | QE11_A     | I    | MFP11 | Quadrature encoder 1 phase A input    |
|        |         | EPWM0_CH1  | I/O  | MFP12 | EPWM0 channel 1 output/capture input. |
|        |         | BPWM0_CH4  | I/O  | MFP13 | BPWM0 channel 4 output/capture input. |
|        | 99      | PE.5       | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |         | EBI_nRD    | O    | MFP2  | EBI read enable output pin.           |
|        |         | SD0_DAT3   | I/O  | MFP3  | SD/SDIO0 data line bit 3.             |
|        |         | SC0_PWR    | O    | MFP6  | Smart Card 0 power pin.               |
|        |         | UART6_TXD  | O    | MFP8  | UART6 data transmitter output pin.    |
|        |         | UART7_nRTS | O    | MFP9  | UART7 request to Send output pin.     |
|        |         | QE11_B     | I    | MFP11 | Quadrature encoder 1 phase B input    |
|        |         | EPWM0_CH2  | I/O  | MFP12 | EPWM0 channel 2 output/capture input. |
|        |         | BPWM0_CH3  | I/O  | MFP13 | BPWM0 channel 3 output/capture input. |
|        | 100     | PE.4       | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |         | EBI_nWR    | O    | MFP2  | EBI write enable output pin.          |
|        |         | SD0_DAT2   | I/O  | MFP3  | SD/SDIO0 data line bit 2.             |
|        |         | SC0_RST    | O    | MFP6  | Smart Card 0 reset pin.               |
|        |         | UART6_RXD  | I    | MFP8  | UART6 data receiver input pin.        |
|        |         | UART7_nCTS | I    | MFP9  | UART7 clear to Send input pin.        |
|        |         | QE10_INDEX | I    | MFP11 | Quadrature encoder 0 index input      |
|        |         | EPWM0_CH3  | I/O  | MFP12 | EPWM0 channel 3 output/capture input. |
|        |         | BPWM0_CH2  | I/O  | MFP13 | BPWM0 channel 2 output/capture input. |
|        | 101     | PE.3       | I/O  | MFP0  | General purpose digital I/O pin.      |
|        |         | EBI_MCLK   | O    | MFP2  | EBI external clock output pin.        |
|        |         | SD0_DAT1   | I/O  | MFP3  | SD/SDIO0 data line bit 1.             |
|        |         | SC0_DAT    | I/O  | MFP6  | Smart Card 0 data pin.                |
|        |         | UART6_nRTS | O    | MFP8  | UART6 request to Send output pin.     |
|        |         | UART7_TXD  | O    | MFP9  | UART7 data transmitter output pin.    |
|        |         | QE10_A     | I    | MFP11 | Quadrature encoder 0 phase A input    |
|        |         | EPWM0_CH4  | I/O  | MFP12 | EPWM0 channel 4 output/capture input. |
|        |         | BPWM0_CH1  | I/O  | MFP13 | BPWM0 channel 1 output/capture input. |



| 64 Pin | 128 Pin | Pin Name               | Type | MFP   | Description   |
|--------|---------|------------------------|------|-------|---|
|        | 102     | PE.2                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EBI_ALE                | O    | MFP2  | EBI address latch enable output pin.  |
|        |         | SD0_DAT0               | I/O  | MFP3  | SD/SDIO0 data line bit 0.   |
|        |         | SC0_CLK                | O    | MFP6  | Smart Card 0 clock pin.   |
|        |         | UART6_nCTS             | I    | MFP8  | UART6 clear to Send input pin.  |
|        |         | UART7_RXD              | I    | MFP9  | UART7 data receiver input pin.  |
|        |         | QEI0_B                 | I    | MFP11 | Quadrature encoder 0 phase B input  |
|        |         | EPWM0_CH5              | I/O  | MFP12 | EPWM0 channel 5 output/capture input.   |
|        |         | BPWM0_CH0              | I/O  | MFP13 | BPWM0 channel 0 output/capture input.   |
|        | 103     | V <sub>SS</sub>        | P    | MFP0  | Ground pin for digital circuit.   |
|        | 104     | V <sub>DD</sub>        | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
|        | 105     | PE.1                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EBI_AD10               | I/O  | MFP2  | EBI address/data bus bit 10.  |
|        |         | QSPI0_MISO0            | I/O  | MFP3  | Quad SPI0 MISO0 (Master In, Slave Out) pin.                                     |
|        |         | I <sup>2</sup> S0_BCLK | O    | MFP5  | I <sup>2</sup> S0 bit clock output pin.   |
|        |         | SPI1_MISO              | I/O  | MFP6  | SPI1 MISO (Master In, Slave Out) pin.   |
|        |         | UART3_TXD              | O    | MFP7  | UART3 data transmitter output pin.  |
|        |         | I <sup>2</sup> C1_SCL  | I/O  | MFP8  | I <sup>2</sup> C1 clock pin.  |
|        |         | UART4_nCTS             | I    | MFP9  | UART4 clear to Send input pin.  |
|        | 106     | PE.0                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EBI_AD11               | I/O  | MFP2  | EBI address/data bus bit 11.  |
|        |         | QSPI0_MOSI0            | I/O  | MFP3  | Quad SPI0 MOSI0 (Master Out, Slave In) pin.                                     |
|        |         | I <sup>2</sup> S0_MCLK | O    | MFP5  | I <sup>2</sup> S0 master clock output pin.                                      |
|        |         | SPI1_MOSI              | I/O  | MFP6  | SPI1 MOSI (Master Out, Slave In) pin.   |
|        |         | UART3_RXD              | I    | MFP7  | UART3 data receiver input pin.  |
|        |         | I <sup>2</sup> C1_SDA  | I/O  | MFP8  | I <sup>2</sup> C1 data input/output pin.  |
|        |         | UART4_nRTS             | O    | MFP9  | UART4 request to Send output pin.   |
|        | 107     | PH.8                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|        |         | EBI_AD12               | I/O  | MFP2  | EBI address/data bus bit 12.  |
|        |         | QSPI0_CLK              | I/O  | MFP3  | Quad SPI0 serial clock pin.   |
|        |         | I <sup>2</sup> S0_DI   | I    | MFP5  | I <sup>2</sup> S0 data input pin.   |
|        |         | SPI1_CLK               | I/O  | MFP6  | SPI1 serial clock pin.  |
|        |         | UART3_nRTS             | O    | MFP7  | UART3 request to Send output pin.   |

| 64 Pin | 128 Pin | Pin Name                 | Type | MFP   | Description  |
|--------|---------|--------------------------|------|-------|--|
|        |         | I <sup>2</sup> C1_SMBAL  | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBALTER pin   |
|        |         | I <sup>2</sup> C2_SCL    | I/O  | MFP9  | I <sup>2</sup> C2 clock pin.   |
|        |         | UART1_TXD                | O    | MFP10 | UART1 data transmitter output pin.   |
|        | 108     | PH.9                     | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |         | EBI_AD13                 | I/O  | MFP2  | EBI address/data bus bit 13.   |
|        |         | QSPIO_SS                 | I/O  | MFP3  | Quad SPI0 slave select pin.  |
|        |         | I <sup>2</sup> S0_DO     | O    | MFP5  | I <sup>2</sup> S0 data output pin.   |
|        |         | SPI1_SS                  | I/O  | MFP6  | SPI1 slave select pin.   |
|        |         | UART3_nCTS               | I    | MFP7  | UART3 clear to Send input pin.   |
|        |         | I <sup>2</sup> C1_SMBSUS | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBSUS pin (PMBus CONTROL pin)                                     |
|        |         | I <sup>2</sup> C2_SDA    | I/O  | MFP9  | I <sup>2</sup> C2 data input/output pin.   |
|        |         | UART1_RXD                | I    | MFP10 | UART1 data receiver input pin.   |
|        | 109     | PH.10                    | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |         | EBI_AD14                 | I/O  | MFP2  | EBI address/data bus bit 14.   |
|        |         | QSPIO_MISO1              | I/O  | MFP3  | Quad SPI0 MISO1 (Master In, Slave Out) pin.  |
|        |         | I <sup>2</sup> S0_LRCK   | O    | MFP5  | I <sup>2</sup> S0 left right channel clock output pin.                                     |
|        |         | SPI1_I2SMCLK             | I/O  | MFP6  | SPI1 I <sup>2</sup> S master clock output pin  |
|        |         | UART4_TXD                | O    | MFP7  | UART4 data transmitter output pin.   |
|        |         | UART0_TXD                | O    | MFP8  | UART0 data transmitter output pin.   |
|        | 110     | PH.11                    | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |         | EBI_AD15                 | I/O  | MFP2  | EBI address/data bus bit 15.   |
|        |         | QSPIO_MOSI1              | I/O  | MFP3  | Quad SPI0 MOSI1 (Master Out, Slave In) pin.  |
|        |         | UART4_RXD                | I    | MFP7  | UART4 data receiver input pin.   |
|        |         | UART0_RXD                | I    | MFP8  | UART0 data receiver input pin.   |
|        |         | EPWM0_CH5                | I/O  | MFP11 | EPWM0 channel 5 output/capture input.  |
|        | 111     | PD.14                    | I/O  | MFP0  | General purpose digital I/O pin.   |
|        |         | EBI_nCS0                 | O    | MFP2  | EBI chip select 0 output pin.  |
|        |         | SPI0_I2SMCLK             | I/O  | MFP5  | SPI0 I <sup>2</sup> S master clock output pin  |
|        |         | EPWM0_CH4                | I/O  | MFP11 | EPWM0 channel 4 output/capture input.  |
| 49     | 112     | V <sub>SS</sub>          | P    | MFP0  | Ground pin for digital circuit.  |
| 50     | 113     | LDO_CAP                  | A    | MFP0  | LDO output pin.<br><b>Note:</b> This pin needs to be connected with an external capacitor. |
| 51     | 114     | V <sub>DD</sub>          | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit.            |
| 52     | 115     | PC.14                    | I/O  | MFP0  | General purpose digital I/O pin.   |

| 64 Pin | 128 Pin | Pin Name                 | Type | MFP   | Description  |
|--------|---------|--------------------------|------|-------|--|
|        |         | EBI_AD11                 | I/O  | MFP2  | EBI address/data bus bit 11.                           |
|        |         | SPI0_I2SMCLK             | I/O  | MFP4  | SPI0 I <sup>2</sup> S master clock output pin          |
|        |         | QSPI0_CLK                | I/O  | MFP6  | Quad SPI0 serial clock pin.                            |
|        |         | EPWM0_SYNC_IN            | I    | MFP11 | EPWM0 counter synchronous trigger input pin.           |
|        |         | ETM_TRACE_CLK            | I    | MFP12 | ETM receiver Trace Clock input pin                     |
|        |         | TM1                      | I/O  | MFP13 | Timer1 event counter input/toggle output pin.          |
|        |         | USB_VBUS_ST              | I    | MFP14 | USB external VBUS regulator status pin.                |
| 53     | 116     | PB.15                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EADC0_CH15               | A    | MFP1  | EADC0 channel 15 analog input.                         |
|        |         | EADC1_CH15               | A    | MFP1  | EADC1 channel 15 analog input.                         |
|        |         | EBI_AD12                 | I/O  | MFP2  | EBI address/data bus bit 12.                           |
|        |         | SPI0_SS                  | I/O  | MFP4  | SPI0 slave select pin.                                 |
|        |         | UART0_nCTS               | I    | MFP6  | UART0 clear to Send input pin.                         |
|        |         | UART3_TXD                | O    | MFP7  | UART3 data transmitter output pin.                     |
|        |         | I <sup>2</sup> C2_SMBAL  | O    | MFP8  | I <sup>2</sup> C2 SMBus SMBALTER pin                   |
|        |         | EPWM0_BRAKE1             | I    | MFP10 | EPWM0 Brake 1 input pin.                               |
|        |         | EPWM1_CH0                | I/O  | MFP11 | EPWM1 channel 0 output/capture input.                  |
|        |         | ETM_TRACE_DATA0          | I    | MFP12 | ETM receiver Trace Data 0 input pin                    |
|        |         | TM0_EXT                  | I/O  | MFP13 | Timer0 external capture input/toggle output pin.       |
|        |         | USB_VBUS_EN              | O    | MFP14 | USB external VBUS regulator enable pin.                |
| 54     | 117     | PB.14                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|        |         | EADC0_CH14               | A    | MFP1  | EADC0 channel 14 analog input.                         |
|        |         | EADC1_CH14               | A    | MFP1  | EADC1 channel 14 analog input.                         |
|        |         | EBI_AD13                 | I/O  | MFP2  | EBI address/data bus bit 13.                           |
|        |         | SPI0_CLK                 | I/O  | MFP4  | SPI0 serial clock pin.                                 |
|        |         | UART0_nRTS               | O    | MFP6  | UART0 request to Send output pin.                      |
|        |         | UART3_RXD                | I    | MFP7  | UART3 data receiver input pin.                         |
|        |         | I <sup>2</sup> C2_SMBSUS | O    | MFP8  | I <sup>2</sup> C2 SMBus SMBSUS pin (PMBus CONTROL pin) |
|        |         | EPWM1_CH1                | I/O  | MFP11 | EPWM1 channel 1 output/capture input.                  |
|        |         | ETM_TRACE_DATA1          | I    | MFP12 | ETM receiver Trace Data 1 input pin                    |
|        |         | TM1_EXT                  | I/O  | MFP13 | Timer1 external capture input/toggle output pin.       |
|        |         | CLKO                     | O    | MFP14 | Clock Out  |
|        |         | USB_VBUS_ST              | I    | MFP15 | USB external VBUS regulator status pin.                |
| 55     | 118     | PB.13                    | I/O  | MFP0  | General purpose digital I/O pin.                       |

| 64 Pin          | 128 Pin | Pin Name              | Type   | MFP   | Description   |
|-----------------|---------|-----------------------|--|-------|---|
|                 |         | EADC0_CH13            | A  | MFP1  | EADC0 channel 13 analog input.  |
|                 |         | EADC1_CH13            | A  | MFP1  | EADC1 channel 13 analog input.  |
|                 |         | ACMP0_P3              | A  | MFP1  | Analog comparator 0 positive input 3 pin.   |
|                 |         | ACMP1_P3              | A  | MFP1  | Analog comparator 1 positive input 3 pin.   |
|                 |         | EBI_AD14              | I/O  | MFP2  | EBI address/data bus bit 14.  |
|                 |         | SPI0_MISO             | I/O  | MFP4  | SPI0 MISO (Master In, Slave Out) pin.   |
|                 |         | UART0_TXD             | O  | MFP6  | UART0 data transmitter output pin.  |
|                 |         | UART3_nRTS            | O  | MFP7  | UART3 request to Send output pin.   |
|                 |         | I <sup>2</sup> C2_SCL | I/O  | MFP8  | I <sup>2</sup> C2 clock pin.  |
|                 |         | CCAP_PIXCLK           | I  | MFP10 | Camera capture interface pix clock input pin.   |
|                 |         | EPWM1_CH2             | I/O  | MFP11 | EPWM1 channel 2 output/capture input.   |
|                 |         | ETM_TRACE_DATA2       | I  | MFP12 | ETM receiver Trace Data 2 input pin   |
|                 |         | TM2_EXT               | I/O  | MFP13 | Timer2 external capture input/toggle output pin.  |
| 56              | 119     | PB.12                 | I/O  | MFP0  | General purpose digital I/O pin.  |
|                 |         | EADC0_CH12            | A  | MFP1  | EADC0 channel 12 analog input.  |
|                 |         | EADC1_CH12            | A  | MFP1  | EADC1 channel 12 analog input.  |
|                 |         | DAC0_OUT              | A  | MFP1  | DAC0 channel analog output.   |
|                 |         | ACMP0_P2              | A  | MFP1  | Analog comparator 0 positive input 2 pin.   |
|                 |         | ACMP1_P2              | A  | MFP1  | Analog comparator 1 positive input 2 pin.   |
|                 |         | EBI_AD15              | I/O  | MFP2  | EBI address/data bus bit 15.  |
|                 |         | SPI0_MOSI             | I/O  | MFP4  | SPI0 MOSI (Master Out, Slave In) pin.   |
|                 |         | UART0_RXD             | I  | MFP6  | UART0 data receiver input pin.  |
|                 |         | UART3_nCTS            | I  | MFP7  | UART3 clear to Send input pin.  |
|                 |         | I <sup>2</sup> C2_SDA | I/O  | MFP8  | I <sup>2</sup> C2 data input/output pin.  |
|                 |         | SD0_nCD               | I  | MFP9  | SD/SDIO0 card detect input pin  |
|                 |         | CCAP_SCLK             | O  | MFP10 | Camera capture interface sensor clock pin.  |
| EPWM1_CH3       | I/O     | MFP11                 | EPWM1 channel 3 output/capture input.            |       |   |
| ETM_TRACE_DATA3 | I       | MFP12                 | ETM receiver Trace Data 3 input pin              |       |   |
| TM3_EXT         | I/O     | MFP13                 | Timer3 external capture input/toggle output pin. |       |   |
| 57              | 120     | AV <sub>DD</sub>      | P  | MFP0  | Power supply for internal analog circuit.   |
| 58              | 121     | V <sub>REF</sub>      | A  | MFP0  | ADC reference voltage input.<br><b>Note:</b> This pin needs to be connected with a 1uF capacitor. |
| 59              | 122     | AV <sub>SS</sub>      | P  | MFP0  | Ground pin for analog circuit.  |
| 60              | 123     | PB.11                 | I/O  | MFP0  | General purpose digital I/O pin.  |

| 64 Pin | 128 Pin | Pin Name                | Type | MFP   | Description                                   |
|--------|---------|-------------------------|------|-------|---|
|        |         | EADC0_CH11              | A    | MFP1  | EADC0 channel 11 analog input.                |
|        |         | EBI_ADR16               | O    | MFP2  | EBI address bus bit 16.                       |
|        |         | UART0_nCTS              | I    | MFP5  | UART0 clear to Send input pin.                |
|        |         | UART4_TXD               | O    | MFP6  | UART4 data transmitter output pin.            |
|        |         | I <sup>2</sup> C1_SCL   | I/O  | MFP7  | I <sup>2</sup> C1 clock pin.                  |
|        |         | CAN0_TXD                | O    | MFP8  | CAN0 bus transmitter output.                  |
|        |         | SPI0_I2SMCLK            | I/O  | MFP9  | SPI0 I <sup>2</sup> S master clock output pin |
|        |         | BPWM1_CH0               | I/O  | MFP10 | BPWM1 channel 0 output/capture input.         |
|        |         | CCAP_SFIELD             | I    | MFP12 | Camera capture interface SFIELD input pin.    |
| 61     | 124     | PB.10                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         | EADC0_CH10              | A    | MFP1  | EADC0 channel 10 analog input.                |
|        |         | EBI_ADR17               | O    | MFP2  | EBI address bus bit 17.                       |
|        |         | UART0_nRTS              | O    | MFP5  | UART0 request to Send output pin.             |
|        |         | UART4_RXD               | I    | MFP6  | UART4 data receiver input pin.                |
|        |         | I <sup>2</sup> C1_SDA   | I/O  | MFP7  | I <sup>2</sup> C1 data input/output pin.      |
|        |         | CAN0_RXD                | I    | MFP8  | CAN0 bus receiver input.                      |
|        |         | BPWM1_CH1               | I/O  | MFP10 | BPWM1 channel 1 output/capture input.         |
|        |         | CCAP_VSYNC              | I    | MFP12 | Camera capture interface vsync input pin.     |
| 62     | 125     | PB.9                    | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         | EADC0_CH9               | A    | MFP1  | EADC0 channel 9 analog input.                 |
|        |         | EBI_ADR18               | O    | MFP2  | EBI address bus bit 18.                       |
|        |         | UART0_TXD               | O    | MFP5  | UART0 data transmitter output pin.            |
|        |         | UART1_nCTS              | I    | MFP6  | UART1 clear to Send input pin.                |
|        |         | I <sup>2</sup> C1_SMBAL | O    | MFP7  | I <sup>2</sup> C1 SMBus SMBALTER pin          |
|        |         | UART7_TXD               | O    | MFP8  | UART7 data transmitter output pin.            |
|        |         | I <sup>2</sup> C0_SCL   | I/O  | MFP9  | I <sup>2</sup> C0 clock pin.                  |
|        |         | BPWM1_CH2               | I/O  | MFP10 | BPWM1 channel 2 output/capture input.         |
|        |         | CAN2_TXD                | O    | MFP12 | CAN2 bus transmitter output.                  |
|        |         | INT7                    | I    | MFP13 | External interrupt 7 input pin.               |
|        |         | CCAP_HSYNC              | I    | MFP14 | Camera capture interface hsync input pin.     |
| 63     | 126     | PB.8                    | I/O  | MFP0  | General purpose digital I/O pin.              |
|        |         | EADC0_CH8               | A    | MFP1  | EADC0 channel 8 analog input.                 |
|        |         | EBI_ADR19               | O    | MFP2  | EBI address bus bit 19.                       |
|        |         | UART0_RXD               | I    | MFP5  | UART0 data receiver input pin.                |

| 64 Pin       | 128 Pin | Pin Name                | Type | MFP   | Description  |
|--------------|---------|-------------------------|------|-------|--|
|              |         | UART1_nRTS              | O    | MFP6  | UART1 request to Send output pin.                      |
|              |         | I <sup>2</sup> C1_SMBUS | O    | MFP7  | I <sup>2</sup> C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
|              |         | UART7_RXD               | I    | MFP8  | UART7 data receiver input pin.                         |
|              |         | I <sup>2</sup> C0_SDA   | I/O  | MFP9  | I <sup>2</sup> C0 data input/output pin.               |
|              |         | BPWM1_CH3               | I/O  | MFP10 | BPWM1 channel 3 output/capture input.                  |
|              |         | CAN2_RXD                | I    | MFP12 | CAN2 bus receiver input.                               |
|              |         | INT6                    | I    | MFP13 | External interrupt 6 input pin.                        |
| 64           | 127     | PB.7                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|              |         | EADC0_CH7               | A    | MFP1  | EADC0 channel 7 analog input.                          |
|              |         | EBI_nWRL                | O    | MFP2  | EBI low byte write enable output pin.                  |
|              |         | CAN1_TXD                | O    | MFP5  | CAN1 bus transmitter output.                           |
|              |         | UART1_TXD               | O    | MFP6  | UART1 data transmitter output pin.                     |
|              |         | EBI_nCS0                | O    | MFP8  | EBI chip select 0 output pin.                          |
|              |         | BPWM1_CH4               | I/O  | MFP10 | BPWM1 channel 4 output/capture input.                  |
|              |         | EPWM1_BRAKE0            | I    | MFP11 | EPWM1 Brake 0 input pin.                               |
|              |         | EPWM1_CH4               | I/O  | MFP12 | EPWM1 channel 4 output/capture input.                  |
|              |         | INT5                    | I    | MFP13 | External interrupt 5 input pin.                        |
|              |         | USB_VBUS_ST             | I    | MFP14 | USB external VBUS regulator status pin.                |
|              |         | ACMP0_O                 | O    | MFP15 | Analog comparator 0 output pin.                        |
|              |         | 1                       | 128  | PB.6  | I/O  |
| EADC0_CH6    | A       |                         |      | MFP1  | EADC0 channel 6 analog input.                          |
| EBI_nWRH     | O       |                         |      | MFP2  | EBI high byte write enable output pin                  |
| CAN1_RXD     | I       |                         |      | MFP5  | CAN1 bus receiver input.                               |
| UART1_RXD    | I       |                         |      | MFP6  | UART1 data receiver input pin.                         |
| EBI_nCS1     | O       |                         |      | MFP8  | EBI chip select 1 output pin.                          |
| BPWM1_CH5    | I/O     |                         |      | MFP10 | BPWM1 channel 5 output/capture input.                  |
| EPWM1_BRAKE1 | I       |                         |      | MFP11 | EPWM1 Brake 1 input pin.                               |
| EPWM1_CH5    | I/O     |                         |      | MFP12 | EPWM1 channel 5 output/capture input.                  |
| INT4         | I       |                         |      | MFP13 | External interrupt 4 input pin.                        |
| USB_VBUS_EN  | O       |                         |      | MFP14 | USB external VBUS regulator enable pin.                |
| ACMP1_O      | O       |                         |      | MFP15 | Analog comparator 1 output pin.                        |

### 4.4 M487KMCAN Pin Description

MFP\* = Multi-function pin. (Refer to section SYS\_GP<sub>x</sub>\_MFPL and SYS\_GP<sub>x</sub>\_MFPH)

PA.0 MFP0 means SYS\_GPA\_MFPL[3:0] = 0x0.

PA.9 MFP5 means SYS\_GPA\_MFPH[7:4] = 0x5.

**Note:** PA.15 MFP can only be as USB\_OTG\_ID when enable full-Speed USB.

| 128 Pin | Pin Name               | Type  | MFP                             | Description                                   |
|---------|------------------------|-------|---------------------------------|---|
| 1       | PB.5                   | I/O   | MFP0                            | General purpose digital I/O pin.              |
|         | EADC0_CH5              | A     | MFP1                            | EADC0 channel 5 analog input.                 |
|         | ACMP1_N                | A     | MFP1                            | Analog comparator 1 negative input pin.       |
|         | EBI_ADR0               | O     | MFP2                            | EBI address bus bit 0.                        |
|         | SD0_DAT3               | I/O   | MFP3                            | SD/SDIO0 data line bit 3.                     |
|         | EMAC_RMII_REFCLK       | I     | MFP4                            | EMAC RMII reference clock input pin.          |
|         | SPI1_MISO              | I/O   | MFP5                            | SPI1 MISO (Master In, Slave Out) pin.         |
|         | I <sup>2</sup> C0_SCL  | I/O   | MFP6                            | I <sup>2</sup> C0 clock pin.                  |
|         | UART5_TXD              | O     | MFP7                            | UART5 data transmitter output pin.            |
|         | USCI1_CTL0             | I/O   | MFP8                            | USCI1 control 0 pin.                          |
|         | SC0_CLK                | O     | MFP9                            | Smart Card 0 clock pin.                       |
|         | I <sup>2</sup> S0_BCLK | O     | MFP10                           | I <sup>2</sup> S0 bit clock output pin.       |
|         | EPWM0_CH0              | I/O   | MFP11                           | EPWM0 channel 0 output/capture input.         |
|         | TM0                    | I/O   | MFP14                           | Timer0 event counter input/toggle output pin. |
| INT0    | I                      | MFP15 | External interrupt 0 input pin. |   |
| 2       | PB.4                   | I/O   | MFP0                            | General purpose digital I/O pin.              |
|         | EADC0_CH4              | A     | MFP1                            | EADC0 channel 4 analog input.                 |
|         | ACMP1_P1               | A     | MFP1                            | Analog comparator 1 positive input 1 pin.     |
|         | EBI_ADR1               | O     | MFP2                            | EBI address bus bit 1.                        |
|         | SD0_DAT2               | I/O   | MFP3                            | SD/SDIO0 data line bit 2.                     |
|         | EMAC_RMII_RXD0         | I     | MFP4                            | EMAC RMII Receive Data bus bit 0.             |
|         | SPI1_MOSI              | I/O   | MFP5                            | SPI1 MOSI (Master Out, Slave In) pin.         |
|         | I <sup>2</sup> C0_SDA  | I/O   | MFP6                            | I <sup>2</sup> C0 data input/output pin.      |
|         | UART5_RXD              | I     | MFP7                            | UART5 data receiver input pin.                |
|         | USCI1_CTL1             | I/O   | MFP8                            | USCI1 control 1 pin.                          |
|         | SC0_DAT                | I/O   | MFP9                            | Smart Card 0 data pin.                        |
|         | I <sup>2</sup> S0_MCLK | O     | MFP10                           | I <sup>2</sup> S0 master clock output pin.    |
|         | EPWM0_CH1              | I/O   | MFP11                           | EPWM0 channel 1 output/capture input.         |

| 128 Pin | Pin Name             | Type  | MFP                             | Description                                     |
|---------|----------------------|-------|---------------------------------|---|
|         | TM1                  | I/O   | MFP14                           | Timer1 event counter input/toggle output pin.   |
|         | INT1                 | I     | MFP15                           | External interrupt 1 input pin.                 |
| 3       | PB.3                 | I/O   | MFP0                            | General purpose digital I/O pin.                |
|         | EADC0_CH3            | A     | MFP1                            | EADC0 channel 3 analog input.                   |
|         | ACMP0_N              | A     | MFP1                            | Analog comparator 0 negative input pin.         |
|         | EBI_ADR2             | O     | MFP2                            | EBI address bus bit 2.                          |
|         | SD0_DAT1             | I/O   | MFP3                            | SD/SDIO0 data line bit 1.                       |
|         | EMAC_RMII_RXD1       | I     | MFP4                            | EMAC RMII Receive Data bus bit 1.               |
|         | SPI1_CLK             | I/O   | MFP5                            | SPI1 serial clock pin.                          |
|         | UART1_TXD            | O     | MFP6                            | UART1 data transmitter output pin.              |
|         | UART5_nRTS           | O     | MFP7                            | UART5 request to Send output pin.               |
|         | USCI1_DAT1           | I/O   | MFP8                            | USCI1 data 1 pin.                               |
|         | SC0_RST              | O     | MFP9                            | Smart Card 0 reset pin.                         |
|         | I <sup>2</sup> S0_DI | I     | MFP10                           | I <sup>2</sup> S0 data input pin.               |
|         | EPWM0_CH2            | I/O   | MFP11                           | EPWM0 channel 2 output/capture input.           |
|         | TM2                  | I/O   | MFP14                           | Timer2 event counter input/toggle output pin.   |
|         | INT2                 | I     | MFP15                           | External interrupt 2 input pin.                 |
| 4       | PB.2                 | I/O   | MFP0                            | General purpose digital I/O pin.                |
|         | EADC0_CH2            | A     | MFP1                            | EADC0 channel 2 analog input.                   |
|         | ACMP0_P1             | A     | MFP1                            | Analog comparator 0 positive input 1 pin.       |
|         | OPA0_O               | A     | MFP1                            | Operational amplifier 0 output pin.             |
|         | EBI_ADR3             | O     | MFP2                            | EBI address bus bit 3.                          |
|         | SD0_DAT0             | I/O   | MFP3                            | SD/SDIO0 data line bit 0.                       |
|         | EMAC_RMII_CRSDV      | I     | MFP4                            | EMAC RMII Carrier Sense/Receive Data input pin. |
|         | SPI1_SS              | I/O   | MFP5                            | SPI1 slave select pin.                          |
|         | UART1_RXD            | I     | MFP6                            | UART1 data receiver input pin.                  |
|         | UART5_nCTS           | I     | MFP7                            | UART5 clear to Send input pin.                  |
|         | USCI1_DAT0           | I/O   | MFP8                            | USCI1 data 0 pin.                               |
|         | SC0_PWR              | O     | MFP9                            | Smart Card 0 power pin.                         |
|         | I <sup>2</sup> S0_DO | O     | MFP10                           | I <sup>2</sup> S0 data output pin.              |
|         | EPWM0_CH3            | I/O   | MFP11                           | EPWM0 channel 3 output/capture input.           |
|         | TM3                  | I/O   | MFP14                           | Timer3 event counter input/toggle output pin.   |
| INT3    | I                    | MFP15 | External interrupt 3 input pin. |   |
| 5       | PC.12                | I/O   | MFP0                            | General purpose digital I/O pin.                |



| 128 Pin | Pin Name              | Type | MFP   | Description                                 |
|---------|-----------------------|------|-------|---|
|         | EBI_ADR4              | O    | MFP2  | EBI address bus bit 4.                      |
|         | UART0_TXD             | O    | MFP3  | UART0 data transmitter output pin.          |
|         | I <sup>2</sup> C0_SCL | I/O  | MFP4  | I <sup>2</sup> C0 clock pin.                |
|         | SPI3_MISO             | I/O  | MFP6  | SPI3 MISO (Master In, Slave Out) pin.       |
|         | SC0_nCD               | I    | MFP9  | Smart Card 0 card detect pin.               |
|         | ECAP1_IC2             | I    | MFP11 | Enhanced capture unit 1 input 2 pin.        |
|         | EPWM1_CH0             | I/O  | MFP12 | EPWM1 channel 0 output/capture input.       |
|         | ACMP0_O               | O    | MFP14 | Analog comparator 0 output pin.             |
| 6       | PC.11                 | I/O  | MFP0  | General purpose digital I/O pin.            |
|         | EBI_ADR5              | O    | MFP2  | EBI address bus bit 5.                      |
|         | UART0_RXD             | I    | MFP3  | UART0 data receiver input pin.              |
|         | I <sup>2</sup> C0_SDA | I/O  | MFP4  | I <sup>2</sup> C0 data input/output pin.    |
|         | SPI3_MOSI             | I/O  | MFP6  | SPI3 MOSI (Master Out, Slave In) pin.       |
|         | ECAP1_IC1             | I    | MFP11 | Enhanced capture unit 1 input 1 pin.        |
|         | EPWM1_CH1             | I/O  | MFP12 | EPWM1 channel 1 output/capture input.       |
|         | ACMP1_O               | O    | MFP14 | Analog comparator 1 output pin.             |
| 7       | PC.10                 | I/O  | MFP0  | General purpose digital I/O pin.            |
|         | EBI_ADR6              | O    | MFP2  | EBI address bus bit 6.                      |
|         | SPI3_CLK              | I/O  | MFP6  | SPI3 serial clock pin.                      |
|         | UART3_TXD             | O    | MFP7  | UART3 data transmitter output pin.          |
|         | CAN1_TXD              | O    | MFP9  | CAN1 bus transmitter output.                |
|         | ECAP1_IC0             | I    | MFP11 | Enhanced capture unit 1 input 0 pin.        |
|         | EPWM1_CH2             | I/O  | MFP12 | EPWM1 channel 2 output/capture input.       |
| 8       | PC.9                  | I/O  | MFP0  | General purpose digital I/O pin.            |
|         | EBI_ADR7              | O    | MFP2  | EBI address bus bit 7.                      |
|         | SPI3_SS               | I/O  | MFP6  | SPI3 slave select pin.                      |
|         | UART3_RXD             | I    | MFP7  | UART3 data receiver input pin.              |
|         | CAN1_RXD              | I    | MFP9  | CAN1 bus receiver input.                    |
|         | EPWM1_CH3             | I/O  | MFP12 | EPWM1 channel 3 output/capture input.       |
| 9       | PB.1                  | I/O  | MFP0  | General purpose digital I/O pin.            |
|         | EADC0_CH1             | A    | MFP1  | EADC0 channel 1 analog input.               |
|         | OPA0_N                | A    | MFP1  | Operational amplifier 0 negative input pin. |
|         | EBI_ADR8              | O    | MFP2  | EBI address bus bit 8.                      |
|         | SD0_CLK               | O    | MFP3  | SD/SDIO0 clock output pin                   |

| 128 Pin | Pin Name               | Type | MFP   | Description   |
|---------|------------------------|------|-------|---|
|         | EMAC_RMII_RXERR        | I    | MFP4  | EMAC RMII Receive Data Error input pin.   |
|         | SPI1_I2SMCLK           | I/O  | MFP5  | SPI1 I <sup>2</sup> S master clock output pin                                   |
|         | SPI3_I2SMCLK           | I/O  | MFP6  | SPI3 I <sup>2</sup> S master clock output pin                                   |
|         | UART2_TXD              | O    | MFP7  | UART2 data transmitter output pin.  |
|         | USCI1_CLK              | I/O  | MFP8  | USCI1 clock pin.  |
|         | I <sup>2</sup> C1_SCL  | I/O  | MFP9  | I <sup>2</sup> C1 clock pin.  |
|         | I <sup>2</sup> S0_LRCK | O    | MFP10 | I <sup>2</sup> S0 left right channel clock output pin.                          |
|         | EPWM0_CH4              | I/O  | MFP11 | EPWM0 channel 4 output/capture input.   |
|         | EPWM1_CH4              | I/O  | MFP12 | EPWM1 channel 4 output/capture input.   |
|         | EPWM0_BRAKE0           | I    | MFP13 | EPWM0 Brake 0 input pin.  |
| 10      | PB.0                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|         | EADC0_CH0              | A    | MFP1  | EADC0 channel 0 analog input.   |
|         | OPA0_P                 | A    | MFP1  | Operational amplifier 0 positive input pin.                                     |
|         | EBI_ADR9               | O    | MFP2  | EBI address bus bit 9.  |
|         | SD0_CMD                | I/O  | MFP3  | SD/SDIO0 command/response pin   |
|         | UART2_RXD              | I    | MFP7  | UART2 data receiver input pin.  |
|         | SPI0_I2SMCLK           | I/O  | MFP8  | SPI0 I <sup>2</sup> S master clock output pin                                   |
|         | I <sup>2</sup> C1_SDA  | I/O  | MFP9  | I <sup>2</sup> C1 data input/output pin.  |
|         | EPWM0_CH5              | I/O  | MFP11 | EPWM0 channel 5 output/capture input.   |
|         | EPWM1_CH5              | I/O  | MFP12 | EPWM1 channel 5 output/capture input.   |
|         | EPWM0_BRAKE1           | I    | MFP13 | EPWM0 Brake 1 input pin.  |
| 11      | V <sub>SS</sub>        | P    | MFP0  | Ground pin for digital circuit.   |
| 12      | V <sub>DD</sub>        | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 13      | PA.11                  | I/O  | MFP0  | General purpose digital I/O pin.  |
|         | ACMP0_P0               | A    | MFP1  | Analog comparator 0 positive input 0 pin.                                       |
|         | EBI_nRD                | O    | MFP2  | EBI read enable output pin.   |
|         | SC2_PWR                | O    | MFP3  | Smart Card 2 power pin.   |
|         | SPI2_SS                | I/O  | MFP4  | SPI2 slave select pin.  |
|         | SD1_DAT3               | I/O  | MFP5  | SD/SDIO1 data line bit 3.   |
|         | USCI0_CLK              | I/O  | MFP6  | USCI0 clock pin.  |
|         | I <sup>2</sup> C2_SCL  | I/O  | MFP7  | I <sup>2</sup> C2 clock pin.  |
|         | BPWM0_CH0              | I/O  | MFP9  | BPWM0 channel 0 output/capture input.   |
|         | EPWM0_SYNC_OUT         | O    | MFP10 | EPWM0 counter synchronous trigger output pin.                                   |

| 128 Pin | Pin Name              | Type | MFP   | Description                                   |
|---------|-----------------------|------|-------|---|
|         | TM0_EXT               | I/O  | MFP13 | Timer0 event counter input/toggle output pin. |
|         | DAC1_ST               | I    | MFP14 | DAC1 external trigger input.                  |
| 14      | PA.10                 | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | ACMP1_P0              | A    | MFP1  | Analog comparator 1 positive input 0 pin.     |
|         | OPA1_O                | A    | MFP1  | Operational amplifier 1 output pin.           |
|         | EBI_nWR               | O    | MFP2  | EBI write enable output pin.                  |
|         | SC2_RST               | O    | MFP3  | Smart Card 2 reset pin.                       |
|         | SPI2_CLK              | I/O  | MFP4  | SPI2 serial clock pin.                        |
|         | SD1_DAT2              | I/O  | MFP5  | SD/SDIO1 data line bit 2.                     |
|         | USCI0_DAT0            | I/O  | MFP6  | USCI0 data 0 pin.                             |
|         | I <sup>2</sup> C2_SDA | I/O  | MFP7  | I <sup>2</sup> C2 data input/output pin.      |
|         | BPWM0_CH1             | I/O  | MFP9  | BPWM0 channel 1 output/capture input.         |
|         | QEI1_INDEX            | I    | MFP10 | Quadrature encoder 1 index input              |
|         | ECAP0_IC0             | I    | MFP11 | Enhanced capture unit 0 input 0 pin.          |
|         | TM1_EXT               | I/O  | MFP13 | Timer1 event counter input/toggle output pin. |
|         | DAC0_ST               | I    | MFP14 | DAC0 external trigger input.                  |
|         |                       |      |       |   |
| 15      | PA.9                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | OPA1_N                | A    | MFP1  | Operational amplifier 1 negative input pin.   |
|         | EBI_MCLK              | O    | MFP2  | EBI external clock output pin.                |
|         | SC2_DAT               | I/O  | MFP3  | Smart Card 2 data pin.                        |
|         | SPI2_MISO             | I/O  | MFP4  | SPI2 MISO (Master In, Slave Out) pin.         |
|         | SD1_DAT1              | I/O  | MFP5  | SD/SDIO1 data line bit 1.                     |
|         | USCI0_DAT1            | I/O  | MFP6  | USCI0 data 1 pin.                             |
|         | UART1_TXD             | O    | MFP7  | UART1 data transmitter output pin.            |
|         | BPWM0_CH2             | I/O  | MFP9  | BPWM0 channel 2 output/capture input.         |
|         | QEI1_A                | I    | MFP10 | Quadrature encoder 1 phase A input            |
|         | ECAP0_IC1             | I    | MFP11 | Enhanced capture unit 0 input 1 pin.          |
|         | TM2_EXT               | I/O  | MFP13 | Timer2 event counter input/toggle output pin. |
|         |                       |      |       |   |
| 16      | PA.8                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | OPA1_P                | A    | MFP1  | Operational amplifier 1 positive input pin.   |
|         | EBI_ALE               | O    | MFP2  | EBI address latch enable output pin.          |
|         | SC2_CLK               | O    | MFP3  | Smart Card 2 clock pin.                       |

| 128 Pin | Pin Name     | Type | MFP   | Description                                   |
|---------|--------------|------|-------|---|
|         | SPI2_MOSI    | I/O  | MFP4  | SPI2 MOSI (Master Out, Slave In) pin.         |
|         | SD1_DAT0     | I/O  | MFP5  | SD/SDIO1 data line bit 0.                     |
|         | USCI0_CTL1   | I/O  | MFP6  | USCI0 control 1 pin.                          |
|         | UART1_RXD    | I    | MFP7  | UART1 data receiver input pin.                |
|         | BPWM0_CH3    | I/O  | MFP9  | BPWM0 channel 3 output/capture input.         |
|         | QE11_B       | I    | MFP10 | Quadrature encoder 1 phase B input            |
|         | ECAP0_IC2    | I    | MFP11 | Enhanced capture unit 0 input 2 pin.          |
|         | TM3_EXT      | I/O  | MFP13 | Timer3 event counter input/toggle output pin. |
|         | INT4         | I    | MFP15 | External interrupt 4 input pin.               |
| 17      | PC.13        | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | EBI_ADR10    | O    | MFP2  | EBI address bus bit 10.                       |
|         | SC2_nCD      | I    | MFP3  | Smart Card 2 card detect pin.                 |
|         | SPI2_I2SMCLK | I/O  | MFP4  | SPI2 I <sup>2</sup> S master clock output pin |
|         | CAN1_TXD     | O    | MFP5  | CAN1 bus transmitter output.                  |
|         | USCI0_CTL0   | I/O  | MFP6  | USCI0 control 0 pin.                          |
|         | UART2_TXD    | O    | MFP7  | UART2 data transmitter output pin.            |
|         | BPWM0_CH4    | I/O  | MFP9  | BPWM0 channel 4 output/capture input.         |
|         | CLKO         | O    | MFP13 | Clock Out                                     |
|         | EADC0_ST     | I    | MFP14 | EADC0 external trigger input.                 |
| 18      | PD.12        | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | OPA2_O       | A    | MFP1  | Operational amplifier 2 output pin.           |
|         | EBI_nCS0     | O    | MFP2  | EBI chip select 0 output pin.                 |
|         | CAN1_RXD     | I    | MFP5  | CAN1 bus receiver input.                      |
|         | UART2_RXD    | I    | MFP7  | UART2 data receiver input pin.                |
|         | BPWM0_CH5    | I/O  | MFP9  | BPWM0 channel 5 output/capture input.         |
|         | QE10_INDEX   | I    | MFP10 | Quadrature encoder 0 index input              |
|         | CLKO         | O    | MFP13 | Clock Out                                     |
|         | EADC0_ST     | I    | MFP14 | EADC0 external trigger input.                 |
|         | INT5         | I    | MFP15 | External interrupt 5 input pin.               |
| 19      | PD.11        | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | OPA2_N       | A    | MFP1  | Operational amplifier 2 negative input pin.   |
|         | EBI_nCS1     | O    | MFP2  | EBI chip select 1 output pin.                 |
|         | UART1_TXD    | O    | MFP3  | UART1 data transmitter output pin.            |
|         | CAN0_TXD     | O    | MFP4  | CAN0 bus transmitter output.                  |

| 128 Pin | Pin Name                | Type | MFP   | Description   |
|---------|-------------------------|------|-------|---|
|         | QEIO_A                  | I    | MFP10 | Quadrature encoder 0 phase A input                    |
|         | INT6                    | I    | MFP15 | External interrupt 6 input pin.                       |
| 20      | PD.10                   | I/O  | MFP0  | General purpose digital I/O pin.                      |
|         | OPA2_P                  | A    | MFP1  | Operational amplifier 2 positive input pin.           |
|         | EBI_nCS2                | O    | MFP2  | EBI chip select 2 output pin.                         |
|         | UART1_RXD               | I    | MFP3  | UART1 data receiver input pin.                        |
|         | CAN0_RXD                | I    | MFP4  | CAN0 bus receiver input.                              |
|         | QEIO_B                  | I    | MFP10 | Quadrature encoder 0 phase B input                    |
|         | INT7                    | I    | MFP15 | External interrupt 7 input pin.                       |
| 21      | PG.2                    | I/O  | MFP0  | General purpose digital I/O pin.                      |
|         | EBI_ADR11               | O    | MFP2  | EBI address bus bit 11.                               |
|         | SPI2_SS                 | I/O  | MFP3  | SPI2 slave select pin.                                |
|         | I <sup>2</sup> C0_SMBAL | O    | MFP4  | I <sup>2</sup> C0 SMBus SMBALTER pin                  |
|         | I <sup>2</sup> C1_SCL   | I/O  | MFP5  | I <sup>2</sup> C1 clock pin.                          |
|         | TM0                     | I/O  | MFP13 | Timer0 event counter input/toggle output pin.         |
| 22      | PG.3                    | I/O  | MFP0  | General purpose digital I/O pin.                      |
|         | EBI_ADR12               | O    | MFP2  | EBI address bus bit 12.                               |
|         | SPI2_CLK                | I/O  | MFP3  | SPI2 serial clock pin.                                |
|         | I <sup>2</sup> C0_SMBUS | O    | MFP4  | I <sup>2</sup> C0 SMBus SMBUS pin (PMBus CONTROL pin) |
|         | I <sup>2</sup> C1_SDA   | I/O  | MFP5  | I <sup>2</sup> C1 data input/output pin.              |
|         | TM1                     | I/O  | MFP13 | Timer1 event counter input/toggle output pin.         |
| 23      | PG.4                    | I/O  | MFP0  | General purpose digital I/O pin.                      |
|         | EBI_ADR13               | O    | MFP2  | EBI address bus bit 13.                               |
|         | SPI2_MISO               | I/O  | MFP3  | SPI2 MISO (Master In, Slave Out) pin.                 |
|         | TM2                     | I/O  | MFP13 | Timer2 event counter input/toggle output pin.         |
| 24      | PF.11                   | I/O  | MFP0  | General purpose digital I/O pin.                      |
|         | EBI_ADR14               | O    | MFP2  | EBI address bus bit 14.                               |
|         | SPI2_MOSI               | I/O  | MFP3  | SPI2 MOSI (Master Out, Slave In) pin.                 |
|         | TAMPER5                 | I/O  | MFP10 | TAMPER detector loop pin 5.                           |
|         | TM3                     | I/O  | MFP13 | Timer3 event counter input/toggle output pin.         |
| 25      | PF.10                   | I/O  | MFP0  | General purpose digital I/O pin.                      |
|         | EBI_ADR15               | O    | MFP2  | EBI address bus bit 15.                               |
|         | SC0_nCD                 | I    | MFP3  | Smart Card 0 card detect pin.                         |
|         | I <sup>2</sup> S0_BCLK  | O    | MFP4  | I <sup>2</sup> S0 bit clock output pin.               |

| 128 Pin              | Pin Name               | Type | MFP   | Description   |
|----------------------|------------------------|------|-------|---|
|                      | SPI0_I2SMCLK           | I/O  | MFP5  | SPI0 I <sup>2</sup> S master clock output pin                                   |
|                      | TAMPER4                | I/O  | MFP10 | TAMPER detector loop pin 4.   |
| 26                   | PF.9                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|                      | EBI_ADR16              | O    | MFP2  | EBI address bus bit 16.   |
|                      | SC0_PWR                | O    | MFP3  | Smart Card 0 power pin.   |
|                      | I <sup>2</sup> S0_MCLK | O    | MFP4  | I <sup>2</sup> S0 master clock output pin.                                      |
|                      | SPI0_SS                | I/O  | MFP5  | SPI0 slave select pin.  |
|                      | TAMPER3                | I/O  | MFP10 | TAMPER detector loop pin 3.   |
|                      | 27                     | PF.8 | I/O   | MFP0  |
| EBI_ADR17            |                        | O    | MFP2  | EBI address bus bit 17.   |
| SC0_RST              |                        | O    | MFP3  | Smart Card 0 reset pin.   |
| I <sup>2</sup> S0_DI |                        | I    | MFP4  | I <sup>2</sup> S0 data input pin.   |
| SPI0_CLK             |                        | I/O  | MFP5  | SPI0 serial clock pin.  |
| TAMPER2              |                        | I/O  | MFP10 | TAMPER detector loop pin 2.   |
| 28                   |                        | PF.7 | I/O   | MFP0  |
|                      | EBI_ADR18              | O    | MFP2  | EBI address bus bit 18.   |
|                      | SC0_DAT                | I/O  | MFP3  | Smart Card 0 data pin.  |
|                      | I <sup>2</sup> S0_DO   | O    | MFP4  | I <sup>2</sup> S0 data output pin.  |
|                      | SPI0_MISO              | I/O  | MFP5  | SPI0 MISO (Master In, Slave Out) pin.   |
|                      | UART4_TXD              | O    | MFP6  | UART4 data transmitter output pin.  |
|                      | TAMPER1                | I/O  | MFP10 | TAMPER detector loop pin 1.   |
| 29                   | PF.6                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|                      | EBI_ADR19              | O    | MFP2  | EBI address bus bit 19.   |
|                      | SC0_CLK                | O    | MFP3  | Smart Card 0 clock pin.   |
|                      | I <sup>2</sup> S0_LRCK | O    | MFP4  | I <sup>2</sup> S0 left right channel clock output pin.                          |
|                      | SPI0_MOSI              | I/O  | MFP5  | SPI0 MOSI (Master Out, Slave In) pin.   |
|                      | UART4_RXD              | I    | MFP6  | UART4 data receiver input pin.  |
|                      | EBI_nCS0               | O    | MFP7  | EBI chip select 0 output pin.   |
|                      | TAMPER0                | I/O  | MFP10 | TAMPER detector loop pin 0.   |
| 30                   | V <sub>DD</sub>        | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 31                   | PF.5                   | I/O  | MFP0  | General purpose digital I/O pin.  |
|                      | UART2_RXD              | I    | MFP2  | UART2 data receiver input pin.  |
|                      | UART2_nCTS             | I    | MFP4  | UART2 clear to Send input pin.  |

| 128 Pin | Pin Name              | Type | MFP   | Description  |
|---------|-----------------------|------|-------|--|
|         | BPWM0_CH4             | I/O  | MFP8  | BPWM0 channel 4 output/capture input.              |
|         | EPWM0_SYNC_OUT        | O    | MFP9  | EPWM0 counter synchronous trigger output pin.      |
|         | X32_IN                | I    | MFP10 | External 32.768 kHz crystal input pin.             |
|         | EADC0_ST              | I    | MFP11 | EADC0 external trigger input.                      |
| 32      | PF.4                  | I/O  | MFP0  | General purpose digital I/O pin.                   |
|         | UART2_TXD             | O    | MFP2  | UART2 data transmitter output pin.                 |
|         | UART2_nRTS            | O    | MFP4  | UART2 request to Send output pin.                  |
|         | BPWM0_CH5             | I/O  | MFP8  | BPWM0 channel 5 output/capture input.              |
|         | X32_OUT               | O    | MFP10 | External 32.768 kHz crystal output pin.            |
| 33      | PH.4                  | I/O  | MFP0  | General purpose digital I/O pin.                   |
|         | EBI_ADR3              | O    | MFP2  | EBI address bus bit 3.                             |
|         | SPI1_MISO             | I/O  | MFP3  | SPI1 MISO (Master In, Slave Out) pin.              |
| 34      | PH.5                  | I/O  | MFP0  | General purpose digital I/O pin.                   |
|         | EBI_ADR2              | O    | MFP2  | EBI address bus bit 2.                             |
|         | SPI1_MOSI             | I/O  | MFP3  | SPI1 MOSI (Master Out, Slave In) pin.              |
| 35      | PH.6                  | I/O  | MFP0  | General purpose digital I/O pin.                   |
|         | EBI_ADR1              | O    | MFP2  | EBI address bus bit 1.                             |
|         | SPI1_CLK              | I/O  | MFP3  | SPI1 serial clock pin.                             |
| 36      | PH.7                  | I/O  | MFP0  | General purpose digital I/O pin.                   |
|         | EBI_ADR0              | O    | MFP2  | EBI address bus bit 0.                             |
|         | SPI1_SS               | I/O  | MFP3  | SPI1 slave select pin.                             |
| 37      | PF.3                  | I/O  | MFP0  | General purpose digital I/O pin.                   |
|         | EBI_nCS0              | O    | MFP2  | EBI chip select 0 output pin.                      |
|         | UART0_TXD             | O    | MFP3  | UART0 data transmitter output pin.                 |
|         | I <sup>2</sup> C0_SCL | I/O  | MFP4  | I <sup>2</sup> C0 clock pin.                       |
|         | XT1_IN                | I    | MFP10 | External 4~24 MHz (high speed) crystal input pin.  |
|         | BPWM1_CH0             | I/O  | MFP11 | BPWM1 channel 0 output/capture input.              |
| 38      | PF.2                  | I/O  | MFP0  | General purpose digital I/O pin.                   |
|         | EBI_nCS1              | O    | MFP2  | EBI chip select 1 output pin.                      |
|         | UART0_RXD             | I    | MFP3  | UART0 data receiver input pin.                     |
|         | I <sup>2</sup> C0_SDA | I/O  | MFP4  | I <sup>2</sup> C0 data input/output pin.           |
|         | QSPI0_CLK             | I/O  | MFP5  | QSPI0 serial clock pin.                            |
|         | XT1_OUT               | O    | MFP10 | External 4~24 MHz (high speed) crystal output pin. |
|         | BPWM1_CH1             | I/O  | MFP11 | BPWM1 channel 1 output/capture input.              |

| 128 Pin     | Pin Name               | Type  | MFP                         | Description   |
|-------------|------------------------|-------|-----------------------------|---|
| 39          | V <sub>SS</sub>        | P     | MFP0                        | Ground pin for digital circuit.   |
| 40          | V <sub>DD</sub>        | P     | MFP0                        | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 41          | PE.8                   | I/O   | MFP0                        | General purpose digital I/O pin.  |
|             | EBI_ADR10              | O     | MFP2                        | EBI address bus bit 10.   |
|             | EMAC_RMII_MDC          | O     | MFP3                        | EMAC RMII PHY Management Clock output pin.                                      |
|             | I <sup>2</sup> S0_BCLK | O     | MFP4                        | I <sup>2</sup> S0 bit clock output pin.   |
|             | SPI2_CLK               | I/O   | MFP5                        | SPI2 serial clock pin.  |
|             | USCI1_CTL1             | I/O   | MFP6                        | USCI1 control 1 pin.  |
|             | UART2_TXD              | O     | MFP7                        | UART2 data transmitter output pin.  |
|             | EPWM0_CH0              | I/O   | MFP10                       | EPWM0 channel 0 output/capture input.   |
|             | EPWM0_BRAKE0           | I     | MFP11                       | EPWM0 Brake 0 input pin.  |
|             | ECAP0_IC0              | I     | MFP12                       | Enhanced capture unit 0 input 0 pin.  |
| TRACE_DATA3 | O                      | MFP14 | ETM Trace Data 3 output pin |   |
| 42          | PE.9                   | I/O   | MFP0                        | General purpose digital I/O pin.  |
|             | EBI_ADR11              | O     | MFP2                        | EBI address bus bit 11.   |
|             | EMAC_RMII_MDIO         | I/O   | MFP3                        | EMAC RMII PHY Management Data pin.  |
|             | I <sup>2</sup> S0_MCLK | O     | MFP4                        | I <sup>2</sup> S0 master clock output pin.                                      |
|             | SPI2_MISO              | I/O   | MFP5                        | SPI2 MISO (Master In, Slave Out) pin.   |
|             | USCI1_CTL0             | I/O   | MFP6                        | USCI1 control 0 pin.  |
|             | UART2_RXD              | I     | MFP7                        | UART2 data receiver input pin.  |
|             | EPWM0_CH1              | I/O   | MFP10                       | EPWM0 channel 1 output/capture input.   |
|             | EPWM0_BRAKE1           | I     | MFP11                       | EPWM0 Brake 1 input pin.  |
|             | ECAP0_IC1              | I     | MFP12                       | Enhanced capture unit 0 input 1 pin.  |
| TRACE_DATA2 | O                      | MFP14 | ETM Trace Data 2 output pin |   |
| 43          | PE.10                  | I/O   | MFP0                        | General purpose digital I/O pin.  |
|             | EBI_ADR12              | O     | MFP2                        | EBI address bus bit 12.   |
|             | EMAC_RMII_TXD0         | O     | MFP3                        | EMAC RMII Transmit Data bus bit 0.  |
|             | I <sup>2</sup> S0_DI   | I     | MFP4                        | I <sup>2</sup> S0 data input pin.   |
|             | SPI2_MOSI              | I/O   | MFP5                        | SPI2 MOSI (Master Out, Slave In) pin.   |
|             | USCI1_DAT0             | I/O   | MFP6                        | USCI1 data 0 pin.   |
|             | UART3_TXD              | O     | MFP7                        | UART3 data transmitter output pin.  |
|             | EPWM0_CH2              | I/O   | MFP10                       | EPWM0 channel 2 output/capture input.   |
|             | EPWM1_BRAKE0           | I     | MFP11                       | EPWM1 Brake 0 input pin.  |



| 128 Pin | Pin Name               | Type | MFP   | Description  |
|---------|------------------------|------|-------|--|
|         | ECAP0_IC2              | I    | MFP12 | Enhanced capture unit 0 input 2 pin.                   |
|         | TRACE_DATA1            | O    | MFP14 | ETM Trace Data 1 output pin                            |
| 44      | PE.11                  | I/O  | MFP0  | General purpose digital I/O pin.                       |
|         | EBI_ADR13              | O    | MFP2  | EBI address bus bit 13.                                |
|         | EMAC_RMII_TXD1         | O    | MFP3  | EMAC RMII Transmit Data bus bit 1.                     |
|         | I <sup>2</sup> S0_DO   | O    | MFP4  | I <sup>2</sup> S0 data output pin.                     |
|         | SPI2_SS                | I/O  | MFP5  | SPI2 slave select pin.                                 |
|         | USCI1_DAT1             | I/O  | MFP6  | USCI1 data 1 pin.                                      |
|         | UART3_RXD              | I    | MFP7  | UART3 data receiver input pin.                         |
|         | UART1_nCTS             | I    | MFP8  | UART1 clear to Send input pin.                         |
|         | EPWM0_CH3              | I/O  | MFP10 | EPWM0 channel 3 output/capture input.                  |
|         | EPWM1_BRAKE1           | I    | MFP11 | EPWM1 Brake 1 input pin.                               |
|         | ECAP1_IC2              | I    | MFP13 | Enhanced capture unit 1 input 2 pin.                   |
|         | TRACE_DATA0            | O    | MFP14 | ETM Trace Data 0 output pin                            |
| 45      | PE.12                  | I/O  | MFP0  | General purpose digital I/O pin.                       |
|         | EBI_ADR14              | O    | MFP2  | EBI address bus bit 14.                                |
|         | EMAC_RMII_TXEN         | O    | MFP3  | EMAC RMII Transmit Enable output pin.                  |
|         | I <sup>2</sup> S0_LRCK | O    | MFP4  | I <sup>2</sup> S0 left right channel clock output pin. |
|         | SPI2_I2SMCLK           | I/O  | MFP5  | SPI2 I <sup>2</sup> S master clock output pin          |
|         | USCI1_CLK              | I/O  | MFP6  | USCI1 clock pin.                                       |
|         | UART1_nRTS             | O    | MFP8  | UART1 request to Send output pin.                      |
|         | EPWM0_CH4              | I/O  | MFP10 | EPWM0 channel 4 output/capture input.                  |
|         | ECAP1_IC1              | I    | MFP13 | Enhanced capture unit 1 input 1 pin.                   |
|         | TRACE_CLK              | O    | MFP14 | ETM Trace Clock output pin                             |
| 46      | PE.13                  | I/O  | MFP0  | General purpose digital I/O pin.                       |
|         | EBI_ADR15              | O    | MFP2  | EBI address bus bit 15.                                |
|         | EMAC_PPS               | O    | MFP3  | EMAC Pulse Per Second output pin.                      |
|         | I <sup>2</sup> C0_SCL  | I/O  | MFP4  | I <sup>2</sup> C0 clock pin.                           |
|         | UART4_nRTS             | O    | MFP5  | UART4 request to Send output pin.                      |
|         | UART1_TXD              | O    | MFP8  | UART1 data transmitter output pin.                     |
|         | EPWM0_CH5              | I/O  | MFP10 | EPWM0 channel 5 output/capture input.                  |
|         | EPWM1_CH0              | I/O  | MFP11 | EPWM1 channel 0 output/capture input.                  |
|         | BPWM1_CH5              | I/O  | MFP12 | BPWM1 channel 5 output/capture input.                  |
|         | ECAP1_IC0              | I    | MFP13 | Enhanced capture unit 1 input 0 pin.                   |

| 128 Pin                  | Pin Name                | Type | MFP   | Description  |
|--------------------------|-------------------------|------|-------|--|
| 47                       | PC.8                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|                          | EBI_ADR16               | O    | MFP2  | EBI address bus bit 16.                                |
|                          | EMAC_RMII_REFCLK        | I    | MFP3  | EMAC RMII reference clock input pin.                   |
|                          | I <sup>2</sup> C0_SDA   | I/O  | MFP4  | I <sup>2</sup> C0 data input/output pin.               |
|                          | UART4_nCTS              | I    | MFP5  | UART4 clear to Send input pin.                         |
|                          | UART1_RXD               | I    | MFP8  | UART1 data receiver input pin.                         |
|                          | EPWM1_CH1               | I/O  | MFP11 | EPWM1 channel 1 output/capture input.                  |
|                          | BPWM1_CH4               | I/O  | MFP12 | BPWM1 channel 4 output/capture input.                  |
| 48                       | PC.7                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|                          | EBI_AD9                 | I/O  | MFP2  | EBI address/data bus bit 9.                            |
|                          | EMAC_RMII_RXD0          | I    | MFP3  | EMAC RMII Receive Data bus bit 0.                      |
|                          | SPI1_MISO               | I/O  | MFP4  | SPI1 MISO (Master In, Slave Out) pin.                  |
|                          | UART4_TXD               | O    | MFP5  | UART4 data transmitter output pin.                     |
|                          | SC2_PWR                 | O    | MFP6  | Smart Card 2 power pin.                                |
|                          | UART0_nCTS              | I    | MFP7  | UART0 clear to Send input pin.                         |
|                          | I <sup>2</sup> C1_SMBAL | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBALTER pin                   |
|                          | EPWM1_CH2               | I/O  | MFP11 | EPWM1 channel 2 output/capture input.                  |
|                          | BPWM1_CH0               | I/O  | MFP12 | BPWM1 channel 0 output/capture input.                  |
|                          | TM0                     | I/O  | MFP14 | Timer0 event counter input/toggle output pin.          |
|                          | INT3                    | I    | MFP15 | External interrupt 3 input pin.                        |
|                          | 49                      | PC.6 | I/O   | MFP0   |
| EBI_AD8                  |                         | I/O  | MFP2  | EBI address/data bus bit 8.                            |
| EMAC_RMII_RXD1           |                         | I    | MFP3  | EMAC RMII Receive Data bus bit 1.                      |
| SPI1_MOSI                |                         | I/O  | MFP4  | SPI1 MOSI (Master Out, Slave In) pin.                  |
| UART4_RXD                |                         | I    | MFP5  | UART4 data receiver input pin.                         |
| SC2_RST                  |                         | O    | MFP6  | Smart Card 2 reset pin.                                |
| UART0_nRTS               |                         | O    | MFP7  | UART0 request to Send output pin.                      |
| I <sup>2</sup> C1_SMBSUS |                         | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| EPWM1_CH3                |                         | I/O  | MFP11 | EPWM1 channel 3 output/capture input.                  |
| BPWM1_CH1                |                         | I/O  | MFP12 | BPWM1 channel 1 output/capture input.                  |
| TM1                      |                         | I/O  | MFP14 | Timer1 event counter input/toggle output pin.          |
| INT2                     |                         | I    | MFP15 | External interrupt 2 input pin.                        |
| 50                       | PA.7                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|                          | EBI_AD7                 | I/O  | MFP2  | EBI address/data bus bit 7.                            |

| 128 Pin | Pin Name              | Type | MFP   | Description  |
|---------|-----------------------|------|-------|--|
|         | EMAC_RMII_CRSDV       | I    | MFP3  | EMAC RMII Carrier Sense/Receive Data input pin.  |
|         | SPI1_CLK              | I/O  | MFP4  | SPI1 serial clock pin.   |
|         | SC2_DAT               | I/O  | MFP6  | Smart Card 2 data pin.   |
|         | UART0_TXD             | O    | MFP7  | UART0 data transmitter output pin.   |
|         | I <sup>2</sup> C1_SCL | I/O  | MFP8  | I <sup>2</sup> C1 clock pin.   |
|         | EPWM1_CH4             | I/O  | MFP11 | EPWM1 channel 4 output/capture input.  |
|         | BPWM1_CH2             | I/O  | MFP12 | BPWM1 channel 2 output/capture input.  |
|         | ACMP0_WLAT            | I    | MFP13 | Analog comparator 0 window latch input pin   |
|         | TM2                   | I/O  | MFP14 | Timer2 event counter input/toggle output pin.  |
|         | INT1                  | I    | MFP15 | External interrupt 1 input pin.  |
| 51      | PA.6                  | I/O  | MFP0  | General purpose digital I/O pin.   |
|         | EBI_AD6               | I/O  | MFP2  | EBI address/data bus bit 6.  |
|         | EMAC_RMII_RXERR       | I    | MFP3  | EMAC RMII Receive Data Error input pin.  |
|         | SPI1_SS               | I/O  | MFP4  | SPI1 slave select pin.   |
|         | SD1_nCD               | I    | MFP5  | SD/SDIO1 card detect input pin   |
|         | SC2_CLK               | O    | MFP6  | Smart Card 2 clock pin.  |
|         | UART0_RXD             | I    | MFP7  | UART0 data receiver input pin.   |
|         | I <sup>2</sup> C1_SDA | I/O  | MFP8  | I <sup>2</sup> C1 data input/output pin.   |
|         | EPWM1_CH5             | I/O  | MFP11 | EPWM1 channel 5 output/capture input.  |
|         | BPWM1_CH3             | I/O  | MFP12 | BPWM1 channel 3 output/capture input.  |
|         | ACMP1_WLAT            | I    | MFP13 | Analog comparator 1 window latch input pin   |
|         | TM3                   | I/O  | MFP14 | Timer3 event counter input/toggle output pin.  |
|         | INT0                  | I    | MFP15 | External interrupt 0 input pin.  |
| 52      | V <sub>SS</sub>       | P    | MFP0  | Ground pin for digital circuit.  |
| 53      | V <sub>DD</sub>       | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit.            |
| 54      | LDO_CAP               | A    | MFP0  | LDO output pin.<br><b>Note:</b> This pin needs to be connected with an external capacitor. |
| 55      | PA.5                  | I/O  | MFP0  | General purpose digital I/O pin.   |
|         | SPIM_D2               | I/O  | MFP2  | SPIM data 2 pin for Quad Mode I/O.   |
|         | QSPI0_MISO1           | I/O  | MFP3  | QSPI0 MISO1 (Master In, Slave Out) pin.  |
|         | SPI1_I2SMCLK          | I/O  | MFP4  | SPI1 I <sup>2</sup> S master clock output pin  |
|         | SD1_CMD               | I/O  | MFP5  | SD/SDIO1 command/response pin  |
|         | SC2_nCD               | I    | MFP6  | Smart Card 2 card detect pin.  |

| 128 Pin | Pin Name              | Type | MFP   | Description                                   |
|---------|-----------------------|------|-------|---|
|         | UART0_nCTS            | I    | MFP7  | UART0 clear to Send input pin.                |
|         | UART5_TXD             | O    | MFP8  | UART5 data transmitter output pin.            |
|         | I <sup>2</sup> C0_SCL | I/O  | MFP9  | I <sup>2</sup> C0 clock pin.                  |
|         | CAN0_TXD              | O    | MFP10 | CAN0 bus transmitter output.                  |
|         | BPWM0_CH5             | I/O  | MFP12 | BPWM0 channel 5 output/capture input.         |
|         | EPWM0_CH0             | I/O  | MFP13 | EPWM0 channel 0 output/capture input.         |
|         | QEI0_INDEX            | I    | MFP14 | Quadrature encoder 0 index input              |
| 56      | PA.4                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | SPIM_D3               | I/O  | MFP2  | SPIM data 3 pin for Quad Mode I/O.            |
|         | QSPI0_MOSI1           | I/O  | MFP3  | QSPI0 MOSI1 (Master Out, Slave In) pin.       |
|         | SPI0_I2SMCLK          | I/O  | MFP4  | SPI0 I <sup>2</sup> S master clock output pin |
|         | SD1_CLK               | O    | MFP5  | SD/SDIO1 clock output pin                     |
|         | SC0_nCD               | I    | MFP6  | Smart Card 0 card detect pin.                 |
|         | UART0_nRTS            | O    | MFP7  | UART0 request to Send output pin.             |
|         | UART5_RXD             | I    | MFP8  | UART5 data receiver input pin.                |
|         | I <sup>2</sup> C0_SDA | I/O  | MFP9  | I <sup>2</sup> C0 data input/output pin.      |
|         | CAN0_RXD              | I    | MFP10 | CAN0 bus receiver input.                      |
|         | BPWM0_CH4             | I/O  | MFP12 | BPWM0 channel 4 output/capture input.         |
|         | EPWM0_CH1             | I/O  | MFP13 | EPWM0 channel 1 output/capture input.         |
|         | QEI0_A                | I    | MFP14 | Quadrature encoder 0 phase A input            |
| 57      | PA.3                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | SPIM_SS               | I/O  | MFP2  | SPIM slave select pin.                        |
|         | QSPI0_SS              | I/O  | MFP3  | QSPI0 slave select pin.                       |
|         | SPI0_SS               | I/O  | MFP4  | SPI0 slave select pin.                        |
|         | SD1_DAT3              | I/O  | MFP5  | SD/SDIO1 data line bit 3.                     |
|         | SC0_PWR               | O    | MFP6  | Smart Card 0 power pin.                       |
|         | UART4_TXD             | O    | MFP7  | UART4 data transmitter output pin.            |
|         | UART1_TXD             | O    | MFP8  | UART1 data transmitter output pin.            |
|         | I <sup>2</sup> C1_SCL | I/O  | MFP9  | I <sup>2</sup> C1 clock pin.                  |
|         | BPWM0_CH3             | I/O  | MFP12 | BPWM0 channel 3 output/capture input.         |
|         | EPWM0_CH2             | I/O  | MFP13 | EPWM0 channel 2 output/capture input.         |
|         | QEI0_B                | I    | MFP14 | Quadrature encoder 0 phase B input            |
| 58      | PA.2                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | SPIM_CLK              | I/O  | MFP2  | SPIM serial clock pin.                        |

| 128 Pin | Pin Name              | Type | MFP   | Description                              |
|---------|-----------------------|------|-------|--|
|         | QSPI0_CLK             | I/O  | MFP3  | QSPI0 serial clock pin.                  |
|         | SPI0_CLK              | I/O  | MFP4  | SPI0 serial clock pin.                   |
|         | SD1_DAT2              | I/O  | MFP5  | SD/SDIO1 data line bit 2.                |
|         | SC0_RST               | O    | MFP6  | Smart Card 0 reset pin.                  |
|         | UART4_RXD             | I    | MFP7  | UART4 data receiver input pin.           |
|         | UART1_RXD             | I    | MFP8  | UART1 data receiver input pin.           |
|         | I <sup>2</sup> C1_SDA | I/O  | MFP9  | I <sup>2</sup> C1 data input/output pin. |
|         | BPWM0_CH2             | I/O  | MFP12 | BPWM0 channel 2 output/capture input.    |
|         | EPWM0_CH3             | I/O  | MFP13 | EPWM0 channel 3 output/capture input.    |
| 59      | PA.1                  | I/O  | MFP0  | General purpose digital I/O pin.         |
|         | SPIM_MISO             | I/O  | MFP2  | SPIM MISO (Master In, Slave Out) pin.    |
|         | QSPI0_MISO0           | I/O  | MFP3  | QSPI0 MISO0 (Master In, Slave Out) pin.  |
|         | SPI0_MISO             | I/O  | MFP4  | SPI0 MISO (Master In, Slave Out) pin.    |
|         | SD1_DAT1              | I/O  | MFP5  | SD/SDIO1 data line bit 1.                |
|         | SC0_DAT               | I/O  | MFP6  | Smart Card 0 data pin.                   |
|         | UART0_TXD             | O    | MFP7  | UART0 data transmitter output pin.       |
|         | UART1_nCTS            | I    | MFP8  | UART1 clear to Send input pin.           |
|         | I <sup>2</sup> C2_SCL | I/O  | MFP9  | I <sup>2</sup> C2 clock pin.             |
|         | BPWM0_CH1             | I/O  | MFP12 | BPWM0 channel 1 output/capture input.    |
|         | EPWM0_CH4             | I/O  | MFP13 | EPWM0 channel 4 output/capture input.    |
|         | DAC1_ST               | I    | MFP15 | DAC1 external trigger input.             |
| 60      | PA.0                  | I/O  | MFP0  | General purpose digital I/O pin.         |
|         | SPIM_MOSI             | I/O  | MFP2  | SPIM MOSI (Master Out, Slave In) pin.    |
|         | QSPI0_MOSI0           | I/O  | MFP3  | QSPI0 MOSI0 (Master Out, Slave In) pin.  |
|         | SPI0_MOSI             | I/O  | MFP4  | SPI0 MOSI (Master Out, Slave In) pin.    |
|         | SD1_DAT0              | I/O  | MFP5  | SD/SDIO1 data line bit 0.                |
|         | SC0_CLK               | O    | MFP6  | Smart Card 0 clock pin.                  |
|         | UART0_RXD             | I    | MFP7  | UART0 data receiver input pin.           |
|         | UART1_nRTS            | O    | MFP8  | UART1 request to Send output pin.        |
|         | I <sup>2</sup> C2_SDA | I/O  | MFP9  | I <sup>2</sup> C2 data input/output pin. |
|         | BPWM0_CH0             | I/O  | MFP12 | BPWM0 channel 0 output/capture input.    |
|         | EPWM0_CH5             | I/O  | MFP13 | EPWM0 channel 5 output/capture input.    |
|         | DAC0_ST               | I    | MFP15 | DAC0 external trigger input.             |
| 61      | V <sub>DDIO</sub>     | P    | MFP0  | Power supply for PA.0~PA.5.              |

| 128 Pin | Pin Name              | Type | MFP   | Description   |
|---------|-----------------------|------|-------|---|
| 62      | PE.14                 | I/O  | MFP0  | General purpose digital I/O pin.  |
|         | EBI_AD8               | I/O  | MFP2  | EBI address/data bus bit 8.   |
|         | UART2_TXD             | O    | MFP3  | UART2 data transmitter output pin.  |
|         | CAN0_TXD              | O    | MFP4  | CAN0 bus transmitter output.  |
|         | SD1_nCD               | I    | MFP5  | SD/SDIO1 card detect input pin  |
| 63      | PE.15                 | I/O  | MFP0  | General purpose digital I/O pin.  |
|         | EBI_AD9               | I/O  | MFP2  | EBI address/data bus bit 9.   |
|         | UART2_RXD             | I    | MFP3  | UART2 data receiver input pin.  |
|         | CAN0_RXD              | I    | MFP4  | CAN0 bus receiver input.  |
| 64      | nRESET                | I    | MFP0  | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.<br><b>Note:</b> It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin. |
| 65      | PF.0                  | I/O  | MFP0  | General purpose digital I/O pin.  |
|         | UART1_TXD             | O    | MFP2  | UART1 data transmitter output pin.  |
|         | I <sup>2</sup> C1_SCL | I/O  | MFP3  | I <sup>2</sup> C1 clock pin.  |
|         | BPWM1_CH0             | I/O  | MFP12 | BPWM1 channel 0 output/capture input.   |
|         | ICE_DAT               | O    | MFP14 | Serial wired debugger data pin.<br><b>Note:</b> It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.  |
| 66      | PF.1                  | I/O  | MFP0  | General purpose digital I/O pin.  |
|         | UART1_RXD             | I    | MFP2  | UART1 data receiver input pin.  |
|         | I <sup>2</sup> C1_SDA | I/O  | MFP3  | I <sup>2</sup> C1 data input/output pin.  |
|         | BPWM1_CH1             | I/O  | MFP12 | BPWM1 channel 1 output/capture input.   |
|         | ICE_CLK               | I    | MFP14 | Serial wired debugger clock pin.<br><b>Note:</b> It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.   |
| 67      | PD.9                  | I/O  | MFP0  | General purpose digital I/O pin.  |
|         | EBI_AD7               | I/O  | MFP2  | EBI address/data bus bit 7.   |
|         | I <sup>2</sup> C2_SCL | I/O  | MFP3  | I <sup>2</sup> C2 clock pin.  |
|         | UART2_nCTS            | I    | MFP4  | UART2 clear to Send input pin.  |
| 68      | PD.8                  | I/O  | MFP0  | General purpose digital I/O pin.  |
|         | EBI_AD6               | I/O  | MFP2  | EBI address/data bus bit 6.   |
|         | I <sup>2</sup> C2_SDA | I/O  | MFP3  | I <sup>2</sup> C2 data input/output pin.  |
|         | UART2_nRTS            | O    | MFP4  | UART2 request to Send output pin.   |
| 69      | PC.5                  | I/O  | MFP0  | General purpose digital I/O pin.  |
|         | EBI_AD5               | I/O  | MFP2  | EBI address/data bus bit 5.   |

| 128 Pin | Pin Name                | Type | MFP   | Description                                   |
|---------|-------------------------|------|-------|---|
|         | SPIM_D2                 | I/O  | MFP3  | SPIM data 2 pin for Quad Mode I/O.            |
|         | QSPI0_MISO1             | I/O  | MFP4  | QSPI0 MISO1 (Master In, Slave Out) pin.       |
|         | UART2_TXD               | O    | MFP8  | UART2 data transmitter output pin.            |
|         | I <sup>2</sup> C1_SCL   | I/O  | MFP9  | I <sup>2</sup> C1 clock pin.                  |
|         | CAN0_TXD                | O    | MFP10 | CAN0 bus transmitter output.                  |
|         | UART4_TXD               | O    | MFP11 | UART4 data transmitter output pin.            |
|         | EPWM1_CH0               | I/O  | MFP12 | EPWM1 channel 0 output/capture input.         |
| 70      | PC.4                    | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | EBI_AD4                 | I/O  | MFP2  | EBI address/data bus bit 4.                   |
|         | SPIM_D3                 | I/O  | MFP3  | SPIM data 3 pin for Quad Mode I/O.            |
|         | QSPI0_MOSI1             | I/O  | MFP4  | QSPI0 MOSI1 (Master Out, Slave In) pin.       |
|         | SC1_nCD                 | I    | MFP5  | Smart Card 1 card detect pin.                 |
|         | I <sup>2</sup> S0_BCLK  | O    | MFP6  | I <sup>2</sup> S0 bit clock output pin.       |
|         | SPI1_I2SMCLK            | I/O  | MFP7  | SPI1 I <sup>2</sup> S master clock output pin |
|         | UART2_RXD               | I    | MFP8  | UART2 data receiver input pin.                |
|         | I <sup>2</sup> C1_SDA   | I/O  | MFP9  | I <sup>2</sup> C1 data input/output pin.      |
|         | CAN0_RXD                | I    | MFP10 | CAN0 bus receiver input.                      |
|         | UART4_RXD               | I    | MFP11 | UART4 data receiver input pin.                |
|         | EPWM1_CH1               | I/O  | MFP12 | EPWM1 channel 1 output/capture input.         |
| 71      | PC.3                    | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | EBI_AD3                 | I/O  | MFP2  | EBI address/data bus bit 3.                   |
|         | SPIM_SS                 | I/O  | MFP3  | SPIM slave select pin.                        |
|         | QSPI0_SS                | I/O  | MFP4  | QSPI0 slave select pin.                       |
|         | SC1_PWR                 | O    | MFP5  | Smart Card 1 power pin.                       |
|         | I <sup>2</sup> S0_MCLK  | O    | MFP6  | I <sup>2</sup> S0 master clock output pin.    |
|         | SPI1_MISO               | I/O  | MFP7  | SPI1 MISO (Master In, Slave Out) pin.         |
|         | UART2_nRTS              | O    | MFP8  | UART2 request to Send output pin.             |
|         | I <sup>2</sup> C0_SMBAL | O    | MFP9  | I <sup>2</sup> C0 SMBus SMBALTER pin          |
|         | CAN1_TXD                | O    | MFP10 | CAN1 bus transmitter output.                  |
|         | UART3_TXD               | O    | MFP11 | UART3 data transmitter output pin.            |
|         | EPWM1_CH2               | I/O  | MFP12 | EPWM1 channel 2 output/capture input.         |
| 72      | PC.2                    | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | EBI_AD2                 | I/O  | MFP2  | EBI address/data bus bit 2.                   |
|         | SPIM_CLK                | I/O  | MFP3  | SPIM serial clock pin.                        |

| 128 Pin | Pin Name                 | Type  | MFP                             | Description   |
|---------|--------------------------|-------|---------------------------------|---|
|         | QSPI0_CLK                | I/O   | MFP4                            | QSPI0 serial clock pin.   |
|         | SC1_RST                  | O     | MFP5                            | Smart Card 1 reset pin.   |
|         | I <sup>2</sup> S0_DI     | I     | MFP6                            | I <sup>2</sup> S0 data input pin.   |
|         | SPI1_MOSI                | I/O   | MFP7                            | SPI1 MOSI (Master Out, Slave In) pin.   |
|         | UART2_nCTS               | I     | MFP8                            | UART2 clear to Send input pin.  |
|         | I <sup>2</sup> C0_SMBSUS | O     | MFP9                            | I <sup>2</sup> C0 SMBus SMBSUS pin (PMBus CONTROL pin)                          |
|         | CAN1_RXD                 | I     | MFP10                           | CAN1 bus receiver input.  |
|         | UART3_RXD                | I     | MFP11                           | UART3 data receiver input pin.  |
|         | EPWM1_CH3                | I/O   | MFP12                           | EPWM1 channel 3 output/capture input.   |
| 73      | PC.1                     | I/O   | MFP0                            | General purpose digital I/O pin.  |
|         | EBI_AD1                  | I/O   | MFP2                            | EBI address/data bus bit 1.   |
|         | SPIM_MISO                | I/O   | MFP3                            | SPIM MISO (Master In, Slave Out) pin.   |
|         | QSPI0_MISO0              | I/O   | MFP4                            | QSPI0 MISO0 (Master In, Slave Out) pin.   |
|         | SC1_DAT                  | I/O   | MFP5                            | Smart Card 1 data pin.  |
|         | I <sup>2</sup> S0_DO     | O     | MFP6                            | I <sup>2</sup> S0 data output pin.  |
|         | SPI1_CLK                 | I/O   | MFP7                            | SPI1 serial clock pin.  |
|         | UART2_TXD                | O     | MFP8                            | UART2 data transmitter output pin.  |
|         | I <sup>2</sup> C0_SCL    | I/O   | MFP9                            | I <sup>2</sup> C0 clock pin.  |
|         | EPWM1_CH4                | I/O   | MFP12                           | EPWM1 channel 4 output/capture input.   |
|         | ACMP0_O                  | O     | MFP14                           | Analog comparator 0 output pin.   |
| 74      | PC.0                     | I/O   | MFP0                            | General purpose digital I/O pin.  |
|         | EBI_AD0                  | I/O   | MFP2                            | EBI address/data bus bit 0.   |
|         | SPIM_MOSI                | I/O   | MFP3                            | SPIM MOSI (Master Out, Slave In) pin.   |
|         | QSPI0_MOSI0              | I/O   | MFP4                            | QSPI0 MOSI0 (Master Out, Slave In) pin.   |
|         | SC1_CLK                  | O     | MFP5                            | Smart Card 1 clock pin.   |
|         | I <sup>2</sup> S0_LRCK   | O     | MFP6                            | I <sup>2</sup> S0 left right channel clock output pin.                          |
|         | SPI1_SS                  | I/O   | MFP7                            | SPI1 slave select pin.  |
|         | UART2_RXD                | I     | MFP8                            | UART2 data receiver input pin.  |
|         | I <sup>2</sup> C0_SDA    | I/O   | MFP9                            | I <sup>2</sup> C0 data input/output pin.  |
|         | EPWM1_CH5                | I/O   | MFP12                           | EPWM1 channel 5 output/capture input.   |
| ACMP1_O | O                        | MFP14 | Analog comparator 1 output pin. |   |
| 75      | V <sub>SS</sub>          | P     | MFP0                            | Ground pin for digital circuit.   |
| 76      | V <sub>DD</sub>          | P     | MFP0                            | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |



| 128 Pin | Pin Name               | Type | MFP   | Description                                   |
|---------|------------------------|------|-------|---|
| 77      | PG.9                   | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | EBI_AD0                | I/O  | MFP2  | EBI address/data bus bit 0.                   |
|         | SD1_DAT3               | I/O  | MFP3  | SD/SDIO1 data line bit 3.                     |
|         | SPI_M_D2               | I/O  | MFP4  | SPI_M data 2 pin for Quad Mode I/O.           |
|         | BPWM0_CH5              | I/O  | MFP12 | BPWM0 channel 5 output/capture input.         |
| 78      | PG.10                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | EBI_AD1                | I/O  | MFP2  | EBI address/data bus bit 1.                   |
|         | SD1_DAT2               | I/O  | MFP3  | SD/SDIO1 data line bit 2.                     |
|         | SPI_M_D3               | I/O  | MFP4  | SPI_M data 3 pin for Quad Mode I/O.           |
|         | BPWM0_CH4              | I/O  | MFP12 | BPWM0 channel 4 output/capture input.         |
| 79      | NC                     | -    | -     | No connection.                                |
| 80      | PG.12                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | EBI_AD3                | I/O  | MFP2  | EBI address/data bus bit 3.                   |
|         | SD1_DAT0               | I/O  | MFP3  | SD/SDIO1 data line bit 0.                     |
|         | SPI_M_CLK              | I/O  | MFP4  | SPI_M serial clock pin.                       |
|         | BPWM0_CH2              | I/O  | MFP12 | BPWM0 channel 2 output/capture input.         |
| 81      | NC                     | -    | -     | No connection.                                |
| 82      | PG.14                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | EBI_AD5                | I/O  | MFP2  | EBI address/data bus bit 5.                   |
|         | SD1_CLK                | O    | MFP3  | SD/SDIO1 clock output pin                     |
|         | SPI_M_MOSI             | I/O  | MFP4  | SPI_M MOSI (Master Out, Slave In) pin.        |
|         | BPWM0_CH0              | I/O  | MFP12 | BPWM0 channel 0 output/capture input.         |
| 83      | PG.15                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | SD1_nCD                | I    | MFP3  | SD/SDIO1 card detect input pin                |
|         | CLKO                   | O    | MFP14 | Clock Out                                     |
|         | EADC0_ST               | I    | MFP15 | EADC0 external trigger input.                 |
| 84      | PD.13                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | EBI_AD10               | I/O  | MFP2  | EBI address/data bus bit 10.                  |
|         | SD0_nCD                | I    | MFP3  | SD/SDIO0 card detect input pin                |
|         | SPI0_I2SMCLK           | I/O  | MFP4  | SPI0 I <sup>2</sup> S master clock output pin |
|         | SPI1_I2SMCLK           | I/O  | MFP5  | SPI1 I <sup>2</sup> S master clock output pin |
|         | SC2_nCD                | I    | MFP7  | Smart Card 2 card detect pin.                 |
| 85      | PA.12                  | I/O  | MFP0  | General purpose digital I/O pin.              |
|         | I <sup>2</sup> S0_BCLK | O    | MFP2  | I <sup>2</sup> S0 bit clock output pin.       |

| 128 Pin | Pin Name               | Type  | MFP                         | Description                                |
|---------|------------------------|-------|-----------------------------|--|
|         | UART4_TXD              | O     | MFP3                        | UART4 data transmitter output pin.         |
|         | I <sup>2</sup> C1_SCL  | I/O   | MFP4                        | I <sup>2</sup> C1 clock pin.               |
|         | SPI2_SS                | I/O   | MFP5                        | SPI2 slave select pin.                     |
|         | CAN0_TXD               | O     | MFP6                        | CAN0 bus transmitter output.               |
|         | SC2_PWR                | O     | MFP7                        | Smart Card 2 power pin.                    |
|         | BPWM1_CH2              | I/O   | MFP11                       | BPWM1 channel 2 output/capture input.      |
|         | QEI1_INDEX             | I     | MFP12                       | Quadrature encoder 1 index input           |
|         | USB_VBUS               | P     | MFP14                       | Power supply from USB host or HUB.         |
| 86      | PA.13                  | I/O   | MFP0                        | General purpose digital I/O pin.           |
|         | I <sup>2</sup> S0_MCLK | O     | MFP2                        | I <sup>2</sup> S0 master clock output pin. |
|         | UART4_RXD              | I     | MFP3                        | UART4 data receiver input pin.             |
|         | I <sup>2</sup> C1_SDA  | I/O   | MFP4                        | I <sup>2</sup> C1 data input/output pin.   |
|         | SPI2_CLK               | I/O   | MFP5                        | SPI2 serial clock pin.                     |
|         | CAN0_RXD               | I     | MFP6                        | CAN0 bus receiver input.                   |
|         | SC2_RST                | O     | MFP7                        | Smart Card 2 reset pin.                    |
|         | BPWM1_CH3              | I/O   | MFP11                       | BPWM1 channel 3 output/capture input.      |
|         | QEI1_A                 | I     | MFP12                       | Quadrature encoder 1 phase A input         |
|         | USB_D-                 | A     | MFP14                       | USB differential signal D-.                |
| 87      | PA.14                  | I/O   | MFP0                        | General purpose digital I/O pin.           |
|         | I <sup>2</sup> S0_DI   | I     | MFP2                        | I <sup>2</sup> S0 data input pin.          |
|         | UART0_TXD              | O     | MFP3                        | UART0 data transmitter output pin.         |
|         | SPI2_MISO              | I/O   | MFP5                        | SPI2 MISO (Master In, Slave Out) pin.      |
|         | I <sup>2</sup> C2_SCL  | I/O   | MFP6                        | I <sup>2</sup> C2 clock pin.               |
|         | SC2_DAT                | I/O   | MFP7                        | Smart Card 2 data pin.                     |
|         | BPWM1_CH4              | I/O   | MFP11                       | BPWM1 channel 4 output/capture input.      |
|         | QEI1_B                 | I     | MFP12                       | Quadrature encoder 1 phase B input         |
| USB_D+  | A                      | MFP14 | USB differential signal D+. |  |
| 88      | PA.15                  | I/O   | MFP0                        | General purpose digital I/O pin.           |
|         | I <sup>2</sup> S0_DO   | O     | MFP2                        | I <sup>2</sup> S0 data output pin.         |
|         | UART0_RXD              | I     | MFP3                        | UART0 data receiver input pin.             |
|         | SPI2_MOSI              | I/O   | MFP5                        | SPI2 MOSI (Master Out, Slave In) pin.      |
|         | I <sup>2</sup> C2_SDA  | I/O   | MFP6                        | I <sup>2</sup> C2 data input/output pin.   |
|         | SC2_CLK                | O     | MFP7                        | Smart Card 2 clock pin.                    |
|         | BPWM1_CH5              | I/O   | MFP11                       | BPWM1 channel 5 output/capture input.      |

| 128 Pin   | Pin Name                    | Type  | MFP                                   | Description  |
|-----------|-----------------------------|-------|---------------------------------------|--|
|           | EPWM0_SYNC_IN               | I     | MFP12                                 | EPWM0 counter synchronous trigger input pin.   |
|           | USB_OTG_ID                  | I     | MFP14                                 | USB_ identification.   |
| 89        | HSUSB_VRES                  | A     | MFP0                                  | HSUSB module reference resistor  |
| 90        | HSUSB_V <sub>DD33</sub>     | P     | MFP0                                  | Power supply for HSUSB V <sub>DD33</sub>   |
| 91        | HSUSB_VBUS                  | P     | MFP0                                  | HSUSB Power supply from USB host or HUB.   |
| 92        | HSUSB_D-                    | A     | MFP0                                  | HSUSB differential signal D-.  |
| 93        | HSUSB_VSS                   | P     | MFP0                                  | Ground pin for HSUSB.  |
| 94        | HSUSB_D+                    | A     | MFP0                                  | HSUSB differential signal D+.  |
| 95        | HSUSB_V <sub>DD12_CAP</sub> | A     | MFP0                                  | HSUSB Internal power regulator output 1.2V decoupling pin.<br>Note: This pin needs to be connected with a 1uF capacitor. |
| 96        | HSUSB_ID                    | I     | MFP0                                  | HSUSB identification.  |
| 97        | NC                          | -     | -                                     | No connection.   |
| 98        | NC                          | -     | -                                     | No connection.   |
| 99        | PE.5                        | I/O   | MFP0                                  | General purpose digital I/O pin.   |
|           | EBI_nRD                     | O     | MFP2                                  | EBI read enable output pin.  |
|           | SD0_DAT3                    | I/O   | MFP3                                  | SD/SDIO0 data line bit 3.  |
|           | SPIM_SS                     | I/O   | MFP4                                  | SPIM slave select pin.   |
|           | SPI3_SS                     | I/O   | MFP5                                  | SPI3 slave select pin.   |
|           | SC0_PWR                     | O     | MFP6                                  | Smart Card 0 power pin.  |
|           | USCI0_CTL1                  | I/O   | MFP7                                  | USCI0 control 1 pin.   |
|           | QE11_B                      | I     | MFP11                                 | Quadrature encoder 1 phase B input   |
|           | EPWM0_CH2                   | I/O   | MFP12                                 | EPWM0 channel 2 output/capture input.  |
| BPWM0_CH3 | I/O                         | MFP13 | BPWM0 channel 3 output/capture input. |  |
| 100       | NC                          | -     | -                                     | No connection.   |
| 101       | PE.3                        | I/O   | MFP0                                  | General purpose digital I/O pin.   |
|           | EBI_MCLK                    | O     | MFP2                                  | EBI external clock output pin.   |
|           | SD0_DAT1                    | I/O   | MFP3                                  | SD/SDIO0 data line bit 1.  |
|           | SPIM_MISO                   | I/O   | MFP4                                  | SPIM MISO (Master In, Slave Out) pin.  |
|           | SPI3_MISO                   | I/O   | MFP5                                  | SPI3 MISO (Master In, Slave Out) pin.  |
|           | SC0_DAT                     | I/O   | MFP6                                  | Smart Card 0 data pin.   |
|           | USCI0_DAT0                  | I/O   | MFP7                                  | USCI0 data 0 pin.  |
|           | QE10_A                      | I     | MFP11                                 | Quadrature encoder 0 phase A input   |
|           | EPWM0_CH4                   | I/O   | MFP12                                 | EPWM0 channel 4 output/capture input.  |
| BPWM0_CH1 | I/O                         | MFP13 | BPWM0 channel 1 output/capture input. |  |

| 128 Pin | Pin Name                | Type | MFP   | Description   |
|---------|-------------------------|------|-------|---|
| 102     | NC                      | -    | -     | No connection.  |
| 103     | V <sub>SS</sub>         | P    | MFP0  | Ground pin for digital circuit.   |
| 104     | V <sub>DD</sub>         | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 105     | PE.1                    | I/O  | MFP0  | General purpose digital I/O pin.  |
|         | EBI_AD10                | I/O  | MFP2  | EBI address/data bus bit 10.  |
|         | QSPI0_MISO0             | I/O  | MFP3  | QSPI0 MISO0 (Master In, Slave Out) pin.   |
|         | SC2_DAT                 | I/O  | MFP4  | Smart Card 2 data pin.  |
|         | I <sup>2</sup> S0_BCLK  | O    | MFP5  | I <sup>2</sup> S0 bit clock output pin.   |
|         | SPI1_MISO               | I/O  | MFP6  | SPI1 MISO (Master In, Slave Out) pin.   |
|         | UART3_TXD               | O    | MFP7  | UART3 data transmitter output pin.  |
|         | I <sup>2</sup> C1_SCL   | I/O  | MFP8  | I <sup>2</sup> C1 clock pin.  |
|         | UART4_nCTS              | I    | MFP9  | UART4 clear to Send input pin.  |
| 106     | PE.0                    | I/O  | MFP0  | General purpose digital I/O pin.  |
|         | EBI_AD11                | I/O  | MFP2  | EBI address/data bus bit 11.  |
|         | QSPI0_MOSI0             | I/O  | MFP3  | QSPI0 MOSI0 (Master Out, Slave In) pin.   |
|         | SC2_CLK                 | O    | MFP4  | Smart Card 2 clock pin.   |
|         | I <sup>2</sup> S0_MCLK  | O    | MFP5  | I <sup>2</sup> S0 master clock output pin.                                      |
|         | SPI1_MOSI               | I/O  | MFP6  | SPI1 MOSI (Master Out, Slave In) pin.   |
|         | UART3_RXD               | I    | MFP7  | UART3 data receiver input pin.  |
|         | I <sup>2</sup> C1_SDA   | I/O  | MFP8  | I <sup>2</sup> C1 data input/output pin.  |
|         | UART4_nRTS              | O    | MFP9  | UART4 request to Send output pin.   |
| 107     | PH.8                    | I/O  | MFP0  | General purpose digital I/O pin.  |
|         | EBI_AD12                | I/O  | MFP2  | EBI address/data bus bit 12.  |
|         | QSPI0_CLK               | I/O  | MFP3  | QSPI0 serial clock pin.   |
|         | SC2_PWR                 | O    | MFP4  | Smart Card 2 power pin.   |
|         | I <sup>2</sup> S0_DI    | I    | MFP5  | I <sup>2</sup> S0 data input pin.   |
|         | SPI1_CLK                | I/O  | MFP6  | SPI1 serial clock pin.  |
|         | UART3_nRTS              | O    | MFP7  | UART3 request to Send output pin.   |
|         | I <sup>2</sup> C1_SMBAL | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBALTER pin  |
|         | I <sup>2</sup> C2_SCL   | I/O  | MFP9  | I <sup>2</sup> C2 clock pin.  |
|         | UART1_TXD               | O    | MFP10 | UART1 data transmitter output pin.  |
| 108     | PH.9                    | I/O  | MFP0  | General purpose digital I/O pin.  |
|         | EBI_AD13                | I/O  | MFP2  | EBI address/data bus bit 13.  |

| 128 Pin | Pin Name                 | Type | MFP   | Description  |
|---------|--------------------------|------|-------|--|
|         | QSPI0_SS                 | I/O  | MFP3  | QSPI0 slave select pin.  |
|         | SC2_RST                  | O    | MFP4  | Smart Card 2 reset pin.  |
|         | I <sup>2</sup> S0_DO     | O    | MFP5  | I <sup>2</sup> S0 data output pin.   |
|         | SPI1_SS                  | I/O  | MFP6  | SPI1 slave select pin.   |
|         | UART3_nCTS               | I    | MFP7  | UART3 clear to Send input pin.   |
|         | I <sup>2</sup> C1_SMBSUS | O    | MFP8  | I <sup>2</sup> C1 SMBus SMBSUS pin (PMBus CONTROL pin)                                     |
|         | I <sup>2</sup> C2_SDA    | I/O  | MFP9  | I <sup>2</sup> C2 data input/output pin.   |
|         | UART1_RXD                | I    | MFP10 | UART1 data receiver input pin.   |
| 109     | PH.10                    | I/O  | MFP0  | General purpose digital I/O pin.   |
|         | EBI_AD14                 | I/O  | MFP2  | EBI address/data bus bit 14.   |
|         | QSPI0_MISO1              | I/O  | MFP3  | QSPI0 MISO1 (Master In, Slave Out) pin.  |
|         | SC2_nCD                  | I    | MFP4  | Smart Card 2 card detect pin.  |
|         | I <sup>2</sup> S0_LRCK   | O    | MFP5  | I <sup>2</sup> S0 left right channel clock output pin.                                     |
|         | SPI1_I2SMCLK             | I/O  | MFP6  | SPI1 I <sup>2</sup> S master clock output pin  |
|         | UART4_TXD                | O    | MFP7  | UART4 data transmitter output pin.   |
|         | UART0_TXD                | O    | MFP8  | UART0 data transmitter output pin.   |
| 110     | PH.11                    | I/O  | MFP0  | General purpose digital I/O pin.   |
|         | EBI_AD15                 | I/O  | MFP2  | EBI address/data bus bit 15.   |
|         | QSPI0_MOSI1              | I/O  | MFP3  | QSPI0 MOSI1 (Master Out, Slave In) pin.  |
|         | UART4_RXD                | I    | MFP7  | UART4 data receiver input pin.   |
|         | UART0_RXD                | I    | MFP8  | UART0 data receiver input pin.   |
|         | EPWM0_CH5                | I/O  | MFP11 | EPWM0 channel 5 output/capture input.  |
| 111     | PD.14                    | I/O  | MFP0  | General purpose digital I/O pin.   |
|         | EBI_nCS0                 | O    | MFP2  | EBI chip select 0 output pin.  |
|         | SPI3_I2SMCLK             | I/O  | MFP3  | SPI3 I <sup>2</sup> S master clock output pin  |
|         | SC1_nCD                  | I    | MFP4  | Smart Card 1 card detect pin.  |
|         | EPWM0_CH4                | I/O  | MFP11 | EPWM0 channel 4 output/capture input.  |
| 112     | V <sub>SS</sub>          | P    | MFP0  | Ground pin for digital circuit.  |
| 113     | LDO_CAP                  | A    | MFP0  | LDO output pin.<br><b>Note:</b> This pin needs to be connected with an external capacitor. |
| 114     | V <sub>DD</sub>          | P    | MFP0  | Power supply for I/O ports and LDO source for internal PLL and digital circuit.            |
| 115     | PC.14                    | I/O  | MFP0  | General purpose digital I/O pin.   |
|         | EBI_AD11                 | I/O  | MFP2  | EBI address/data bus bit 11.   |

| 128 Pin | Pin Name                 | Type | MFP   | Description  |
|---------|--------------------------|------|-------|--|
|         | SC1_nCD                  | I    | MFP3  | Smart Card 1 card detect pin.                          |
|         | SPI0_I2SMCLK             | I/O  | MFP4  | SPI0 I <sup>2</sup> S master clock output pin          |
|         | USCI0_CTL0               | I/O  | MFP5  | USCI0 control 0 pin.                                   |
|         | QSPI0_CLK                | I/O  | MFP6  | QSPI0 serial clock pin.                                |
|         | EPWM0_SYNC_IN            | I    | MFP11 | EPWM0 counter synchronous trigger input pin.           |
|         | ETM_TRACE_CLK            | I    | MFP12 | ETM receiver Trace Clock input pin                     |
|         | TM1                      | I/O  | MFP13 | Timer1 event counter input/toggle output pin.          |
|         | USB_VBUS_ST              | I    | MFP14 | USB external VBUS regulator status pin.                |
|         | HSUSB_VBUS_ST            | I    | MFP15 | HSUSB external VBUS regulator status pin.              |
| 116     | PB.15                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|         | EADC0_CH15               | A    | MFP1  | EADC0 channel 15 analog input.                         |
|         | EBI_AD12                 | I/O  | MFP2  | EBI address/data bus bit 12.                           |
|         | SC1_PWR                  | O    | MFP3  | Smart Card 1 power pin.                                |
|         | SPI0_SS                  | I/O  | MFP4  | SPI0 slave select pin.                                 |
|         | USCI0_CTL1               | I/O  | MFP5  | USCI0 control 1 pin.                                   |
|         | UART0_nCTS               | I    | MFP6  | UART0 clear to Send input pin.                         |
|         | UART3_TXD                | O    | MFP7  | UART3 data transmitter output pin.                     |
|         | I <sup>2</sup> C2_SMBAL  | O    | MFP8  | I <sup>2</sup> C2 SMBus SMBALTER pin                   |
|         | EPWM1_CH0                | I/O  | MFP11 | EPWM1 channel 0 output/capture input.                  |
|         | ETM_TRACE_DATA0          | I    | MFP12 | ETM receiver Trace Data 0 input pin                    |
|         | TM0_EXT                  | I/O  | MFP13 | Timer0 event counter input/toggle output pin.          |
|         | USB_VBUS_EN              | O    | MFP14 | USB external VBUS regulator enable pin.                |
|         | HSUSB_VBUS_EN            | O    | MFP15 | HSUSB external VBUS regulator enable pin.              |
| 117     | PB.14                    | I/O  | MFP0  | General purpose digital I/O pin.                       |
|         | EADC0_CH14               | A    | MFP1  | EADC0 channel 14 analog input.                         |
|         | EBI_AD13                 | I/O  | MFP2  | EBI address/data bus bit 13.                           |
|         | SC1_RST                  | O    | MFP3  | Smart Card 1 reset pin.                                |
|         | SPI0_CLK                 | I/O  | MFP4  | SPI0 serial clock pin.                                 |
|         | USCI0_DAT1               | I/O  | MFP5  | USCI0 data 1 pin.                                      |
|         | UART0_nRTS               | O    | MFP6  | UART0 request to Send output pin.                      |
|         | UART3_RXD                | I    | MFP7  | UART3 data receiver input pin.                         |
|         | I <sup>2</sup> C2_SMBSUS | O    | MFP8  | I <sup>2</sup> C2 SMBus SMBSUS pin (PMBus CONTROL pin) |
|         | EPWM1_CH1                | I/O  | MFP11 | EPWM1 channel 1 output/capture input.                  |
|         | ETM_TRACE_DATA1          | I    | MFP12 | ETM receiver Trace Data 1 input pin                    |

| 128 Pin         | Pin Name              | Type  | MFP   | Description                                   |
|-----------------|-----------------------|-------|---|---|
|                 | TM1_EXT               | I/O   | MFP13   | Timer1 event counter input/toggle output pin. |
|                 | CLKO                  | O     | MFP14   | Clock Out                                     |
| 118             | PB.13                 | I/O   | MFP0  | General purpose digital I/O pin.              |
|                 | EADC0_CH13            | A     | MFP1  | EADC0 channel 13 analog input.                |
|                 | DAC1_OUT              | A     | MFP1  | DAC1 channel analog output.                   |
|                 | ACMP0_P3              | A     | MFP1  | Analog comparator 0 positive input 3 pin.     |
|                 | ACMP1_P3              | A     | MFP1  | Analog comparator 1 positive input 3 pin.     |
|                 | EBI_AD14              | I/O   | MFP2  | EBI address/data bus bit 14.                  |
|                 | SC1_DAT               | I/O   | MFP3  | Smart Card 1 data pin.                        |
|                 | SPI0_MISO             | I/O   | MFP4  | SPI0 MISO (Master In, Slave Out) pin.         |
|                 | USCI0_DAT0            | I/O   | MFP5  | USCI0 data 0 pin.                             |
|                 | UART0_TXD             | O     | MFP6  | UART0 data transmitter output pin.            |
|                 | UART3_nRTS            | O     | MFP7  | UART3 request to Send output pin.             |
|                 | I <sup>2</sup> C2_SCL | I/O   | MFP8  | I <sup>2</sup> C2 clock pin.                  |
|                 | EPWM1_CH2             | I/O   | MFP11   | EPWM1 channel 2 output/capture input.         |
|                 | ETM_TRACE_DATA2       | I     | MFP12   | ETM receiver Trace Data 2 input pin           |
| TM2_EXT         | I/O                   | MFP13 | Timer2 event counter input/toggle output pin. |   |
| 119             | PB.12                 | I/O   | MFP0  | General purpose digital I/O pin.              |
|                 | EADC0_CH12            | A     | MFP1  | EADC0 channel 12 analog input.                |
|                 | DAC0_OUT              | A     | MFP1  | DAC0 channel analog output.                   |
|                 | ACMP0_P2              | A     | MFP1  | Analog comparator 0 positive input 2 pin.     |
|                 | ACMP1_P2              | A     | MFP1  | Analog comparator 1 positive input 2 pin.     |
|                 | EBI_AD15              | I/O   | MFP2  | EBI address/data bus bit 15.                  |
|                 | SC1_CLK               | O     | MFP3  | Smart Card 1 clock pin.                       |
|                 | SPI0_MOSI             | I/O   | MFP4  | SPI0 MOSI (Master Out, Slave In) pin.         |
|                 | USCI0_CLK             | I/O   | MFP5  | USCI0 clock pin.                              |
|                 | UART0_RXD             | I     | MFP6  | UART0 data receiver input pin.                |
|                 | UART3_nCTS            | I     | MFP7  | UART3 clear to Send input pin.                |
|                 | I <sup>2</sup> C2_SDA | I/O   | MFP8  | I <sup>2</sup> C2 data input/output pin.      |
|                 | SD0_nCD               | I     | MFP9  | SD/SDIO0 card detect input pin                |
|                 | EPWM1_CH3             | I/O   | MFP11   | EPWM1 channel 3 output/capture input.         |
| ETM_TRACE_DATA3 | I                     | MFP12 | ETM receiver Trace Data 3 input pin           |   |
| TM3_EXT         | I/O                   | MFP13 | Timer3 event counter input/toggle output pin. |   |
| 120             | AV <sub>DD</sub>      | P     | MFP0  | Power supply for internal analog circuit.     |

| 128 Pin       | Pin Name              | Type  | MFP                                       | Description  |
|---------------|-----------------------|-------|---|--|
| 121           | V <sub>REF</sub>      | A     | MFP0                                      | ADC reference voltage input.<br>Note: This pin needs to be connected with a 1uF capacitor. |
| 122           | AV <sub>SS</sub>      | P     | MFP0                                      | Ground pin for analog circuit.   |
| 123           | PB.11                 | I/O   | MFP0                                      | General purpose digital I/O pin.   |
|               | EADC0_CH11            | A     | MFP1                                      | EADC0 channel 11 analog input.   |
|               | EBI_ADR16             | O     | MFP2                                      | EBI address bus bit 16.  |
|               | EMAC_RMII_MDC         | O     | MFP3                                      | EMAC RMII PHY Management Clock output pin.   |
|               | UART0_nCTS            | I     | MFP5                                      | UART0 clear to Send input pin.   |
|               | UART4_TXD             | O     | MFP6                                      | UART4 data transmitter output pin.   |
|               | I <sup>2</sup> C1_SCL | I/O   | MFP7                                      | I <sup>2</sup> C1 clock pin.   |
|               | CAN0_TXD              | O     | MFP8                                      | CAN0 bus transmitter output.   |
|               | SPI0_I2SMCLK          | I/O   | MFP9                                      | SPI0 I <sup>2</sup> S master clock output pin  |
|               | BPWM1_CH0             | I/O   | MFP10                                     | BPWM1 channel 0 output/capture input.  |
|               | SPI3_CLK              | I/O   | MFP11                                     | SPI3 serial clock pin.   |
| HSUSB_VBUS_ST | I                     | MFP14 | HSUSB external VBUS regulator status pin. |  |
| 124           | PB.10                 | I/O   | MFP0                                      | General purpose digital I/O pin.   |
|               | EADC0_CH10            | A     | MFP1                                      | EADC0 channel 10 analog input.   |
|               | EBI_ADR17             | O     | MFP2                                      | EBI address bus bit 17.  |
|               | EMAC_RMII_MDIO        | I/O   | MFP3                                      | EMAC RMII PHY Management Data pin.   |
|               | USCI1_CTL0            | I/O   | MFP4                                      | USCI1 control 0 pin.   |
|               | UART0_nRTS            | O     | MFP5                                      | UART0 request to Send output pin.  |
|               | UART4_RXD             | I     | MFP6                                      | UART4 data receiver input pin.   |
|               | I <sup>2</sup> C1_SDA | I/O   | MFP7                                      | I <sup>2</sup> C1 data input/output pin.   |
|               | CAN0_RXD              | I     | MFP8                                      | CAN0 bus receiver input.   |
|               | BPWM1_CH1             | I/O   | MFP10                                     | BPWM1 channel 1 output/capture input.  |
|               | SPI3_SS               | I/O   | MFP11                                     | SPI3 slave select pin.   |
| HSUSB_VBUS_EN | O                     | MFP14 | HSUSB external VBUS regulator enable pin. |  |
| 125           | PB.9                  | I/O   | MFP0                                      | General purpose digital I/O pin.   |
|               | EADC0_CH9             | A     | MFP1                                      | EADC0 channel 9 analog input.  |
|               | EBI_ADR18             | O     | MFP2                                      | EBI address bus bit 18.  |
|               | EMAC_RMII_TXD0        | O     | MFP3                                      | EMAC RMII Transmit Data bus bit 0.   |
|               | USCI1_CTL1            | I/O   | MFP4                                      | USCI1 control 1 pin.   |
|               | UART0_TXD             | O     | MFP5                                      | UART0 data transmitter output pin.   |
|               | UART1_nCTS            | I     | MFP6                                      | UART1 clear to Send input pin.   |



| 128 Pin | Pin Name                | Type | MFP   | Description   |
|---------|-------------------------|------|-------|---|
|         | I <sup>2</sup> C1_SMBAL | O    | MFP7  | I <sup>2</sup> C1 SMBus SMBALTER pin                  |
|         | BPWM1_CH2               | I/O  | MFP10 | BPWM1 channel 2 output/capture input.                 |
|         | SPI3_MISO               | I/O  | MFP11 | SPI3 MISO (Master In, Slave Out) pin.                 |
|         | INT7                    | I    | MFP13 | External interrupt 7 input pin.                       |
| 126     | PB.8                    | I/O  | MFP0  | General purpose digital I/O pin.                      |
|         | EADC0_CH8               | A    | MFP1  | EADC0 channel 8 analog input.                         |
|         | EBI_ADR19               | O    | MFP2  | EBI address bus bit 19.                               |
|         | EMAC_RMII_TXD1          | O    | MFP3  | EMAC RMII Transmit Data bus bit 1.                    |
|         | USCI1_CLK               | I/O  | MFP4  | USCI1 clock pin.                                      |
|         | UART0_RXD               | I    | MFP5  | UART0 data receiver input pin.                        |
|         | UART1_nRTS              | O    | MFP6  | UART1 request to Send output pin.                     |
|         | I <sup>2</sup> C1_SMBUS | O    | MFP7  | I <sup>2</sup> C1 SMBus SMBUS pin (PMBus CONTROL pin) |
|         | BPWM1_CH3               | I/O  | MFP10 | BPWM1 channel 3 output/capture input.                 |
|         | SPI3_MOSI               | I/O  | MFP11 | SPI3 MOSI (Master Out, Slave In) pin.                 |
|         | INT6                    | I    | MFP13 | External interrupt 6 input pin.                       |
| 127     | PB.7                    | I/O  | MFP0  | General purpose digital I/O pin.                      |
|         | EADC0_CH7               | A    | MFP1  | EADC0 channel 7 analog input.                         |
|         | EBI_nWRL                | O    | MFP2  | EBI low byte write enable output pin.                 |
|         | EMAC_RMII_TXEN          | O    | MFP3  | EMAC RMII Transmit Enable output pin.                 |
|         | USCI1_DAT0              | I/O  | MFP4  | USCI1 data 0 pin.                                     |
|         | CAN1_TXD                | O    | MFP5  | CAN1 bus transmitter output.                          |
|         | UART1_TXD               | O    | MFP6  | UART1 data transmitter output pin.                    |
|         | SD1_CMD                 | I/O  | MFP7  | SD/SDIO1 command/response pin                         |
|         | EBI_nCS0                | O    | MFP8  | EBI chip select 0 output pin.                         |
|         | BPWM1_CH4               | I/O  | MFP10 | BPWM1 channel 4 output/capture input.                 |
|         | EPWM1_BRAKE0            | I    | MFP11 | EPWM1 Brake 0 input pin.                              |
|         | EPWM1_CH4               | I/O  | MFP12 | EPWM1 channel 4 output/capture input.                 |
|         | INT5                    | I    | MFP13 | External interrupt 5 input pin.                       |
|         | USB_VBUS_ST             | I    | MFP14 | USB external VBUS regulator status pin.               |
|         | ACMP0_O                 | O    | MFP15 | Analog comparator 0 output pin.                       |
| 128     | PB.6                    | I/O  | MFP0  | General purpose digital I/O pin.                      |
|         | EADC0_CH6               | A    | MFP1  | EADC0 channel 6 analog input.                         |
|         | EBI_nWRH                | O    | MFP2  | EBI high byte write enable output pin                 |
|         | EMAC_PPS                | O    | MFP3  | EMAC Pulse Per Second output pin.                     |

| 128 Pin | Pin Name     | Type | MFP   | Description                             |
|---------|--------------|------|-------|---|
|         | USCI1_DAT1   | I/O  | MFP4  | USCI1 data 1 pin.                       |
|         | CAN1_RXD     | I    | MFP5  | CAN1 bus receiver input.                |
|         | UART1_RXD    | I    | MFP6  | UART1 data receiver input pin.          |
|         | SD1_CLK      | O    | MFP7  | SD/SDIO1 clock output pin               |
|         | EBI_nCS1     | O    | MFP8  | EBI chip select 1 output pin.           |
|         | BPWM1_CH5    | I/O  | MFP10 | BPWM1 channel 5 output/capture input.   |
|         | EPWM1_BRAKE1 | I    | MFP11 | EPWM1 Brake 1 input pin.                |
|         | EPWM1_CH5    | I/O  | MFP12 | EPWM1 channel 5 output/capture input.   |
|         | INT4         | I    | MFP13 | External interrupt 4 input pin.         |
|         | USB_VBUS_EN  | O    | MFP14 | USB external VBUS regulator enable pin. |
|         | ACMP1_O      | O    | MFP15 | Analog comparator 1 output pin.         |

5 BLOCK DIAGRAM

5.1 M480 Block Diagram

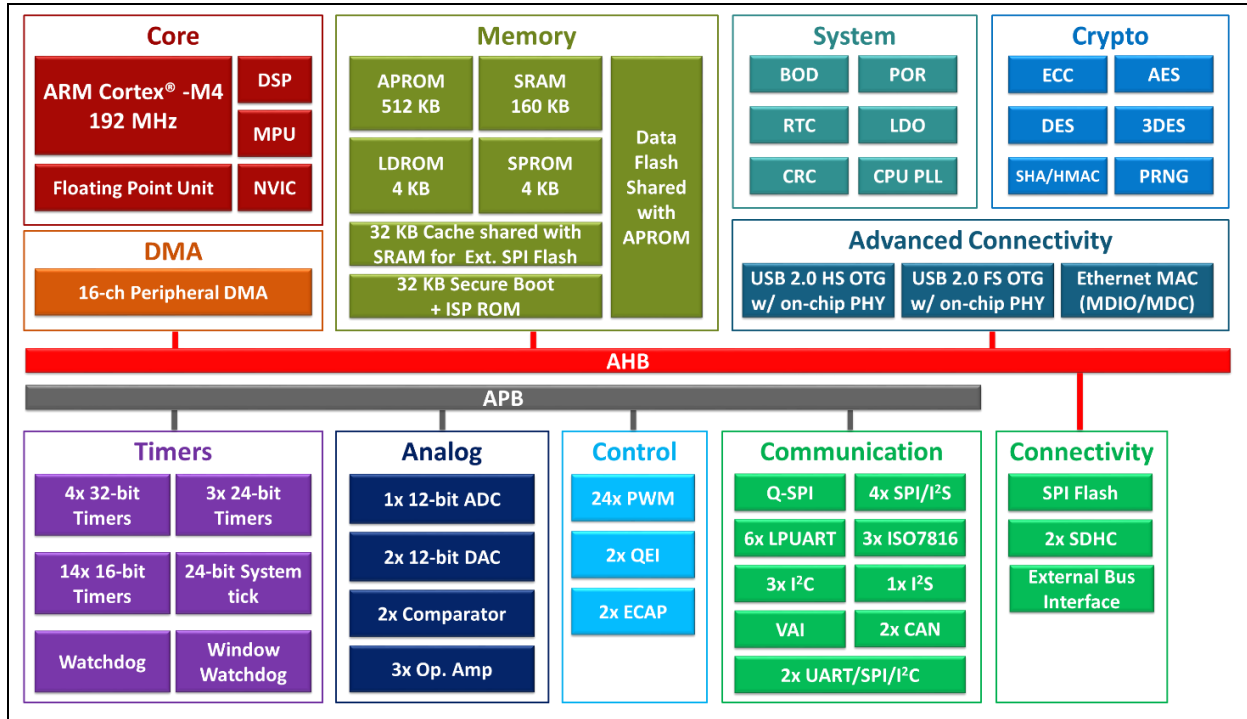


Figure 5-1 NuMicro® M480 Block Diagram (M48xID)

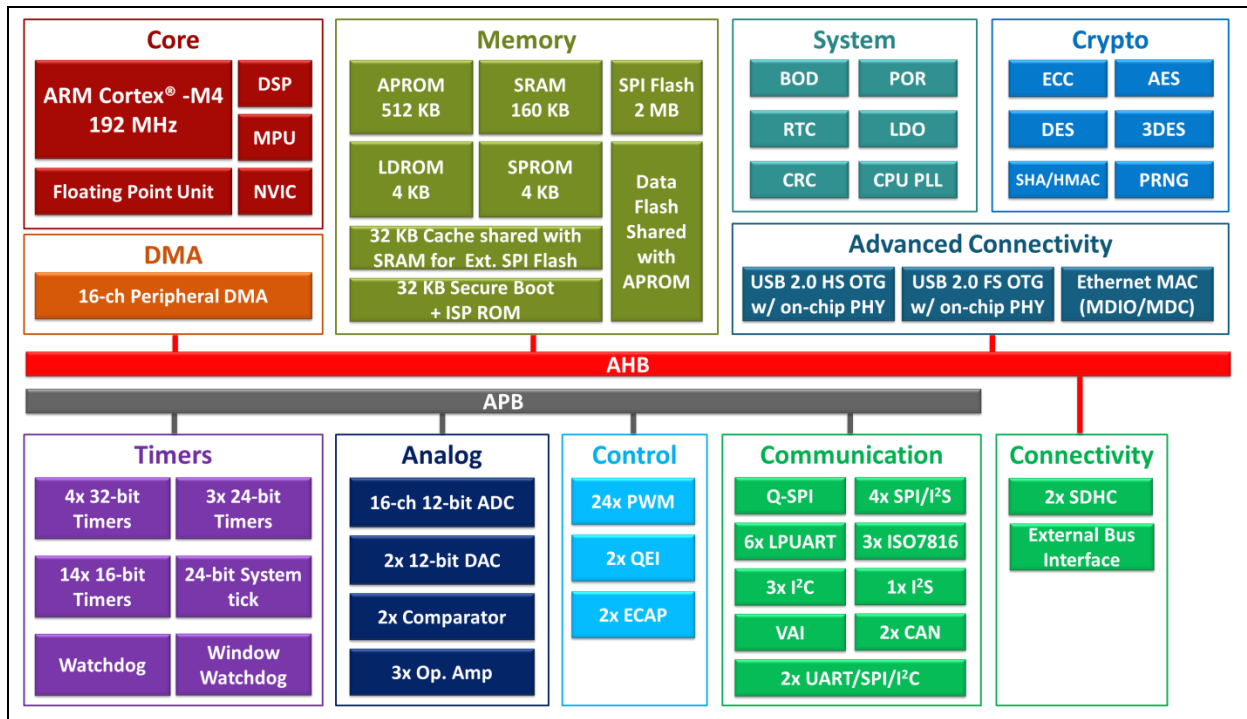


Figure 5-2 NuMicro® M480 Block Diagram (M487KMCAN)

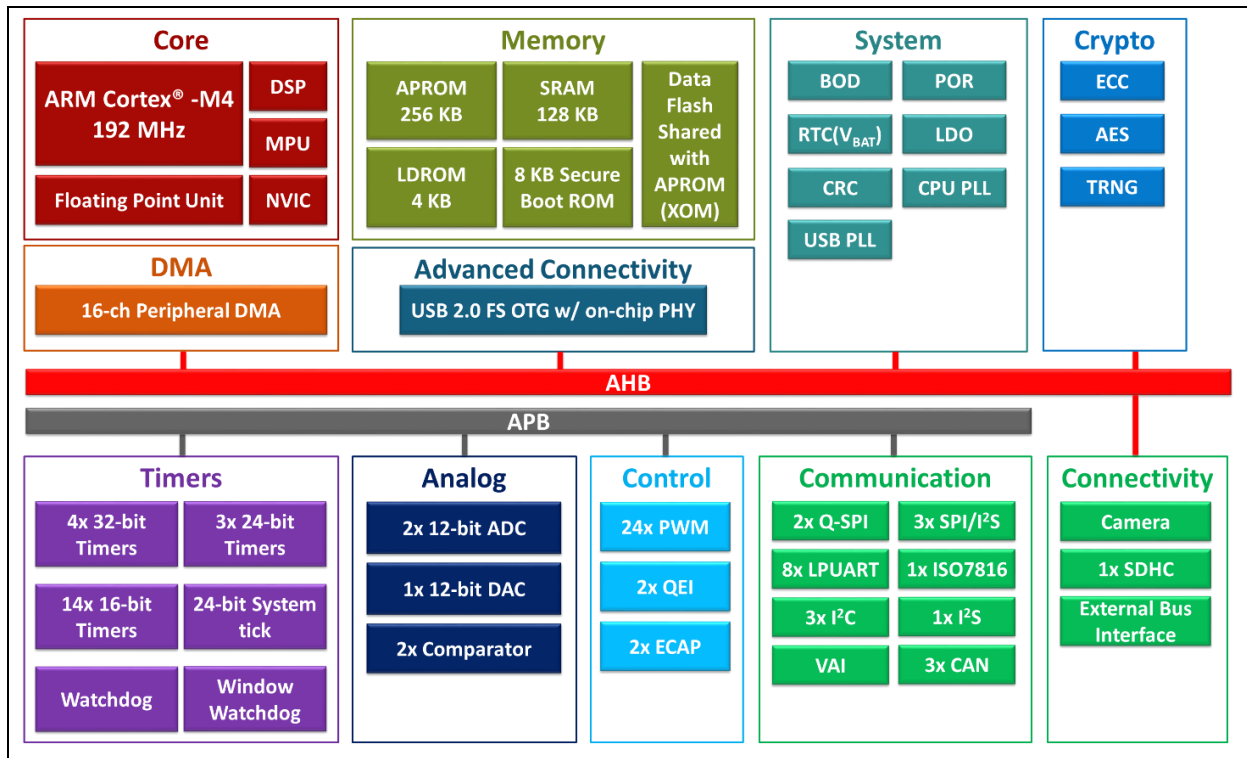


Figure 5-3 NuMicro® M480 Block Diagram (M48xGC)

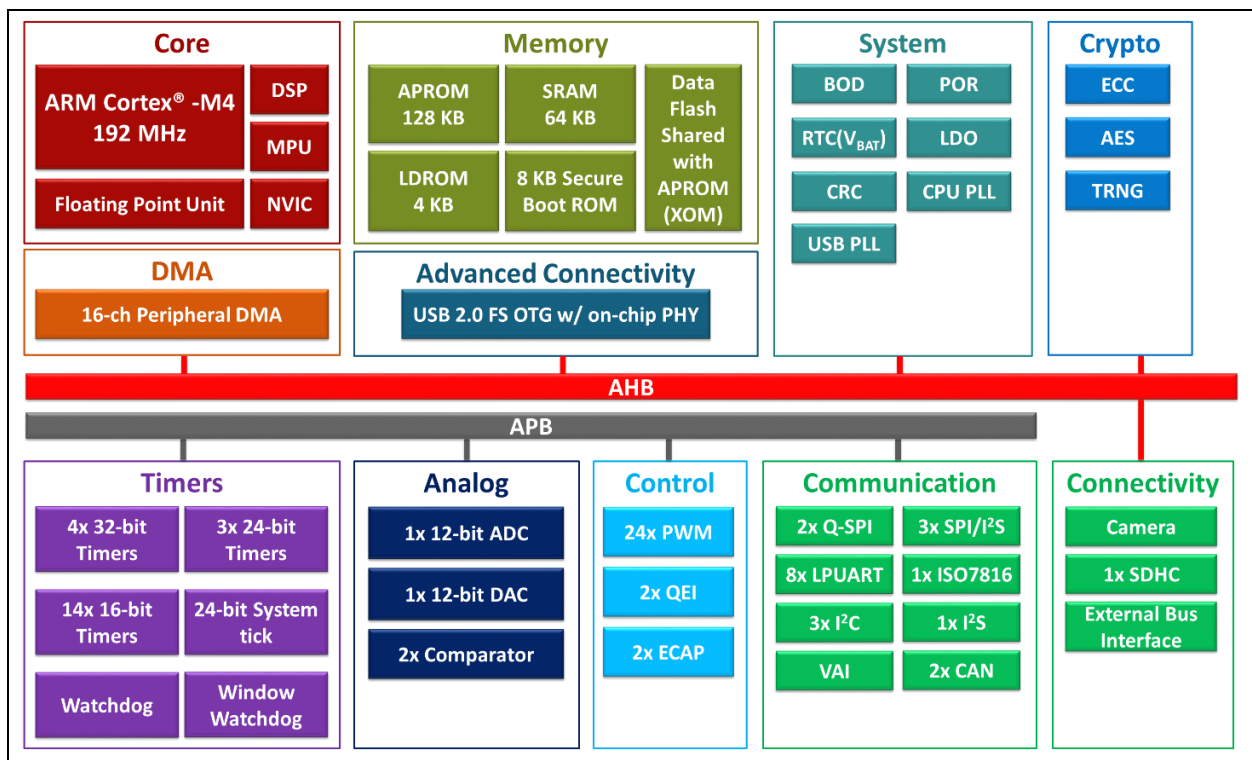


Figure 5-4 NuMicro® M480 Block Diagram (M48xE8)

## 6 FUNCTIONAL DESCRIPTION

### 6.1 Arm® Cortex®-M4F Core

The Cortex®-M4 processor, a configurable, multistage, 32-bit RISC processor, has three AMBA AHB-Lite interfaces for best parallel performance and includes an NVIC component. The processor with optional hardware debug functionality can execute Thumb code and is compatible with other Cortex®-M profile processors. The profile supports two modes - Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The Cortex®-M4F is a processor with the same capability as the Cortex®-M4 processor and includes floating point arithmetic functionality. The NuMicro® M480 series is embedded with Cortex®-M4F processor. Throughout this document, the name Cortex®-M4 refers to both Cortex®-M4 and Cortex®-M4F processors. Figure 6-1 shows the functional controller of the processor.

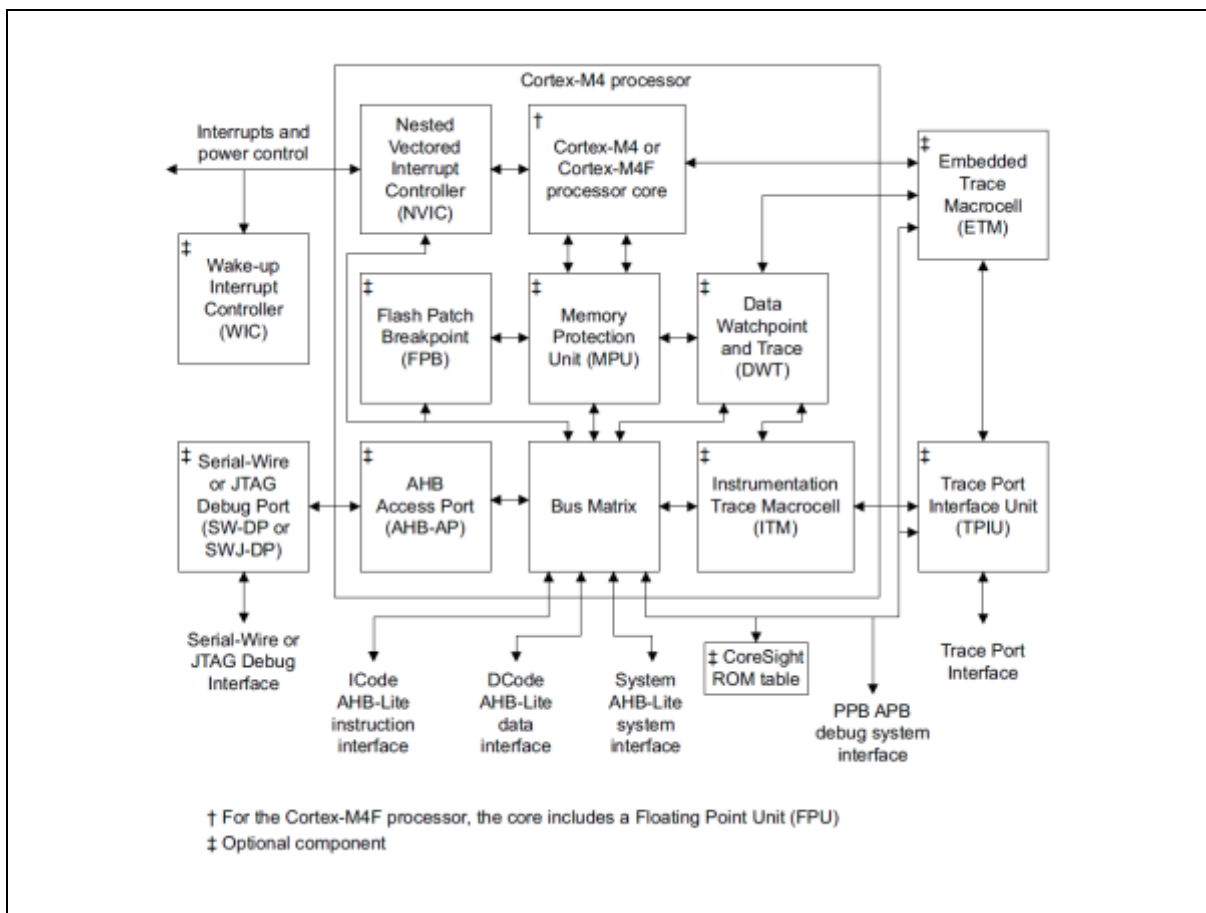


Figure 6-1 Cortex®-M4F Block Diagram

**Cortex®-M4F processor features:**

- A low gate count processor core, with low latency interrupt processing that has:
  - A subset of the Thumb instruction set, defined in the *Armv7-M Architecture Reference Manual*
  - Banked Stack Pointer (SP)
  - Hardware integer divide instructions, SDIV and UDIV
  - Handler and Thread modes
  - Thumb and Debug states
  - Support for interruptible-continued instructions LDM, STM, PUSH, and POP for low interrupt latency
  - Automatic processor state saving and restoration for low latency *Interrupt Service Routine (ISR)* entry and exit
  - Support for Armv6 big-endian byte-invariant or little-endian accesses
  - Support for Armv6 unaligned accesses
- Floating Point Unit (FPU) in the Cortex®-M4F processor providing:
  - 32-bit instructions for single-precision (C float) data-processing operations
  - Combined Multiply and Accumulate instructions for increased precision (Fused MAC)
  - Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
  - Hardware support for denormals and all IEEE rounding modes
  - 32 dedicated 32-bit single precision registers, also addressable as 16 double-word registers
  - Decoupled three stage pipeline
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  - External interrupts. Configurable from 1 to 240 (the NuMicro® M480 series configured with 64 interrupts)
  - Bits of priority, configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping which enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tri- chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
  - Processor state automatically saved on interrupt entry, and restored on interrupt exit with on instruction overhead
  - Support for Wake-up Interrupt Controller (WIC) with Ultra-low Power Sleep mode
- Memory Protection Unit (MPU). An optional MPU for memory protection, including:
  - Eight memory regions
  - Sub Region Disable (SRD), enabling efficient use of memory regions
  - The ability to enable a background region that implements the default memory map attributes

- Low-cost debug solution that features:
  - Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted.
  - Serial Wire Debug Port(SW-DP) or Serial Wire JTAG Debug Port (SWJ-DP) debug access
  - Optional Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
  - Optional Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
  - Optional Instrumentation Trace Macrocell (ITM) for support of printf() style debugging
  - Optional Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer (TPA), including Single Wire Output (SWO) mode
  - Optional Embedded Trace Macrocell (ETM) for instruction trace.
- Bus interfaces:
  - Three Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, Dcode, and System bus interfaces
  - Private Peripheral Bus (PPB) based on Advanced Peripheral Bus (APB) interface
  - Bit-band support that includes atomic bit-band write and read operations.
  - Memory access alignment
  - Write buffer for buffering of write data
  - Exclusive access transfers for multiprocessor systems

## 6.2 System Manager

### 6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Organization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

### 6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS\_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS\_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex<sup>®</sup>-M4 core only by writing 1 to CPURST (SYS\_IPRST0[1])



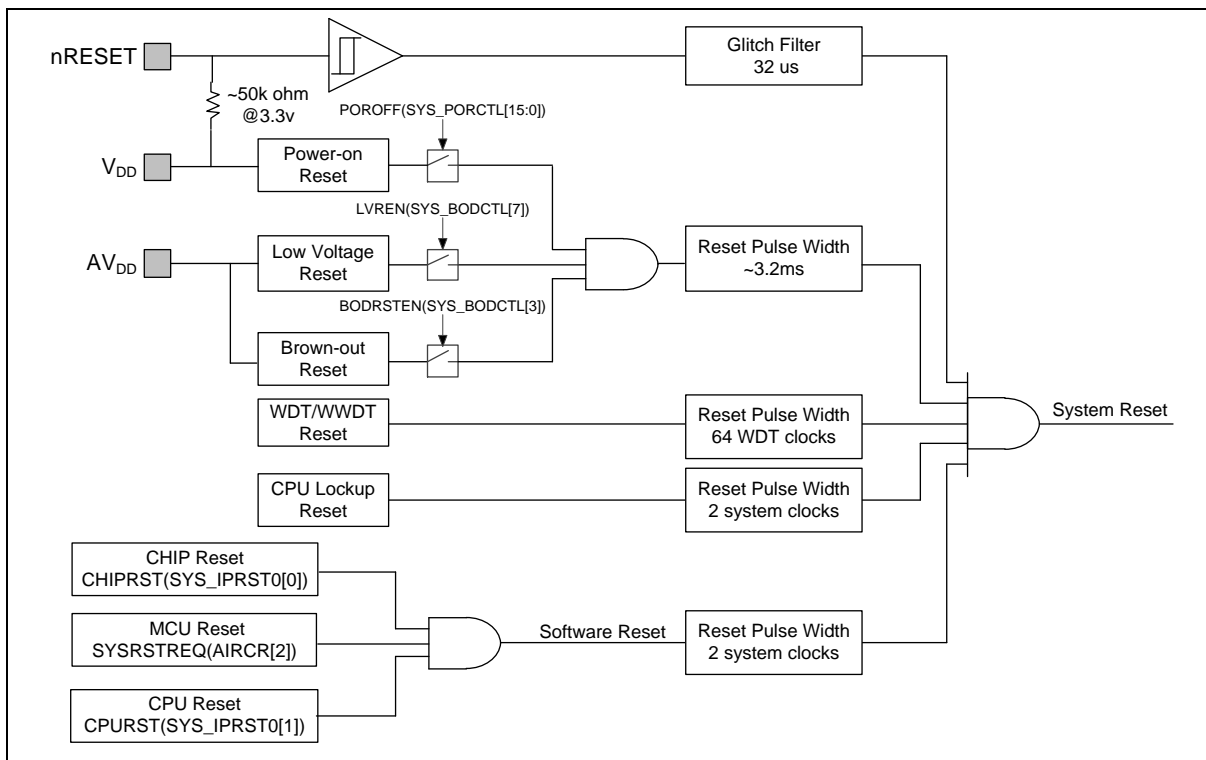


Figure 6-2 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M4 only; the other reset sources will reset Cortex®-M4 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

| Reset Sources Register   | POR                 | nRESET              | WDT                 | LVR                 | BOD                 | Lockup              | CHIP                | MCU                 | CPU       |
|--------------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|-----------|
| SYS_RSTSTS               | Bit 0 = 1           | Bit 1 = 1           | Bit 2 = 1           | Bit 3 = 1           | Bit 4 = 1           | Bit 8 = 1           | Bit 0 = 1           | Bit 5 = 1           | Bit 7 = 1 |
| CHIPRST (SYS_IPRST0[0])  | 0x0                 | -                   | -                   | -                   | -                   | -                   | -                   | -                   | -         |
| BODEN (SYS_BODCTL[0])    |                     |                     |                     |                     |                     |                     |                     |                     |           |
| BODVL (SYS_BODCTL[2:1])  | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | -                   | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | -         |
| BODRSTEN (SYS_BODCTL[3]) |                     |                     |                     |                     |                     |                     |                     |                     |           |
| HXTEN (CLK_PWRCTL[0])    | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 |           |
| LXTEN (CLK_PWRCTL[1])    | 0x0                 | -                   | -                   | -                   | -                   | -                   | -                   | -                   | -         |
| WDTCKEN (CLK_APBCLK0[0]) | 0x1                 | -                   | 0x1                 | -                   | -                   | -                   | 0x1                 | -                   | -         |
| HCLKSEL                  | Reload from         | Reload from         | Reload from         | Reload from         | Reload from         | Reload from         | Reload from         | Reload from         | -         |

| (CLK_CLKSEL0[2:0])  | CONFIG0                      | CONFIG0                      | CONFIG0                      | CONFIG0                      | CONFIG0                      | CONFIG0 | CONFIG0                      | CONFIG0 | CONFIG0 |
|---|------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|---------|------------------------------|---------|---------|
| WDTSEL<br>(CLK_CLKSEL1[1:0])  | 0x3                          | 0x3                          | -                            | -                            | -                            | -       | -                            | -       | -       |
| HXTSTB<br>(CLK_STATUS[0])   | 0x0                          | -                            | -                            | -                            | -                            | -       | -                            | -       | -       |
| LXTSTB<br>(CLK_STATUS[1])   | 0x0                          | -                            | -                            | -                            | -                            | -       | -                            | -       | -       |
| PLLSTB<br>(CLK_STATUS[2])   | 0x0                          | -                            | -                            | -                            | -                            | -       | -                            | -       | -       |
| HIRCSTB<br>(CLK_STATUS[4])  | 0x0                          | -                            | -                            | -                            | -                            | -       | -                            | -       | -       |
| CLKSFAIL<br>(CLK_STATUS[7])   | 0x0                          | 0x0                          | -                            | -                            | -                            | -       | -                            | -       | -       |
| RSTEN<br>(WDT_CTL[1])   | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | -       | Reload<br>from<br>CONFIG0    | -       | -       |
| WDTEN<br>(WDT_CTL[7])   |                              |                              |                              |                              |                              |         |                              |         |         |
| WDT_CTL<br>except bit 1 and bit 7.  | 0x0700                       | 0x0700                       | 0x0700                       | 0x0700                       | 0x0700                       | -       | 0x0700                       | -       | -       |
| WDT_ALTCTL  | 0x0000                       | 0x0000                       | 0x0000                       | 0x0000                       | 0x0000                       | -       | 0x0000                       | -       | -       |
| WWDT_RLDCNT   | 0x0000                       | 0x0000                       | 0x0000                       | 0x0000                       | 0x0000                       | -       | 0x0000                       | -       | -       |
| WWDT_CTL  | 0x3F0800                     | 0x3F0800                     | 0x3F0800                     | 0x3F0800                     | 0x3F0800                     | -       | 0x3F0800                     | -       | -       |
| WWDT_STATUS   | 0x0000                       | 0x0000                       | 0x0000                       | 0x0000                       | 0x0000                       | -       | 0x0000                       | -       | -       |
| WWDT_CNT  | 0x3F                         | 0x3F                         | 0x3F                         | 0x3F                         | 0x3F                         | -       | 0x3F                         | -       | -       |
| BS<br>(FMC_ISPCTL[1])   | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | -       | Reload<br>from<br>CONFIG0    | -       | -       |
| BL<br>(FMC_ISPCTL[16])  |                              |                              |                              |                              |                              |         |                              |         |         |
| FMC_DFBA  | Reload<br>from<br>CONFIG1    | Reload<br>from<br>CONFIG1    | Reload<br>from<br>CONFIG1    | Reload<br>from<br>CONFIG1    | Reload<br>from<br>CONFIG1    | -       | Reload<br>from<br>CONFIG1    | -       | -       |
| CBS<br>(FMC_ISPSTS[2:1])  | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | Reload<br>from<br>CONFIG0    | -       | Reload<br>from<br>CONFIG0    | -       | -       |
| VECMAP<br>(FMC_ISPSTS[23:9])  | Reload<br>base on<br>CONFIG0 | Reload<br>base on<br>CONFIG0 | Reload<br>base on<br>CONFIG0 | Reload<br>base on<br>CONFIG0 | Reload<br>base on<br>CONFIG0 | -       | Reload<br>base on<br>CONFIG0 | -       | -       |
| Other Peripheral<br>Registers   | Reset Value                  |                              |                              |                              |                              |         |                              |         |         |
| FMC Registers   | Reset Value                  |                              |                              |                              |                              |         |                              |         |         |
| <b>Note:</b> '-' means that the value of register keeps original setting. |                              |                              |                              |                              |                              |         |                              |         |         |

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than  $0.2 V_{DD}$  and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above  $0.7 V_{DD}$  and the state keeps longer than 32 us (glitch filter). The PINRF(SYS\_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset Figure 6-3 shows the nRESET reset waveform.

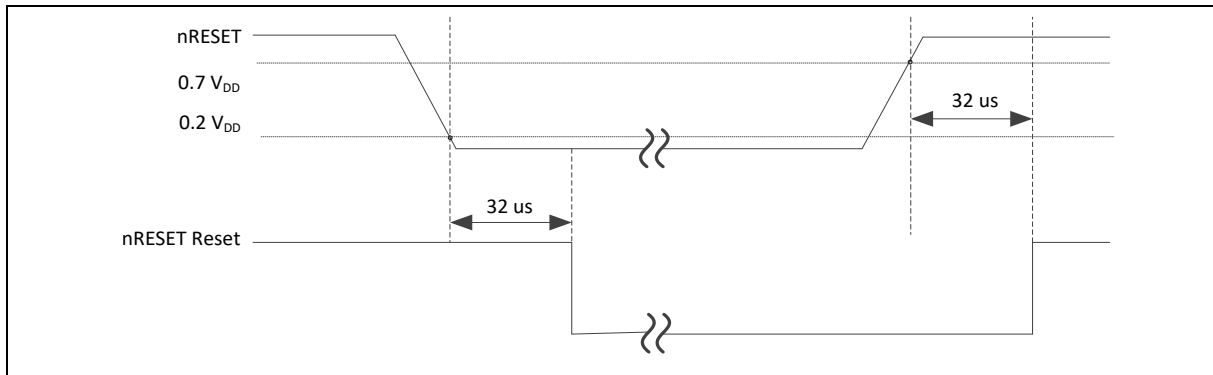


Figure 6-3 nRESET Reset Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS\_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS\_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6-4 shows the power-on reset waveform.

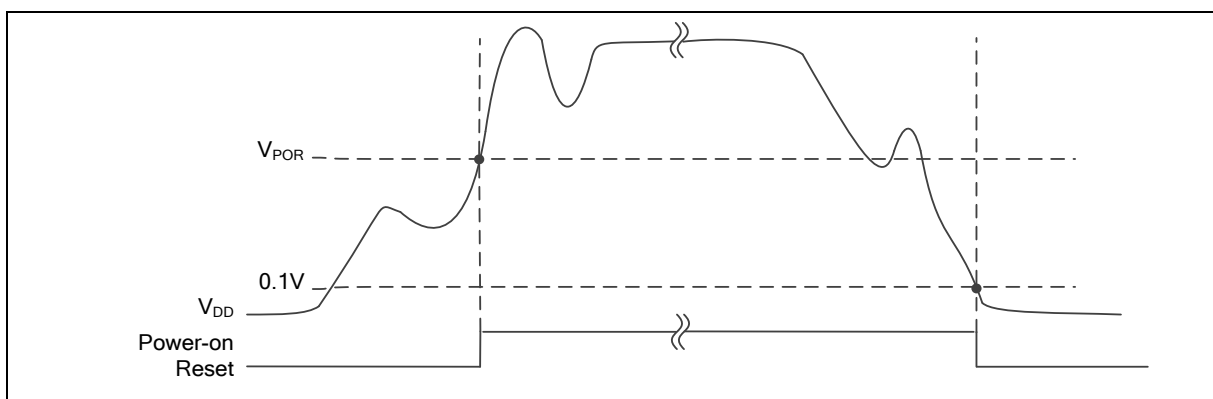


Figure 6-4 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS\_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect  $AV_{DD}$  during system operation. When the  $AV_{DD}$  voltage is lower than  $V_{LVR}$  and the state keeps longer than De-glitch time set by LVRDGSEL (SYS\_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the  $AV_{DD}$  voltage rises above

$V_{LVR}$  and the state keeps longer than De-glitch time set by LVRDGSEL (SYS\_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6-5 shows the Low Voltage Reset waveform.

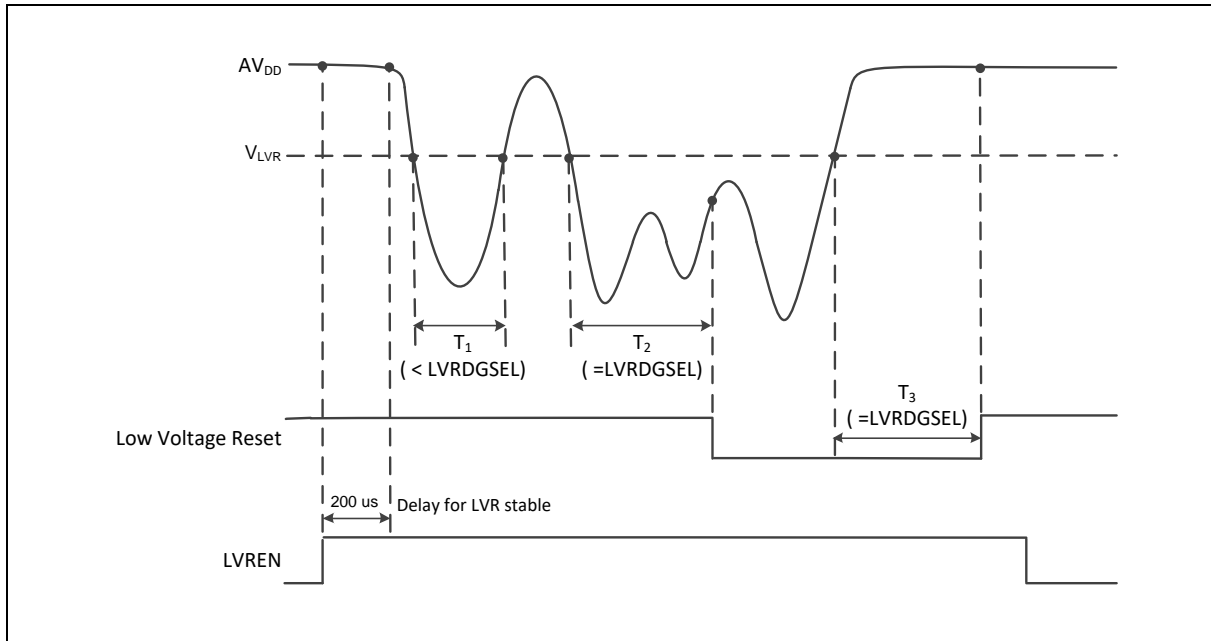


Figure 6-5 Low Voltage Reset (LVR) Waveform

#### 6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS\_BODCTL[0]), Brown-out Detector function will detect  $AV_{DD}$  during system operation. When the  $AV_{DD}$  voltage is lower than  $V_{BOD}$  which is decided by BODEN and BODVL (SYS\_BODCTL[18:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS\_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the  $AV_{DD}$  voltage rises above  $V_{BOD}$  and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS\_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6-6 shows the Brown-out Detector waveform.

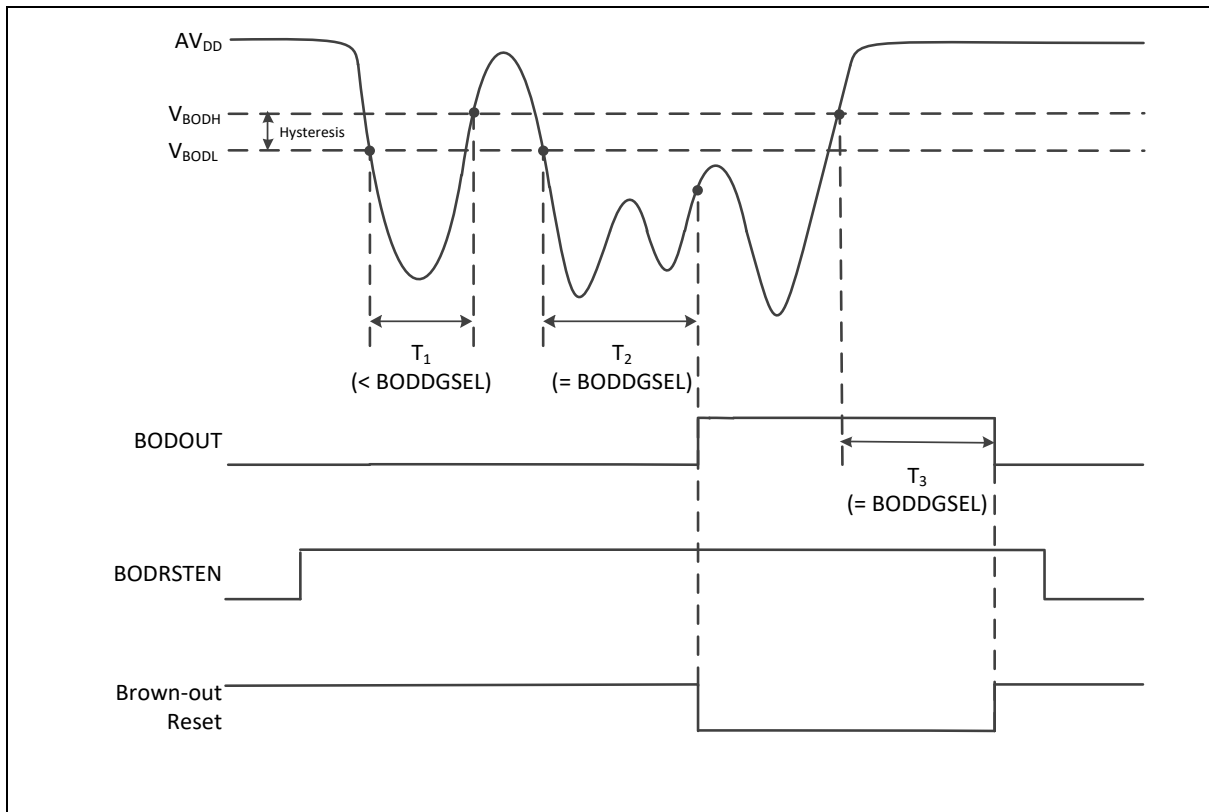


Figure 6-6 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS\_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor’s built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M4 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS\_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC\_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS\_IPRST0[1]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC\_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRC[R2]) to 1 to assert the MCU Reset.

### 6.2.3 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from  $AV_{DD}$  and  $AV_{SS}$  provides the power for analog components operation.
- Digital power from  $V_{DD}$  and  $V_{SS}$  supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from  $V_{BUS}$  offers the power for operating the USB transceiver.
- RTC power from  $V_{BAT}$  provides the power for RTC and 80 bytes backup registers.

The outputs of internal voltage regulators, LDO and  $V_{DD33}$ , require an external capacitor which should be located close to the corresponding pin. Analog power ( $AV_{DD}$ ) should be the same voltage level of the digital power ( $V_{DD}$ ). Figure 6-7 shows the NuMicro® M480 power distribution.

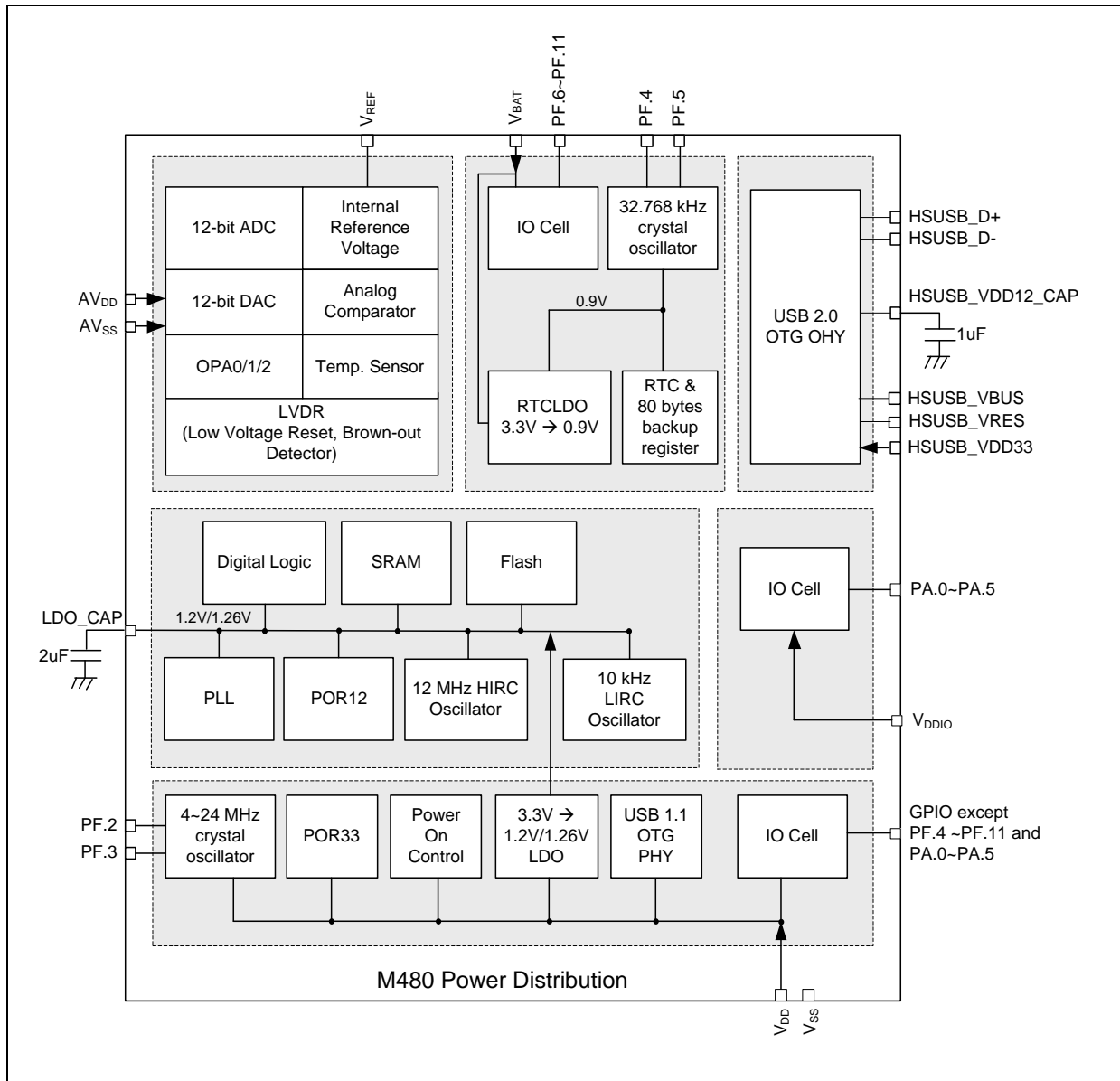


Figure 6-7 NuMicro® M480 Power Distribution Diagram

**Note:**

1. When  $V_{BAT}$  power source first power-on, the power-on reset will happened and reset all  $V_{BAT}$  domain circuit. The I/O in  $V_{BAT}$  domain (PF.4 ~ PF.11) will become floating state and make additional leakage in  $V_{BAT}$  domain. User should power on  $V_{DD}$  first to reset chip and set I/O control to make these I/Os becomes a static state to prevent additional leakage .
2. The  $V_{BAT}$  domain I/O (PF.4 ~ PF.11) will have unpredictable 1.5V glitch during power-on if  $V_{BAT}$  and  $V_{DD}$  connect together. To prevent this unpredictable glitch to make , user should avoid use these pins to be other IC's active or inactive control pins.

### 6.2.4 Power Modes and Wake-up Sources

The NuMicro® M480 series has power manager unit to support several operating modes for saving power. Table 6.2-2 lists all power mode at NuMicro® M480 series.

| Mode  | CPU Operating Maximum Speed ( MHz) | LDO_CAP (V) | Clock Disable   |
|---|------------------------------------|-------------|---|
| Normal mode   | 160                                | 1.20        | All clocks are disabled by control register.  |
| Turbo mode  | 192                                | 1.26        | All clocks are disabled by control register.  |
| Idle mode   | CPU enter Sleep mode               | 1.20/1.26   | Only CPU clock is disabled.   |
| Fast Wakeup Power-down mode (FWPD)                    | CPU enters Deep Sleep mode         | 1.20/1.26   | Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT. |
| Normal Power-down mode (NPD)                          | CPU enters Deep Sleep mode         | 1.20/1.26   | Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT. |
| Low leakage Power-down mode (LLPD)                    | CPU enters Deep Sleep mode         | 0.9         | Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT. |
| Standby Power-down mode (SPD0)                        | Power off                          | Floating    | Only LIRC/LXT still enable for RTC function and wake-up timer usage   |
| Standby Power-down mode (SPD1) (M48xID/M487KMCAN)     | Power off                          | Floating    | Only LIRC/LXT still enable for RTC function and wake-up timer usage   |
| Deep Power-down mode (DPD)*                           | Power off                          | Floating    | Only LIRC/LXT still enable for RTC function and wake-up timer usage   |
| *M487KMCAN doesn't support Deep Power-down mode (DPD) |                                    |             |   |

Table 6.2-2 Power Mode Table

**Note:**

1. User must turn on LIRC before entering SPD0/1 mode.
2. SPD0 mode has 32KB data retention in SRAM bank0. (M48xID/M487KMCAN)
3. SPD0 mode data retention size is configurable. (M48xGC/M48xE8)



There are different power mode entry setting For each power mode, they have different entry setting and leaving condition. Table 6.2-3 shows the entry setting for each power mode. When chip power-on, chip is running ar normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK\_PWRCTL:[7]) and PDMSEL (CLK\_PMUCTL[2:0]) and execute WFI instruction. And

| Register/Instruction Mode                             | SLEEPDEEP (SCR[2]) | PDEN (CLK_PWRCTL[7]) | PDMSEL (CLK_PMUCTL[2:0]) | CPU Run WFI Instruction |
|---|--------------------|----------------------|--------------------------|-------------------------|
| Normal mode   | 0                  | 0                    | 0                        | NO                      |
| Idle mode   | 0                  | 0                    | 0                        | YES                     |
| Fast Wakeup Power-down mode                           | 1                  | 1                    | 2                        | YES                     |
| Normal Power-down mode                                | 1                  | 1                    | 0                        | YES                     |
| Low leakage Power-down mode                           | 1                  | 1                    | 1                        | YES                     |
| Standby Power-down mode 0                             | 1                  | 1                    | 4                        | YES                     |
| Standby Power-down mode 1                             | 1                  | 1                    | 5                        | YES                     |
| Deep Power-down mode*                                 | 1                  | 1                    | 6                        | YES                     |
| *M487KMCAN doesn't support Deep Power-down mode (DPD) |                    |                      |                          |                         |

Table 6.2-3 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-4 lists the available clocks for each power mode.

| Power Mode       | Normal Mode  | Idle Mode                     | Power-Down Mode   |
|------------------|--|-------------------------------|---|
| Definition       | CPU is in active state                             | CPU is in sleep state         | CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended. |
| Entry Condition  | Chip is in normal mode after system reset released | CPU executes WFI instruction. | CPU sets sleep mode enable and power down enable and executes WFI instruction.        |
| Wake-up Sources  | N/A  | All interrupts                | RTC, WDT, I <sup>2</sup> C, Timer, UART, BOD, GPIO, EINT, USCI, USB, ACMP and BOD.    |
| Available Clocks | All  | All except CPU clock          | LXT and LIRC  |
| After Wake-up    | N/A  | CPU back to normal mode       | CPU back to normal mode   |

Table 6.2-4 Power Mode Definition Table

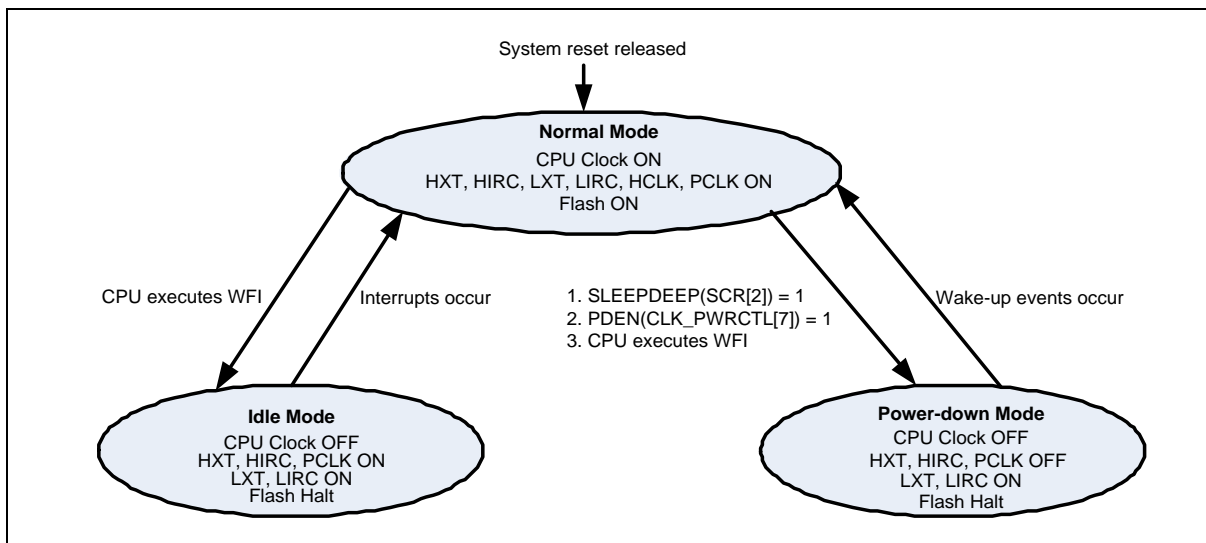


Figure 6-8 Power Mode State Machine

|                | Idle Mode | NPD, LLPD, FWPD     | SPD                 | DPD                   |
|----------------|-----------|---------------------|---------------------|-----------------------|
| HXT            | ON        | Halt                | Halt                | Halt                  |
| HIRC           | ON        | Halt                | Halt                | Halt                  |
| LXT            | ON        | ON/OFF <sup>1</sup> | ON/OFF <sup>1</sup> | ON/OFF <sup>1</sup>   |
| LIRC           | ON        | ON/OFF <sup>2</sup> | ON/OFF <sup>2</sup> | ON/OFF <sup>2,8</sup> |
| PLL            | ON        | Halt                | Halt                | Halt                  |
| HCLK/PCLK      | ON        | Halt                | Halt                | Halt                  |
| CPU            | Halt      | Halt                | Halt                | Halt                  |
| SRAM retention | ON        | ON                  | ON/OFF <sup>7</sup> | Halt                  |
| FLASH          | ON        | Halt                | Halt                | Halt                  |
| TIMER          | ON        | ON/OFF <sup>3</sup> | Halt                | Halt                  |
| WDT            | ON        | ON/OFF <sup>4</sup> | Halt                | Halt                  |
| RTC (LXT)      | ON        | ON/OFF <sup>5</sup> | ON/OFF <sup>5</sup> | ON/OFF <sup>5</sup>   |
| UART           | ON        | ON/OFF <sup>6</sup> | Halt                | Halt                  |
| Others         | ON        | Halt                | Halt                | Halt                  |

Table 6.2-5 Clocks in Power Modes

**Note:**

1. LXT ON or OFF depends on SW setting in normal mode.
2. LIRC ON or OFF depends on S/W setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If RTC clock source is selected as LXT and LXT is on.
6. If UART clock source is selected as LXT and LXT is on.

7. SRAM retention size depends on SW setting in normal mode.
8. If timer wake up function is disabled, LIRC will be disabled automatically when chip enter DPD mode for power saving.

**Wake-up sources in Normal Power-down mode (NPD):**

RTC, WDT, I<sup>2</sup>C, Timer, UART, USCI, BOD, EBOD, GPIO, USB, and ACMP.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-6 lists the condition about how to enter Power-down mode again for each peripheral.

User needs to wait this condition before setting PDEN(CLK\_PWRCTL[7]) and execute WFI to enter Power-down mode.

| Wake-Up Source                              | Wake-Up Condition                    | Power-Down Mode       |     |     | Re-Entering Power-Down Mode Condition   |
|---|--------------------------------------|-----------------------|-----|-----|---|
|   |                                      | NPD/<br>FWPD/<br>LLPD | SPD | DPD |   |
| BOD   | Brown-Out Detector Reset / Interrupt | V                     | -   | -   | After software writes 1 to clear BODIF (SYS_BODCTL[4]).   |
|   | Brown-Out Detector Reset             | -                     | V   | -   | After software writes 1 (CLK_PMUSTS[31]) to clear BODWK (CLK_PMUSTS[13]) when SPD mode is entered.  |
| LVR   | LVR Reset                            | V                     | -   | -   | After software writes 1 to clear LVRF (SYS_RSTSTS[3])   |
|   |                                      | -                     | V   | -   | After software writes 1 (CLK_PMUSTS[31]) to clear LVRWK (CLK_PMUSTS[12]) when SPD mode is entered.  |
| POR   | POR Reset                            | V                     | V   | -   | After software writes 1 to clear PORF (SYS_RSTSTS[0])   |
| INT   | External Interrupt                   | V                     | -   | -   | After software write 1 to clear the Px_INTSRC[n] bit.   |
| GPIO  | GPIO Interrupt                       | V                     | -   | -   | After software write 1 to clear the Px_INTSRC[n] bit.   |
| GPIO(PA~PD) Wake-up pin                     | rising or falling edge event, 64-pin | -                     | V   | -   | After software writes 1 (CLK_PMUSTS[31]) to clear GPxWK (CLK_PMUSTS[11:8]) when SPD mode is entered.  |
| GPIO(PC.0) Wake-up pin                      | rising or falling edge event , 1-pin | -                     | -   | V   | After software writes 1 (CLK_PMUSTS[31]) to clear PINWK0 (CLK_PMUSTS[0]) when DPD mode is entered. (M48xID Only)                            |
| GPIO(PC.0/PB.0/PB.2/PB.12/PF.6) Wake-up pin | rising or falling edge event, 5-pin  | -                     | -   | V   | After software writes 1 (CLK_PMUSTS[31]) to clear PINWKx (CLK_PMUSTS[6:3] and CLK_PMUSTS[0]) when DPD mode is entered. (M48xGC/M48xE8 Only) |
| TIMER                                       | Timer Interrupt                      | V                     | -   | -   | After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).  |
| Wakeup timer                                | Wakeup by wake-up timer time-out     | -                     | V   | V   | After software writes 1 (CLK_PMUSTS[31]) to clear TMRWK (CLK_PMUSTS[1]) when SPD or DPD mode is entered.                                    |

| Wake-Up Source        | Wake-Up Condition                        | Power-Down Mode       |     |                          | Re-Entering Power-Down Mode Condition  |
|-----------------------|--|-----------------------|-----|--------------------------|--|
|                       |  | NPD/<br>FWPD/<br>LLPD | SPD | DPD                      |  |
| WDT                   | WDT Interrupt                            | V                     | -   | -                        | After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).   |
| RTC                   | Alarm Interrupt                          | V                     | -   | -                        | After software writes 1 to clear ALMIF (RTC_INTSTS[0]).  |
|                       | Time Tick Interrupt                      | V                     | -   | -                        | After software writes 1 to clear TICKIF (RTC_INTSTS[1]).   |
|                       | Wakeup by RTC alarm                      | -                     | V   | V<br>(M48xGC/<br>M48xE8) | After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when DPD or SPD mode is entered.                                 |
|                       | Wakeup by RTC tick time                  | -                     | V   | V<br>(M48xGC/<br>M48xE8) | After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when DPD or SPD mode is entered.                                 |
|                       | Wakeup by tamper event                   | -                     | V   | V<br>(M48xGC/<br>M48xE8) | After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when DPD or SPD mode is entered.                                 |
| UART                  | nCTS wake-up                             | V                     | -   | -                        | After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).  |
|                       | RX Data wake-up                          | V                     | -   | -                        | After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).  |
|                       | Received FIFO Threshold Wake-up          | V                     | -   | -                        | After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).   |
|                       | RS-485 AAD Mode Wake-up                  | V                     | -   | -                        | After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).  |
|                       | Received FIFO Threshold Time-out Wake-up | V                     | -   | -                        | After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).   |
| USCI UART             | CTS Toggle                               | V                     | -   | -                        | After software writes 1 to clear WKF (UUART_WKSTS[0]).   |
|                       | Data Toggle                              | V                     | -   | -                        | After software writes 1 to clear WKF (UUART_WKSTS[0]).   |
| USCI I <sup>2</sup> C | Data toggle                              | V                     | -   | -                        | After software writes 1 to clear WKF (UI2C_WKSTS[0]).  |
|                       | Address match                            | V                     | -   | -                        | After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]).                                 |
| USCI SPI              | SS Toggle                                | V                     | -   | -                        | After software writes 1 to clear WKF (USPI_WKSTS[0]).  |
| I <sup>2</sup> C      | Address match wake-up                    | V                     | -   | -                        | After software writes 1 to clear WKAKDONE (I <sup>2</sup> C_WKSTS[1]). Then software writes 1 to clear WKIF (I <sup>2</sup> C_WKSTS[0]). |

| Wake-Up Source | Wake-Up Condition                       | Power-Down Mode       |     |     | Re-Entering Power-Down Mode Condition  |
|----------------|---|-----------------------|-----|-----|--|
|                |   | NPD/<br>FWPD/<br>LLPD | SPD | DPD |  |
| USB            | Remote Wake-up                          | V                     | -   | -   | After software writes 1 to clear BUSIF (USB_INTSTS[0]).  |
| ACMP           | Comparator Power-Down Wake-Up Interrupt | V                     | -   | -   | After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).                |
| ACMP           | ACMPO status change                     | -                     | V   | -   | After software writes 1 (CLK_PMUSTS[31]) to clear ACMPO (CLK_PMUSTS[14]) when SPD mode is entered. |

Table 6.2-6 Re-Entering Power-down Mode Condition

6.2.5 Power Modes and Power Level Transition

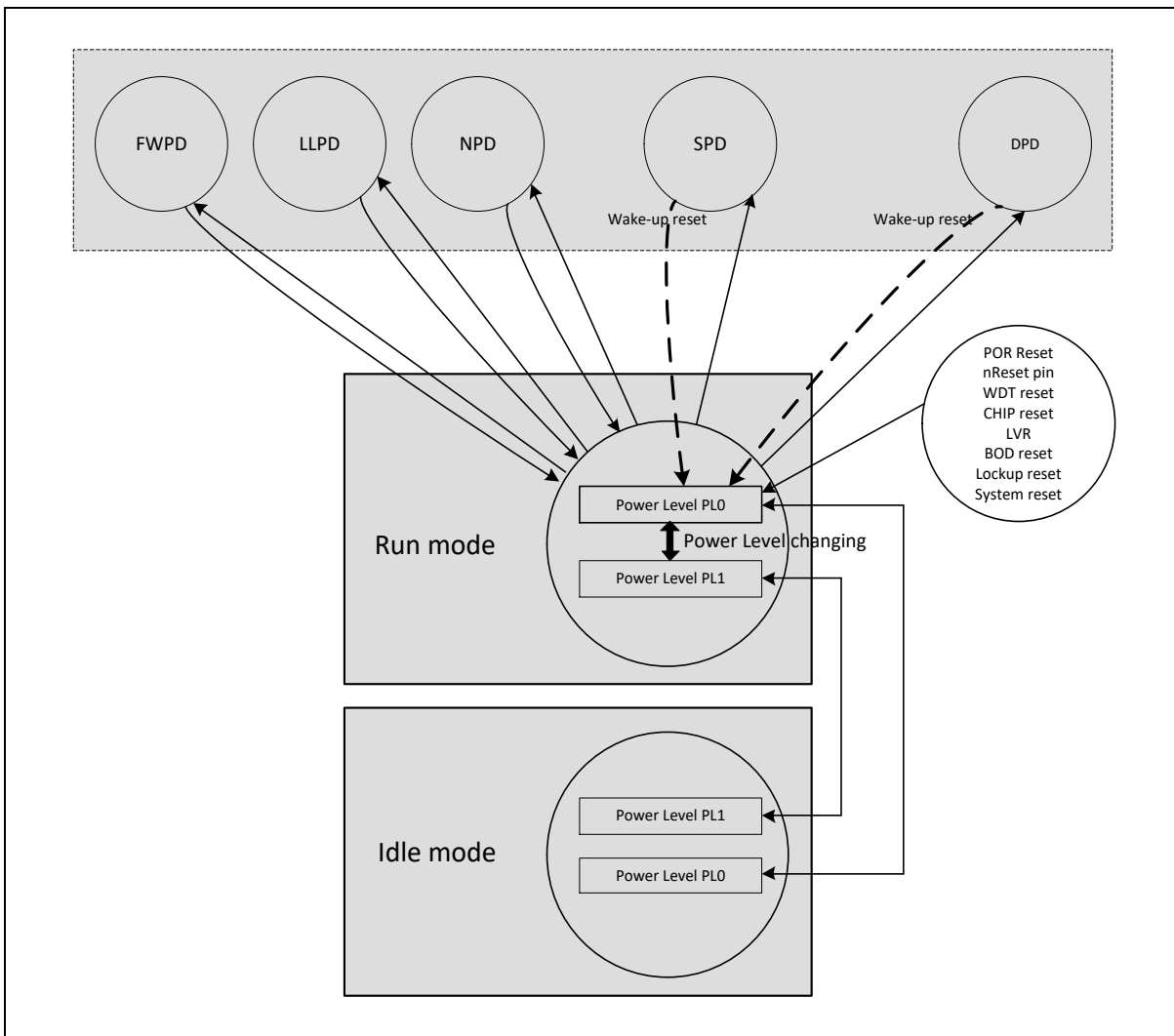


Figure 6-9 NuMicro® M480 Power Distribution Diagram

### 6.2.6 System Memory Map

The NuMicro® M480 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The NuMicro® M480 series only supports little-endian data format.

| Address Space  | Token     | Controllers  |
|--|-----------|--|
| Flash and SRAM Memory Space                              |           |  |
| 0x0000_0000 – 0x0003_FFFF                                | FLASH_BA  | FLASH Memory Space (256 Kbytes)                                      |
| 0x0000_0000 – 0x0007_FFFF                                | FLASH_BA  | FLASH Memory Space (512 Kbytes)                                      |
| 0x0800_0000 – 0x09FF_FFFF                                | SPIM_BA   | SPIM Memory Space (32 Mbytes) (M48xID)                               |
| 0x0800_0000 – 0x081F_FFFF                                | SPIM_BA   | Embedded SPI Flash Space(2 Mbytes) (M487KMCAN)                       |
| 0x2000_0000 – 0x2000_7FFF                                | SRAM0_BA  | SRAM Memory Space (32 Kbytes)  |
| 0x2000_8000 – 0x2001_FFFF                                | SRAM1_BA  | SRAM Memory Space (96 Kbytes)  |
| 0x2002_0000 – 0x2002_7FFF                                | SRAM2_BA  | SRAM Memory Space (32 Kbytes) for CPU only and share with SPIM cache |
| 0x6000_0000 – 0x6FFF_FFFF                                | EXTMEM_BA | External Memory Space (256 Mbytes)                                   |
| Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF) |           |  |
| 0x4000_0000 – 0x4000_01FF                                | SYS_BA    | System Control Registers   |
| 0x4000_0200 – 0x4000_02FF                                | CLK_BA    | Clock Control Registers  |
| 0x4000_0300 – 0x4000_03FF                                | NMI_BA    | NMI Control Registers  |
| 0x4000_4000 – 0x4000_4FFF                                | GPIO_BA   | GPIO Control Registers   |
| 0x4000_7000 – 0x4000_7FFF                                | SPIM_BA   | SPIM Control Registers   |
| 0x4000_8000 – 0x4000_8FFF                                | PDMA_BA   | Peripheral DMA Control Registers                                     |
| 0x4000_9000 – 0x4000_9FFF                                | USBH_BA   | USB Host Control Registers   |
| 0x4000_B000 – 0x4000_BFFF                                | EMAC_BA   | Ethernet MAC Control Registers                                       |
| 0x4000_C000 – 0x4000_CFFF                                | FMC_BA    | Flash Memory Control Registers                                       |
| 0x4000_D000 – 0x4000_DFFF                                | SDH0_BA   | SDHOST0 Control Registers  |
| 0x4000_E000 – 0x4000_EFFF                                | SDH1_BA   | SDHOST1 Control Registers  |
| 0x4001_0000 – 0x4001_0FFF                                | EBI_BA    | External Bus Interface Control Registers                             |
| 0x4001_9000 – 0x4001_9FFF                                | HSUSBD_BA | HSUSBD Control Registers   |
| 0x4001_A000 – 0x4001_AFFF                                | HSUSBH_BA | HSUSBH Host Control Registers  |
| 0x4003_0000 – 0x4003_0FFF                                | CCAP_BA   | CCAP Control Registers   |
| 0x4003_1000 – 0x4003_1FFF                                | CRC_BA    | CRC Generator Registers  |
| 0x4003_E000 – 0x4003_EFFF                                | SWDC_BA   | SWD Control Registers  |
| 0x4003_F000 – 0x4003_FFFF                                | ETMC_BA   | ETM Control Registers  |
| 0x5008_0000 – 0x5008_0FFF                                | CRYP_BA   | Cryptographic Accelerator Registers                                  |
| APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)        |           |  |

| Address Space             | Token                | Controllers   |
|---------------------------|----------------------|---|
| 0x4004_0000 – 0x4004_0FFF | WDT_BA               | Watchdog Timer Control Registers                              |
| 0x4004_1000 – 0x4004_1FFF | RTC_BA               | Real Time Clock (RTC) Control Register                        |
| 0x4004_3000 – 0x4004_3FFF | EADC0_BA             | Enhanced Analog-Digital-Converter 0 (EADC0) Control Registers |
| 0x4004_5000 – 0x4004_5FFF | ACMP01_BA            | Analog Comparator 0/ 1 Control Registers                      |
| 0x4004_6000 – 0x4004_6FFF | OPA_BA               | OP Amplifier Control Registers                                |
| 0x4004_7000 – 0x4004_7FFF | DAC_BA               | DAC Control Registers   |
| 0x4004_8000 – 0x4004_8FFF | I <sup>2</sup> S0_BA | I <sup>2</sup> S0 Interface Control Registers                 |
| 0x4004_B000 – 0x4004_BFFF | EADC1_BA             | Enhanced Analog-Digital-Converter 1 (EADC1) Control Registers |
| 0x4004_D000 – 0x4004_DFFF | OTG_BA               | OTG Control Registers   |
| 0x4004_F000 – 0x4004_FFFF | HSOTG_BA             | HSOTG Control Registers                                       |
| 0x4005_0000 – 0x4005_0FFF | TMR01_BA             | Timer0/Timer1 Control Registers                               |
| 0x4005_1000 – 0x4005_1FFF | TMR23_BA             | Timer2/Timer3 Control Registers                               |
| 0x4005_8000 – 0x4005_8FFF | EPWM0_BA             | EPWM0 Control Registers                                       |
| 0x4005_9000 – 0x4005_9FFF | EPWM1_BA             | EPWM1 Control Registers                                       |
| 0x4005_A000 – 0x4005_AFFF | BPWM0_BA             | BPWM0 Control Registers                                       |
| 0x4005_B000 – 0x4005_BFFF | BPWM1_BA             | BPWM1 Control Registers                                       |
| 0x4006_0000 – 0x4006_0FFF | QSPI0_BA             | QSPI0 Control Registers                                       |
| 0x4006_1000 – 0x4006_1FFF | SPI0_BA              | SPI0 Control Registers  |
| 0x4006_2000 – 0x4006_2FFF | SPI1_BA              | SPI1 Control Registers  |
| 0x4006_3000 – 0x4006_3FFF | SPI2_BA              | SPI2 Control Registers  |
| 0x4006_4000 – 0x4006_4FFF | SPI3_BA              | SPI3 Control Registers  |
| 0x4006_9000 – 0x4006_9FFF | QSPI1_BA             | QSPI1 Control Registers                                       |
| 0x4007_0000 – 0x4007_0FFF | UART0_BA             | UART0 Control Registers                                       |
| 0x4007_1000 – 0x4007_1FFF | UART1_BA             | UART1 Control Registers                                       |
| 0x4007_2000 – 0x4007_2FFF | UART2_BA             | UART2 Control Registers                                       |
| 0x4007_3000 – 0x4007_3FFF | UART3_BA             | UART3 Control Registers                                       |
| 0x4007_4000 – 0x4007_4FFF | UART4_BA             | UART4 Control Registers                                       |
| 0x4007_5000 – 0x4007_5FFF | UART5_BA             | UART5 Control Registers                                       |
| 0x4007_6000 – 0x4007_6FFF | UART6_BA             | UART6 Control Registers                                       |
| 0x4007_7000 – 0x4007_7FFF | UART7_BA             | UART7 Control Registers                                       |
| 0x4008_0000 – 0x4008_0FFF | I <sup>2</sup> C0_BA | I <sup>2</sup> C0 Control Registers                           |
| 0x4008_1000 – 0x4008_1FFF | I <sup>2</sup> C1_BA | I <sup>2</sup> C1 Control Registers                           |
| 0x4008_2000 – 0x4008_2FFF | I <sup>2</sup> C2_BA | I <sup>2</sup> C2 Control Registers                           |
| 0x4009_0000 – 0x4009_0FFF | SC0_BA               | Smartcard Host 0 Control Registers                            |

| Address Space  | Token    | Controllers                                     |
|--|----------|---|
| 0x4009_1000 – 0x4009_1FFF                            | SC1_BA   | Smartcard Host 1 Control Registers              |
| 0x4009_2000 – 0x4009_2FFF                            | SC2_BA   | Smartcard Host 2 Control Registers              |
| 0x4009_3000 – 0x4009_3FFF                            | SC3_BA   | Smartcard Host 3 Control Registers              |
| 0x400A_0000 – 0x400A_0FFF                            | CAN0_BA  | CAN0 Bus Control Registers                      |
| 0x400A_1000 – 0x400A_1FFF                            | CAN1_BA  | CAN1 Bus Control Registers                      |
| 0x400A_2000 – 0x400A_2FFF                            | CAN2_BA  | CAN2 Bus Control Registers                      |
| 0x400B_0000 – 0x400B_0FFF                            | QEI0_BA  | QEI0 Control Registers                          |
| 0x400B_1000 – 0x400B_1FFF                            | QEI1_BA  | QEI1 Control Registers                          |
| 0x400B_4000 – 0x400B_4FFF                            | ECAP0_BA | ECAP0 Control Registers                         |
| 0x400B_5000 – 0x400B_5FFF                            | ECAP1_BA | ECAP1 Control Registers                         |
| 0x400B_9000 – 0x400B_9FFF                            | TRNG_BA  | TRNG Control Registers                          |
| 0x400C_0000 – 0x400C_0FFF                            | USBD_BA  | USB Device Control Register                     |
| 0x400D_0000 – 0x400D_0FFF                            | USCI0_BA | USCI0 Control Registers                         |
| 0x400D_1000 – 0x400D_1FFF                            | USCI1_BA | USCI1 Control Registers                         |
| System Controllers Space (0xE000_E000 ~ 0xE000_EFFF) |          |   |
| 0xE000_E010 – 0xE000_E0FF                            | SCS_BA   | System Timer Control Registers                  |
| 0xE000_E100 – 0xE000_ECFF                            | SCS_BA   | External Interrupt Controller Control Registers |
| 0xE000_ED00 – 0xE000_ED8F                            | SCS_BA   | System Control Registers                        |

Table 6.2-7 Address Space Assignments for On-Chip Controllers

### 6.2.7 SRAM Memory Organization

The M480 series supports embedded SRAM with total 160 Kbytes size and the SRAM organization is separated to three banks: SRAM bank0 and SRAM bank1 and SRAM bank2. The first bank has 32 Kbytes address space, the second bank has 96 Kbyte address space and the third bank has 32Kbyte. These three banks address space can be accessed simultaneously. The SRAM bank0 supports parity error check to make sure chip operating more stable. The SRAM bank2 is shared with SPIM cache, it can switch to external SPI Flash cache memory. Note that SRAM bank2 has additional two wait cycles when reading data.

- Supports total 160 Kbytes SRAM
- Supports byte / half word / word write
- Supports fixed 32 Kbytes SRAM bank0 for independent access
- Supports parity error check function for SRAM bank0
- Supports oversize response error
- Supports remap address to 0x1000\_0000



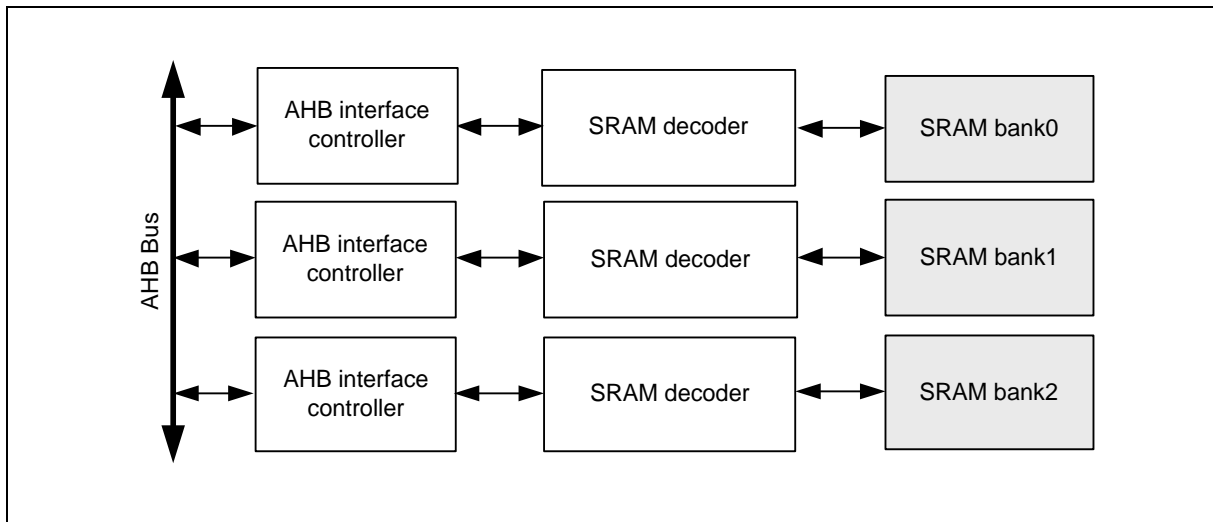


Figure 6-10 SRAM Block Diagram

Figure 6-10 shows the SRAM organization of M480. There are three SRAM banks in M480. The bank0 is addressed to 32 Kbytes, the bank1 is addressed to 96 Kbytes and the bank2 is addressed to 32 Kbyte. The bank0 address space is from 0x2000\_0000 to 0x2000\_7FFF. The bank1 address space is from 0x2000\_8000 to 0x2001\_FFFF. The bank2 address space is from 0x2002\_0000 to 0x2002\_7FFF. The address between 0x2002\_8000 to 0x3FFF\_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

|            | 160 Kbytes Device  | 128 Kbytes Device  | 64KB Device  | Read Access                           |
|------------|--|--|--|---------------------------------------|
| SRAM bank0 | 0x2000_0000 ~ 0x2000_7FFF<br>or<br>0x1000_0000 ~ 0x1000_7FFF | 0x2000_0000 ~ 0x2000_7FFF<br>or<br>0x1000_0000 ~ 0x1000_7FFF | 0x2000_0000 ~ 0x2000_7FFF<br>or<br>0x1000_0000 ~ 0x1000_7FFF | Zero wait cycle for continuous access |
| SRAM bank1 | 0x2000_8000 ~ 0x2001_FFFF<br>or<br>0x1000_8000 ~ 0x1001_FFFF | 0x2000_8000 ~ 0x2001_FFFF<br>or<br>0x1000_8000 ~ 0x1001_FFFF | 0x2000_8000 ~ 0x2000_FFFF<br>or<br>0x1000_8000 ~ 0x1000_FFFF | Zero wait cycle for continuous access |
| SRAM bank2 | 0x2002_0000 ~ 0x2002_7FFF<br>or<br>0x1002_0000 ~ 0x1002_7FFF |  |  | Two wait cycles                       |

Table 6.2-8 SRAM Organization

The address of each bank is remapping from 0x2000\_0000 to 0x1000\_0000. CPU can access SRAM bank0 through 0x2000\_0000 to 0x2000\_7FFF or 0x1000\_0000 to 0x1000\_7FFF, and access SRAM bank1 through 0x2000\_8000 to 0x2001\_FFFF or 0x1000\_8000 to 0x1001\_FFFF, and access SRAM bank2 through 0x2002\_0000 to 0x2002\_7FFF or 0x1002\_0000 to 0x1002\_7FFF.

When setting the control register CCMEN(SPIM\_CTL1[2]) to 0, SRAM bank2 is switched to external SPI Flash cache memory. In this case, the SRAM bank2 can't be accessed as general SRAM. If user access SRAM bank2 by AHB bus master, the SPI Flash controller will send error response via HRESP AHB bus signal to bus master.

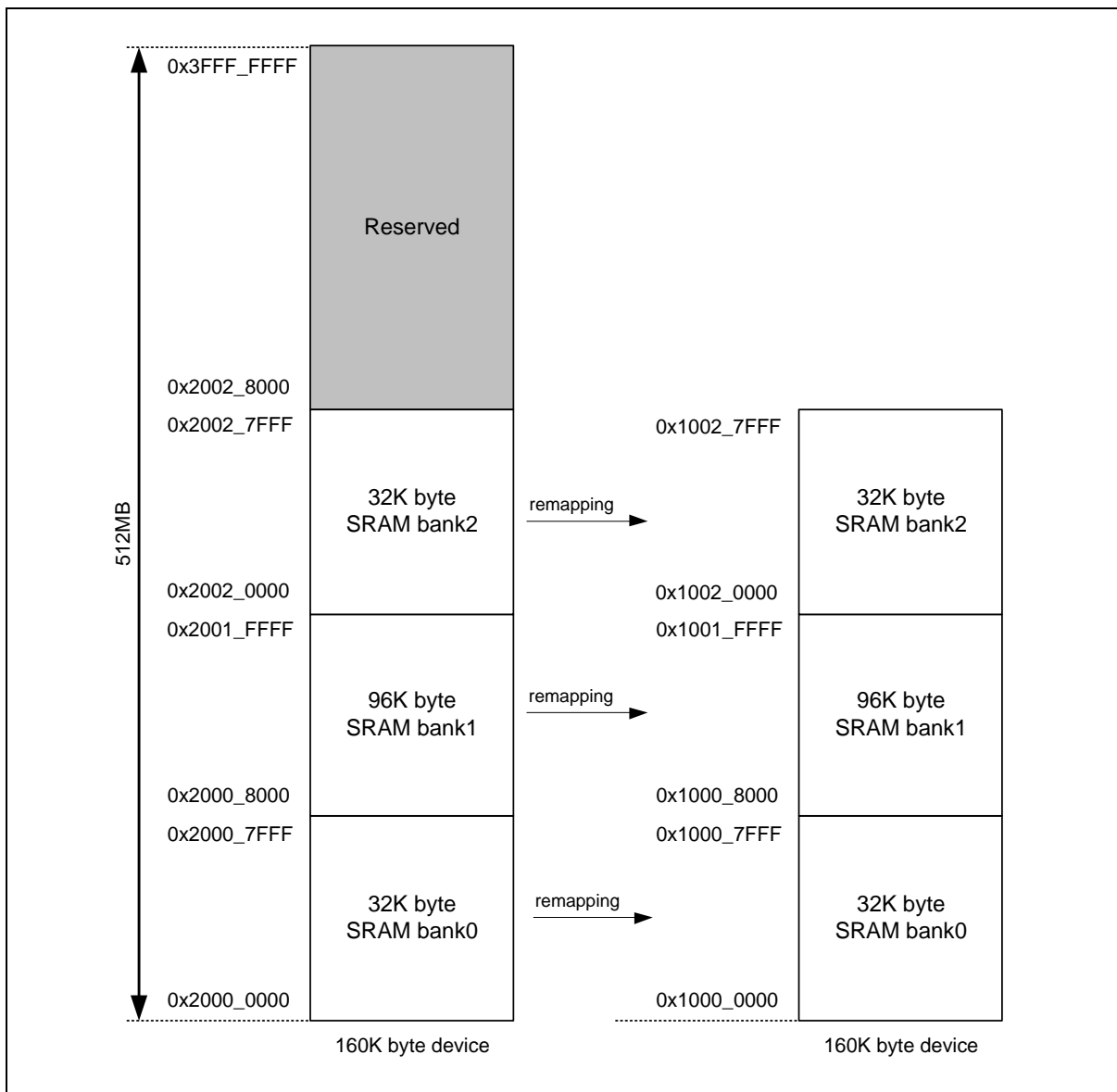


Figure 6-11 SRAM Memory Organization

SRAM bank0 has byte parity error check function. When CPU is accessing SRAM bank0, the parity error checking mechanism is dynamic operating. As parity error occurred, the PERRIF (SYS\_SRAM\_STATUS[0]) will be asserted to 1 and the SYS\_SRAM\_ERRADDR register will recode the address with parity error. Chip will enter interrupt when SRAM parity error occurred if PERRIEN (SYS\_SRAM\_INTCTL[0]) is set to 1. When SRAM parity error occurred, chip will stop detecting SRAM parity error until user writes 1 to clear the PERRIF(SYS\_SRAM\_STATUS[0]) bit.

### 6.2.8 Bus Matrix

The M480 supports Bus Matrix to manage the access arbitration between masters. The access arbitration can be selected by INTACTEN (SYS\_AHBCTL[0]) to use round-robin algorithm or set Cortex®-M4 CPU as the highest bus priority.

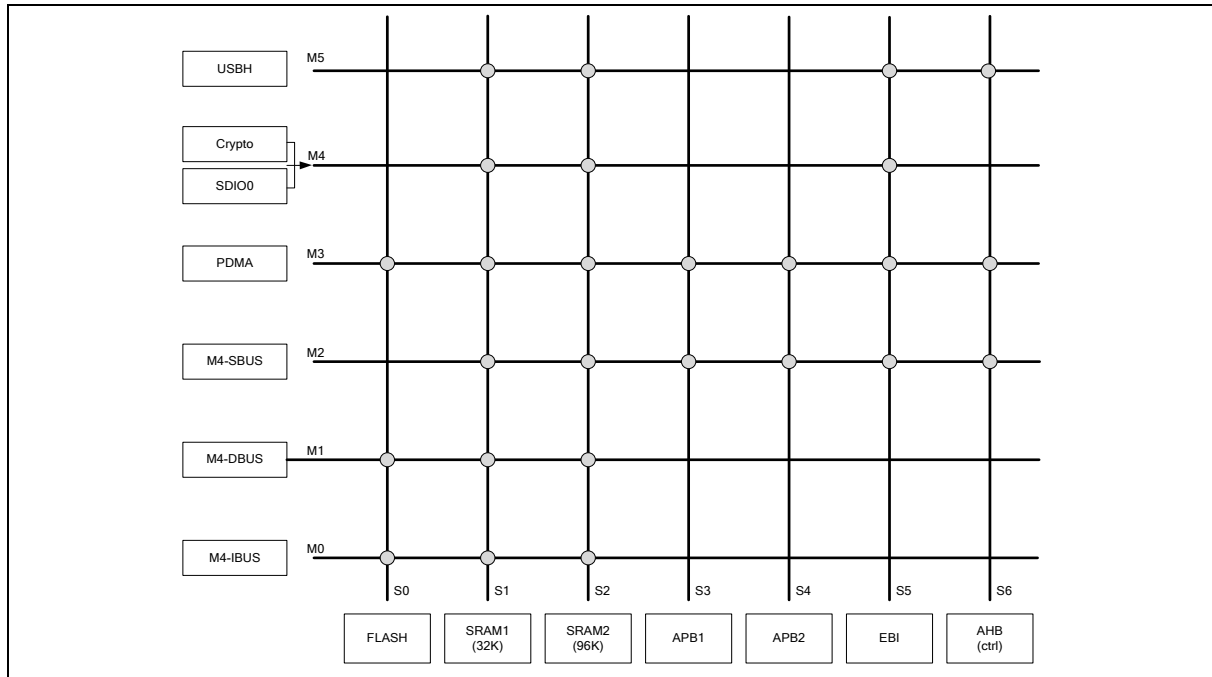


Figure 6-12 NuMicro® M480 Bus Matrix Diagram

### 6.2.9 HIRC Auto Trim

This chip supports auto-trim function: the HIRC trim (12 MHz RC oscillator) and HIRC trim (48 MHz RC oscillator), according to the accurate LXT (32.768 kHz crystal oscillator) or internal USB synchronous mode, automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 12 MHz clock. In such case, if neither using use PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS\_IRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS\_IRCTCTL[1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS\_IRCTSTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

In HIRC case, the system needs an accurate 48 MHz clock. In such case, if neither using use PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS\_HIRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS\_HIRCTCTL[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS\_HIRCTSTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

**6.2.10 Register Lock Control**

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS\_REGLCTL address at 0x4000\_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

|                  |                     |
|------------------|---------------------|
| SYS_IPRST0       | Address 0x4000_0008 |
| SYS_BODCTL       | address 0x4000_0018 |
| SYS_VREFCTL      | address 0x4000_0028 |
| SYS_USBPHY       | address 0x4000_002C |
| SYS_SRAM_BISTCTL | address 0x4000_00D0 |
| SYS_PORDISAN     | address 0x4000_01EC |
| SYS_PLCTL        | address 0x4000_01F8 |
| CLK_PWRCTL       | address 0x4000_0200 |
| CLK_APBCLK0      | address 0x4000_0208 |
| CLK_CLKSELO      | address 0x4000_0210 |
| CLK_CLKSEL1      | address 0x4000_0214 |
| CLK_PLLCTL       | address 0x4000_0240 |
| CLK_PMUCTL       | address 0x4000_0290 |
| NMIEN            | address 0x4000_0300 |
| AHBMCTL          | address 0x4000_0400 |
| FMC_FTCTL        | address 0x4000_5018 |
| FMC_ICPCMD       | address 0x4000_501C |
| FMC_ISPCTL       | address 0x4000_C000 |
| FMC_ISPTRG       | address 0x4000_C010 |
| FMC_ISPSTS       | address 0x4000_C040 |
| FMC_CYCCTL       | address 0x4000_C04C |
| FMC_KPKEYTRG     | address 0x4000_C05C |
| FMC_KPKEYSTS     | address 0x4000_C060 |
| WDT_CTL          | address 0x4004_0000 |
| WDT_ALTCTL       | address 0x4004_0004 |
| TIMER0_CTL       | address 0x4005_0000 |
| TIMER1_CTL       | address 0x4005_0100 |
| TIMER2_CTL       | address 0x4005_1000 |
| TIMER3_CTL       | address 0x4005_1100 |
| TIMER0_PWMCTL    | address 0x4005_0040 |
| TIMER1_PWMCTL    | address 0x4005_0140 |
| TIMER2_PWMCTL    | address 0x4005_1040 |

|                   |                                 |
|-------------------|---------------------------------|
| TIMER3_PWMCTL     | address 0x4005_1140             |
| TIMER0_PWMDTCTL   | address 0x4005_0058             |
| TIMER1_PWMDTCTL   | address 0x4005_0158             |
| TIMER2_PWMDTCTL   | address 0x4005_1058             |
| TIMER3_PWMDTCTL   | address 0x4005_1158             |
| TIMER0_PWMBRKCTL  | address 0x4005_0070             |
| TIMER1_PWMBRKCTL  | address 0x4005_0170             |
| TIMER2_PWMBRKCTL  | address 0x4005_1070             |
| TIMER3_PWMBRKCTL  | address 0x4005_1170             |
| TIMER0_PWMSWBRK   | address 0x4005_007C             |
| TIMER1_PWMSWBRK   | address 0x4005_017C             |
| TIMER2_PWMSWBRK   | address 0x4005_107C             |
| TIMER3_PWMSWBRK   | address 0x4005_117C             |
| TIMER0_PWMINTEN1  | address 0x4005_0084             |
| TIMER1_PWMINTEN1  | address 0x4005_0184             |
| TIMER2_PWMINTEN1  | address 0x4005_1084             |
| TIMER3_PWMINTEN1  | address 0x4005_1184             |
| TIMER0_PWMINTSTS1 | address 0x4005_008C             |
| TIMER1_PWMINTSTS1 | address 0x4005_018C             |
| TIMER2_PWMINTSTS1 | address 0x4005_108C             |
| TIMER3_PWMINTSTS1 | address 0x4005_118C             |
| EPWM_CTL0         | address 0x4005_8000/0x4005_9000 |
| EPWM_CTL1         | address 0x4005_8000/0x4005_9000 |
| EPWM_DTCTL0_1     | address 0x4005_8070/0x4005_9070 |
| EPWM_DTCTL2_3     | address 0x4005_8074/0x4005_9074 |
| EPWM_DTCTL4_5     | address 0x4005_8078/0x4005_9078 |
| EPWM_BRKCTL0_1    | address 0x4005_80C8/0x4005_90C8 |
| EPWM_BRKCTL2_3    | address 0x4005_80CC/0x4005_90CC |
| EPWM_BRKCTL4_5    | address 0x4005_80D0/0x4005_90D0 |
| EPWM_SWBRK        | address 0x4005_80DC/0x4005_90DC |
| EPWM_INTEN1       | address 0x4005_80E4/0x4005_90E4 |
| EPWM_INTSTS1      | address 0x4005_80EC/0x4005_90EC |
| BPWM_CTL0         | address 0x4005_A000/0x4005_B000 |
| SYST_VAL          | address 0xE000_E018             |

### 6.2.11 System Timer (SysTick)

The Cortex®-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST\_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST\_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST\_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST\_LOAD value rather than an arbitrary value when it is enabled.

If the SYST\_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “*Arm® Cortex®-M4 Technical Reference Manual*” and “*Arm® v6-M Architecture Reference Manual*”.

### 6.2.12 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-16 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

## 6.3 Clock Controller

### 6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK\_PWRCTL[7]) and Cortex®-M4F core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 12 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6-13 shows the clock generator and the overview of the clock source control.



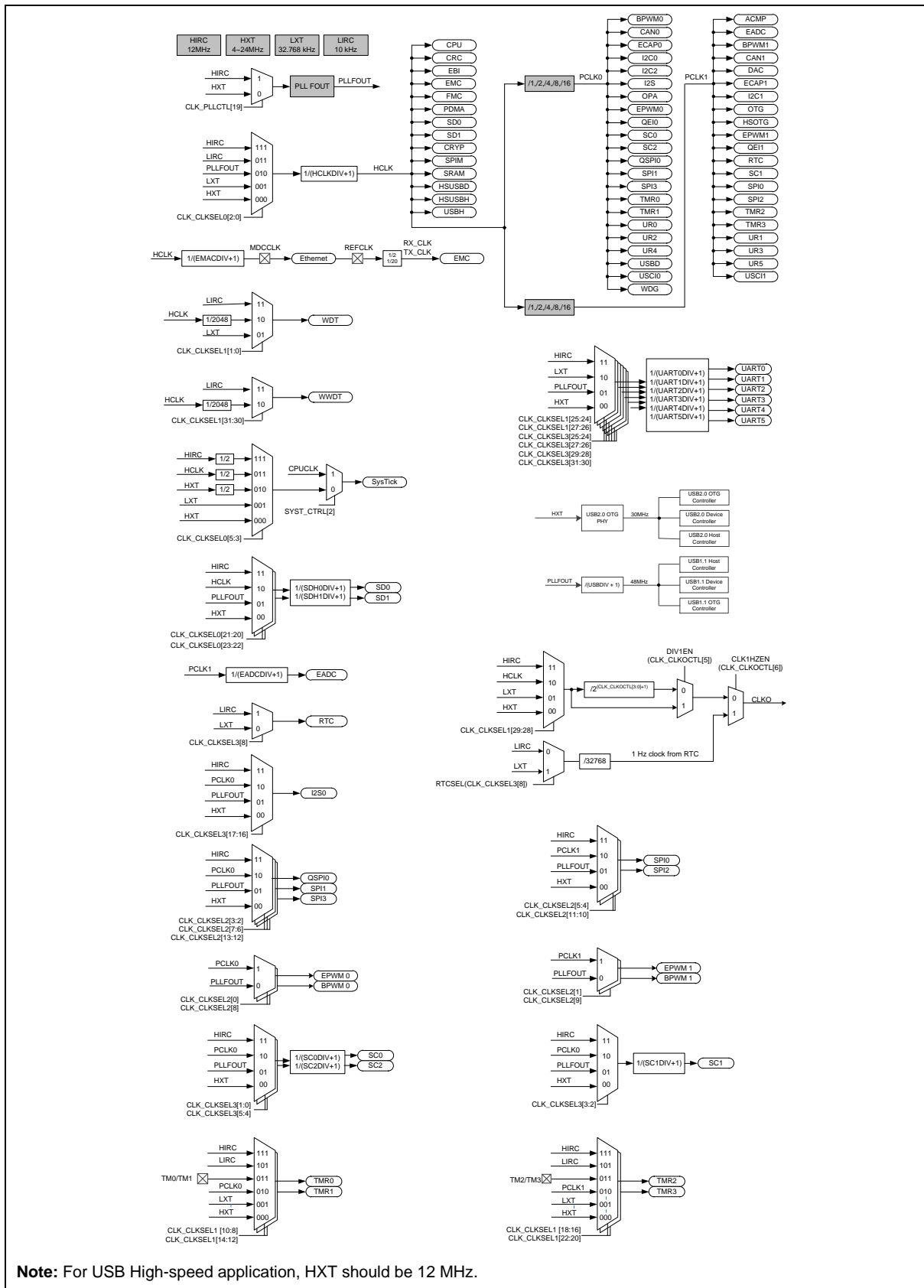


Figure 6-13 Clock Generator Global View Diagram (M48xID/M487KMCAN)

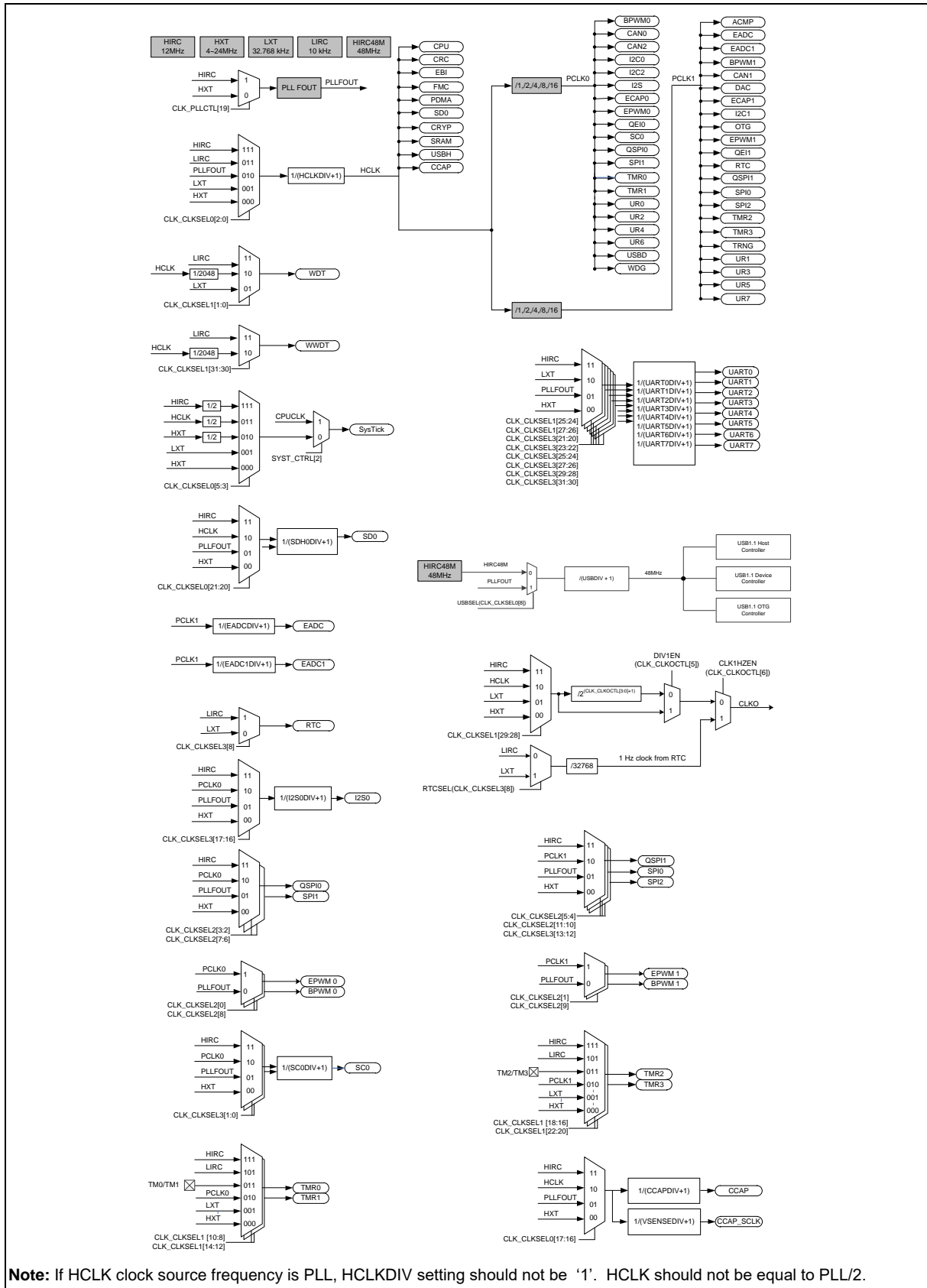


Figure 6-14 Clock Generator Global View Diagram (M48xGC/M48xE8)

### 6.3.2 Clock Generator

The clock generator consists of 5 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 12 MHz internal high speed oscillator (HIRC)
- 12 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

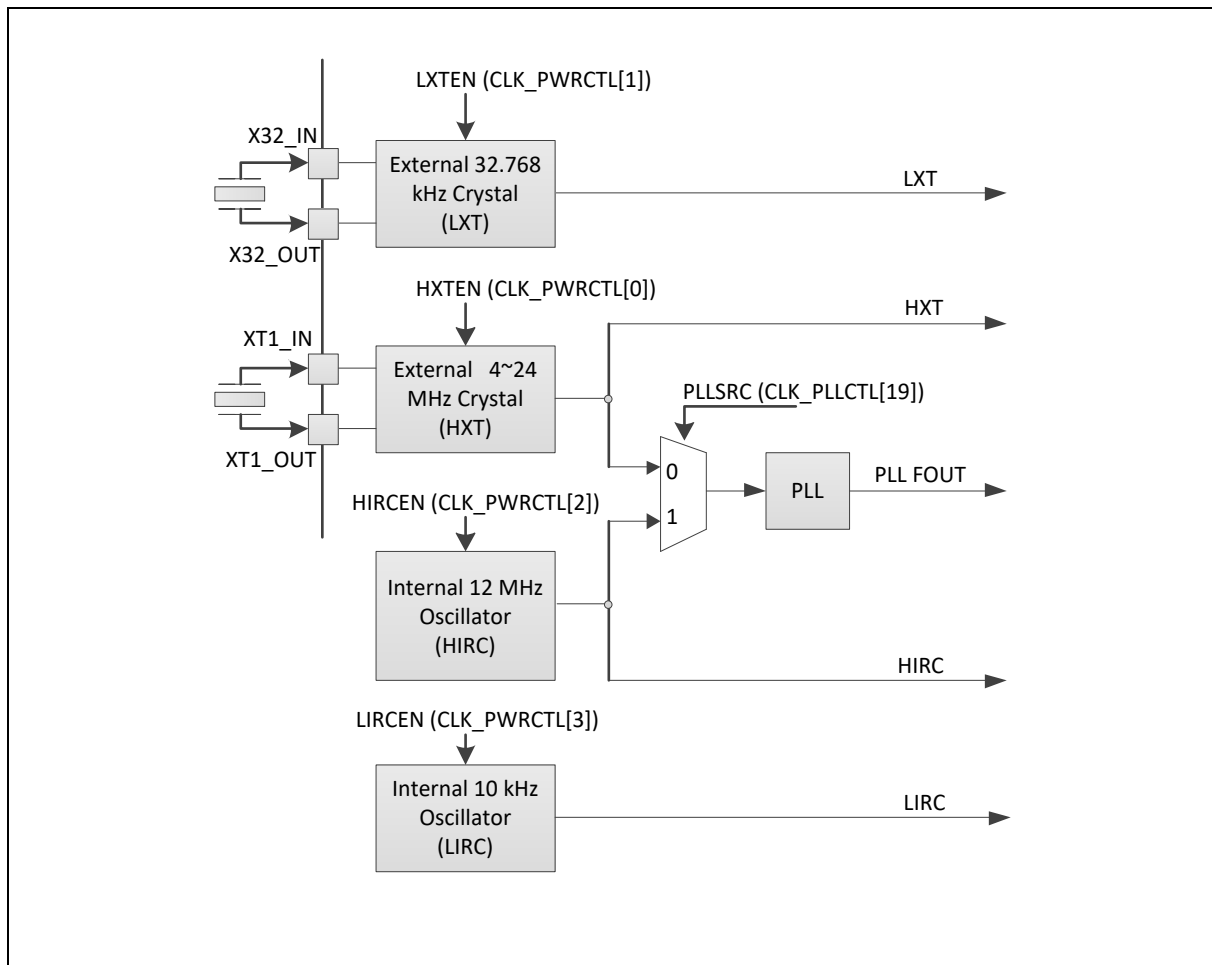


Figure 6-15 Clock Generator Block Diagram

### 6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK\_CLKSEL0[2:0]). The block diagram is shown in Figure 6-16.

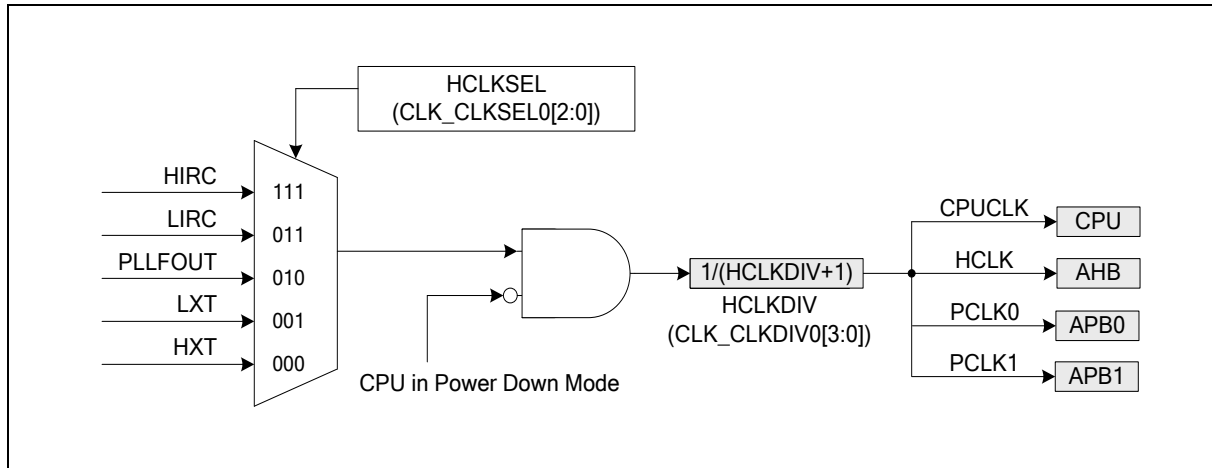


Figure 6-16 System Clock Block Diagrams

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK\_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK\_CLKDCTL[5]) is set to 1. User can try to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

Figure 6-17 shows The HXT clock stops detection and system clock switches to HIRC procedure

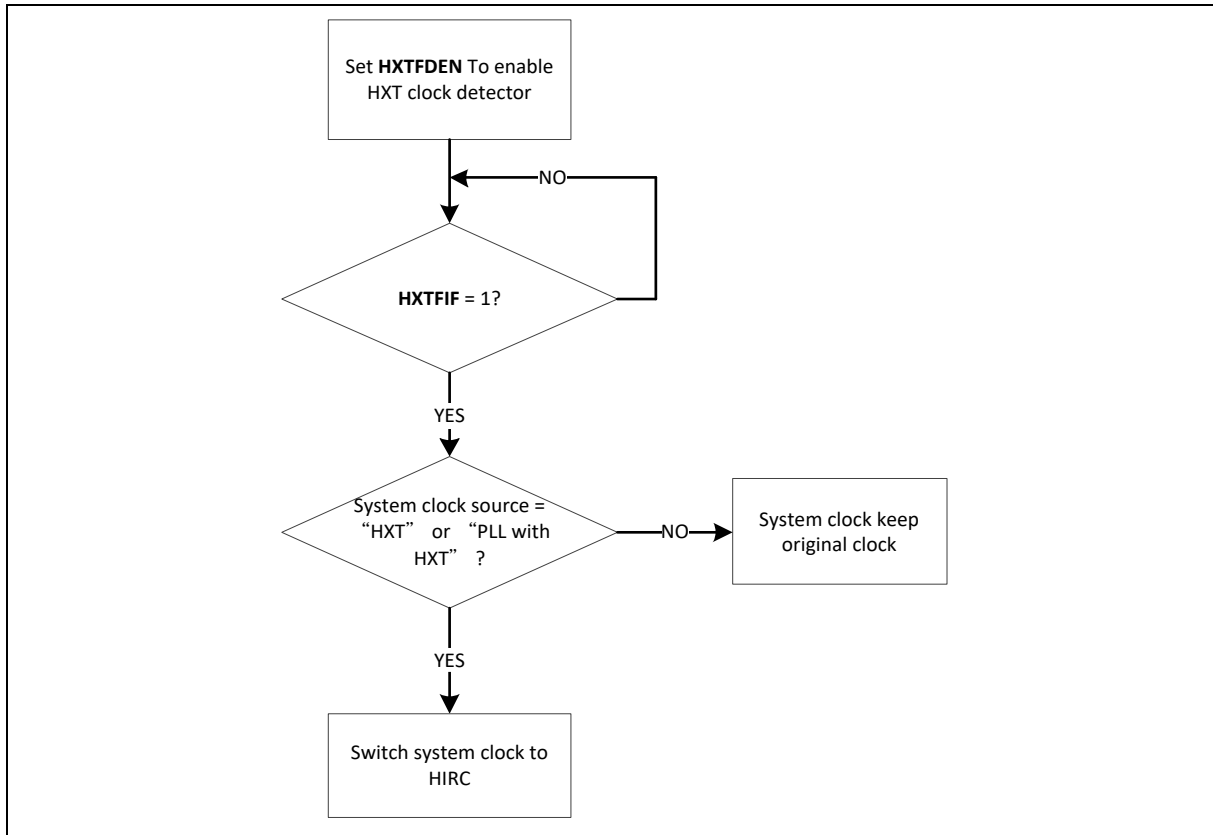


Figure 6-17 HXT Stop Protect Procedure

The clock source of SysTick in Cortex®-M4F core can use CPU clock or external clock (SYST\_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK\_CLKSEL0[5:3]). The block diagram is shown in Figure 6-18.

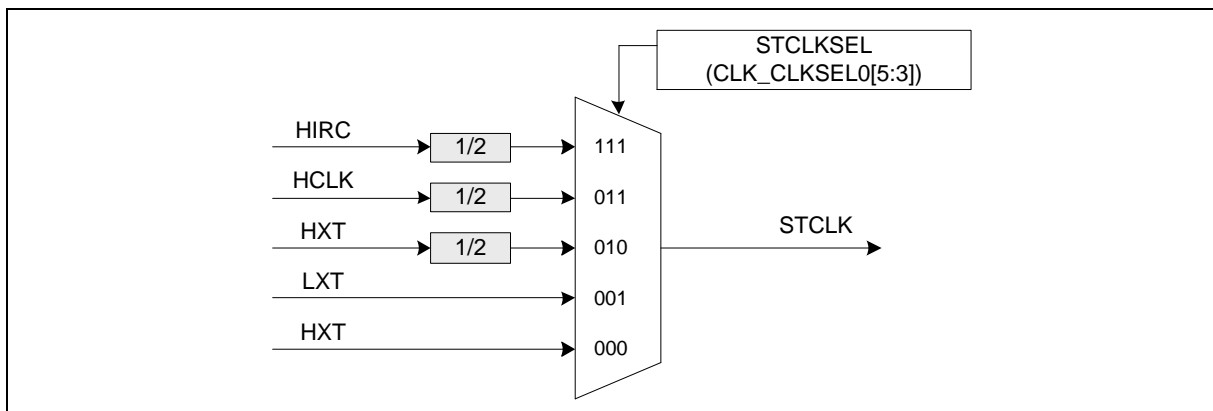


Figure 6-18 SysTick Clock Control Block Diagram

### 6.3.4 Peripherals Clock

Each peripheral clock has its own clock source selection. Refer to the CLK\_CLKSEL1, CLK\_CLKSEL2 and CLK\_CLKSEL3 register.

### 6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For these clocks, which still keep active, are listed below:

- Clock Generator
  - 10 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

### 6.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from  $F_{in}/2^1$  to  $F_{in}/2^{16}$  where  $F_{in}$  is input clock frequency to the clock divider.

The output formula is  $F_{out} = F_{in}/2^{(N+1)}$ , where  $F_{in}$  is the input clock frequency,  $F_{out}$  is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK\_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK\_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK\_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

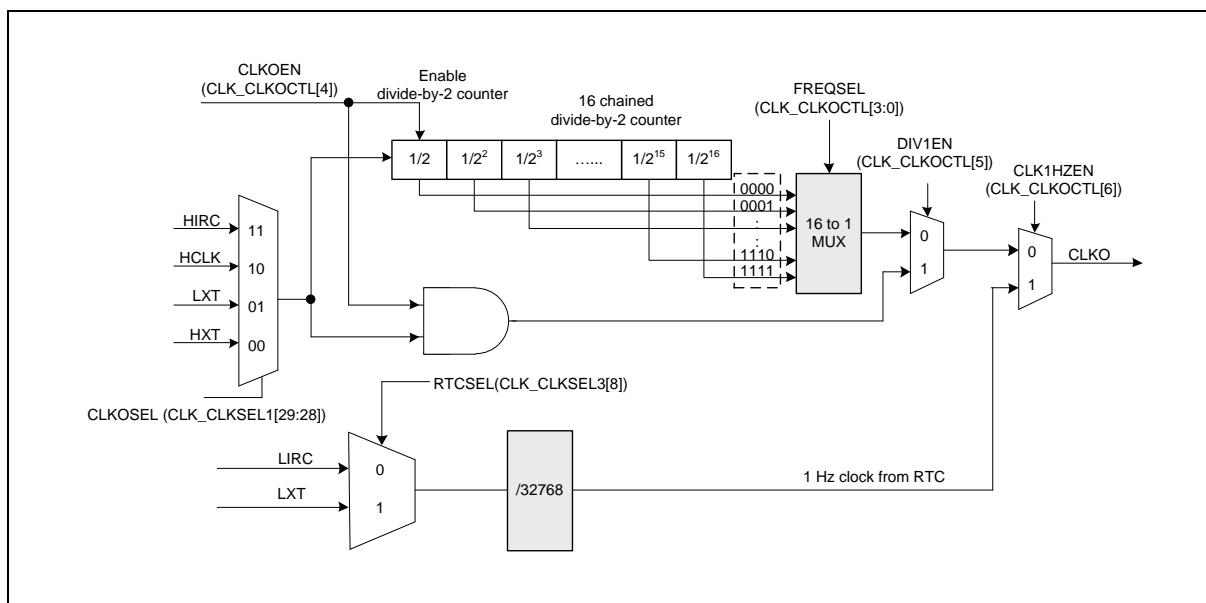


Figure 6-19 Clock Output Block Diagram

6.3.7 USB Clock Source

The clock sources of USB 1.0 and 2.0 systems are generated from external crystal clock 12MHz or programmable PLL output. M48xGC/M48xE8 has a HIRC48M for USB 1.0 system. The generated clocks are shown in Figure 6-20 and Figure 6-21.

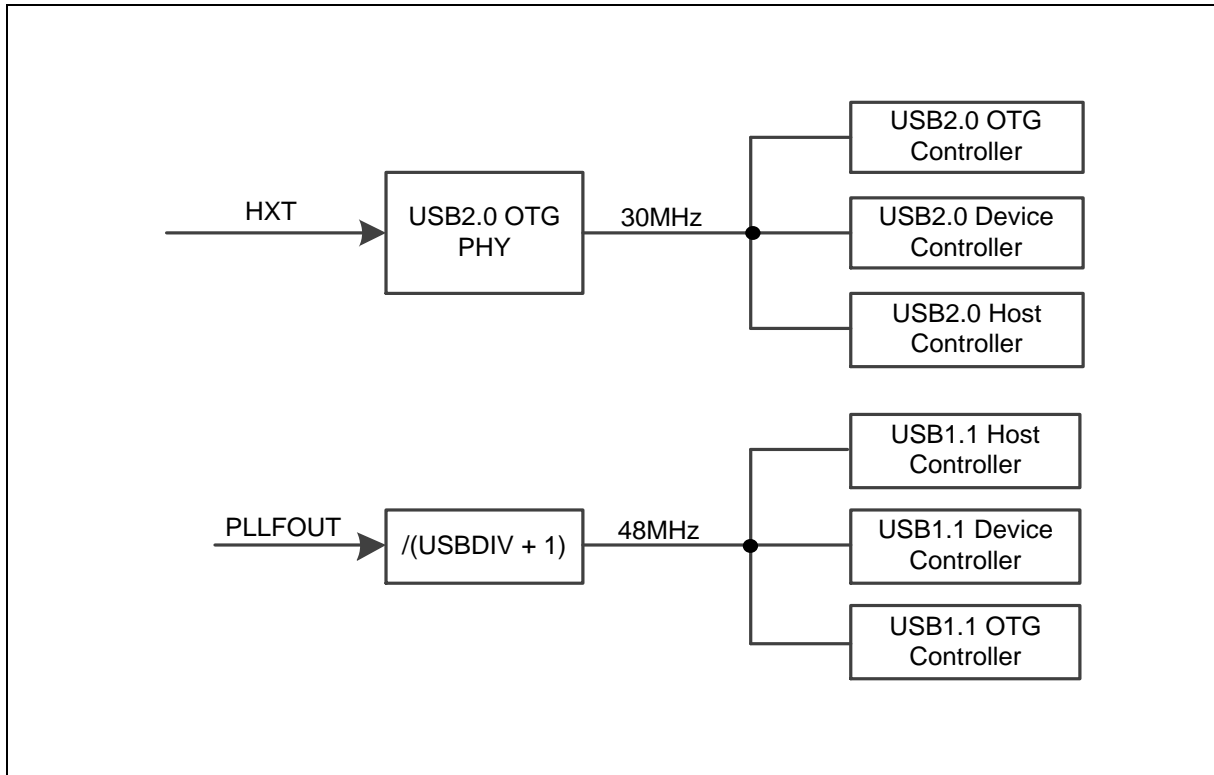


Figure 6-20 USB Clock Source (M48xID/M487KMCAN)

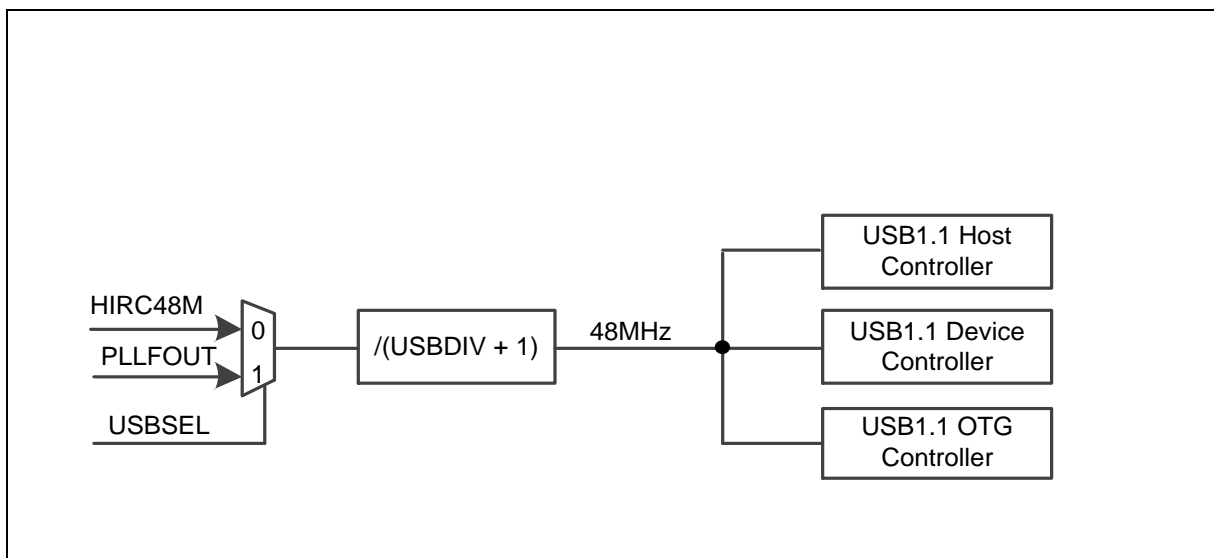


Figure 6-21 USB Clock Source (M48xGC/M48xE8)

## 6.4 True Random Number Generator (TRNG)

### 6.4.1 Overview

The True Random Number Generator (TRNG) is used to generate the randomness by extracting from physical phenomena.

### 6.4.2 Features

- Generates 800 random bits per second



## 6.5 Flash Memory Controller (FMC)

### 6.5.1 Overview

The FMC is equipped with 128/256/512 Kbytes on-chip embedded Flash for application and configurable Data Flash to store some application dependent data. Thus, the total size of application rom (APROM) is 128/256/512 Kbytes. A User Configuration block provides for system initiation. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 4 Kbytes security protection ROM (SPROM) can conceal user program. A 3 Kbytes one-time-program ROM (OTP) is used for recording one-time-program data. A 32 Kbytes Boot Loader consists of native ISP functions and secure boot function. A 8 Kbytes Boot Loader consists of secure boot function. A 4 Kbytes cache with zero wait cycle is used to improve Flash access performance. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

### 6.5.2 Features

- Supports dual-bank Flash macro for safe firmware upgrade
- Supports 128/256 Kbytes application ROM (APROM)
- Supports 512 Kbytes application ROM (APROM)
- Supports 4 Kbytes loader ROM (LDROM)
- Supports 4 Kbytes security protection ROM (SPROM) to conceal user program
- Supports mirror SPROM in dual-bank Flash macro to read SPROM code while writing other ROM
- Supports 4 XOM (eXecution Only Memory) regions to conceal user program in APROM.
- Supports Data Flash with configurable memory size
- Supports 16 bytes User Configuration block to control system initiation
- Supports 3 Kbytes one-time-program ROM (OTP)
- Supports 4 Kbytes page erase for all embedded Flash
- Supports block and bank erase for APROM, except for XOM regions
- Supports Boot Loader with native In-System-Programming (ISP) functions
- Supports Secure Boot function for code integrity and authenticity
- Supports Security Key protection function for APROM, LDROM, SPROM, User Configuration block and KPROM protection
- Supports 32-bit/64-bit and multi-word Flash programming function
- Supports fast Flash programming verification function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory
- Supports cache memory to improve Flash access performance and reduce power consumption

| FMC Features  | M48xID/M487KMCAN | M48xGC/M48xE8 |
|---|------------------|---------------|
| Dual-bank Flash macro                                   | ●                |               |
| 128/256 Kbytes APROM                                    | ●                | ●             |
| 512 Kbytes APROM  | ●                |               |
| 4 Kbytes LDROM  | ●                | ●             |
| 4 Kbytes SPROM  | ●                |               |
| 4 XOM region  |                  | ●             |
| Data Flash with configurable memory size                | ●                | ●             |
| 16 bytes User Configuration block (UCFG)                | ●                | ●             |
| 3 Kbytes OTP  | ●                | ●             |
| 8 Kbytes KPROM  | ●                | ●             |
| 4 Kbytes page erase                                     | ●                | ●             |
| Block and bank erase for APROM, except for XOM          | ●                | ●             |
| 32 Kbytes Boot Loader with native ISP functions         | ●                |               |
| 8 Kbytes Boot Loader with native ISP functions          |                  | ●             |
| AES secure boot function                                | ●                |               |
| ECC secure boot function                                |                  | ●             |
| Security Key protection function for APROM and LDROM    | ●                | ●             |
| Security Key protection function for UCFG and KPROM     | ●                | ●             |
| Security Key protection function for SPROM              | ●                |               |
| 32-bit/64-bit and multi-word Flash programming function | ●                | ●             |
| Fast Flash programming verification function            | ●                | ●             |
| CRC32 checksum calculation function                     | ●                | ●             |
| 4 Kbytes cache memory                                   | ●                | ●             |
| In-Application-Programming function (IAP)               | ●                | ●             |
| Boot from boot loader via PF.0 at reset rising          | ●                |               |

Table 6.5-1 FMC Features Comparison Table at Different Chip

## 6.6 General Purpose I/O (GPIO)

### 6.6.1 Overview

This chip has up to 118 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 118 pins are arranged in 8 ports named as PA, PB, PC, PD, PE, PF, PG and PH. PA, PB, PE and PG has 16 pins on port. PC, PD has 15 pins on port. PF, PH has 12 pins on port. Each of the 118 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]).

### 6.6.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impedance mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- Supports independent pull-up and pull-down control
- Enabling the pin interrupt function will also enable the wake-up function

## 6.7 PDMA Controller (PDMA)

### 6.7.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 16 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

### 6.7.2 Features

- Supports 16 independently configurable channels
- Selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and SPI, UART, DAC, ADC and PWM request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel1
- Supports stride function from channel 0 to channel 5
- Enhanced Stride Function for image processing (M48xGC/M48xE8)

## 6.8 Timer Controller (TMR)

### 6.8.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The timer controller also provides four PWM generators. Each PWM generator supports two PWM output channels in independent mode and complementary mode. The output state of PWM output pin can be control by pin mask, polarity and break control, and dead-time generator.

### 6.8.2 Features

#### 6.8.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx\_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx\_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger EPWM, BPWM, QEI, EADC, DAC and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports internal clock (HIRC, LIRC) and external clock (HXT, LXT) for capture event
- Supports Inter-Timer trigger mode
- Supports event counting source from internal USB SOF signal

### 6.8.2.2 PWM Function Features

- Supports maximum clock frequency up to maximum PCLK
- Supports independent mode for PWM generator with two output channels
- Supports complementary mode for PWM generator with paired PWM output channel
  - 12-bit dead-time insertion with 12-bit prescale
- Supports 12-bit prescale from 1 to 4096
- Supports 16-bit PWM counter
  - Up, down and up-down count operation type
  - One-shot or auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, Brown-out detection, SRAM parity error and CPU lockup)
  - Brake pin noise filter control for brake source
  - Edge detect brake source to control brake state until brake status cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
  - Brake condition happened
- Supports trigger EADC on the following events:
  - PWM zero point, period, zero or period point, up-count compared or down-count compared point events

## 6.9 Watchdog Timer (WDT)

### 6.9.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

### 6.9.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval ( $2^4 \sim 2^{18}$ ) and the time-out interval is 1.6 ms ~ 26.214 s if WDT\_CLK = 10 kHz.
- System kept in reset state for a period of  $(1 / \text{WDT\_CLK}) * 63$
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT\_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as 10 kHz or LXT.

## 6.10 Window Watchdog Timer (WWDT)

### 6.10.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

### 6.10.2 Features

- 6-bit down counter value (CNTDAT, WWDT\_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT\_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT\_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

## 6.11 Real Time Clock (RTC)

### 6.11.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

### 6.11.2 Features

- Supports independent RTC power domain with external power pin  $V_{BAT}$ . (M48xGC/M48xE8)
- Supports real time counter in RTC\_TIME (hour, minute, second) and calendar counter in RTC\_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC\_TALM and RTC\_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC\_TAMSK and RTC\_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC\_CLKFMT register.
- Optional support 1/128 second HZCNT in RTC\_TIME and RTC\_TALM.
- Supports Leap Year indication in RTC\_LEAPYEAR register.
- Supports Day of the Week counter in RTC\_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC\_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports Daylight Saving Time software control in RTC\_DSTCTL.
- Supports up to 6 individual tamper pins.
- Supports 20/80 bytes spare registers and tamper pins detection to clear the content of these spare registers.
- Supports Flash mass erase operate will also clear the 20 bytes spare registers content. (M48xGC/M48xE8)



## 6.12 EPWM Generator and Capture Timer (EPWM)

### 6.12.1 Overview

The chip provides two EPWM generators — EPWM0 and EPWM1. Each EPWM supports 6 channels of EPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit EPWM counter with 16-bit comparator. The EPWM counter supports up, down and up-down counter types. EPWM uses comparator compared with counter to generate events. These events use to generate EPWM pulse, interrupt and trigger signal for EADC/DAC to start conversion.

The EPWM generator supports two standard EPWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various EPWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC. For EPWM output control unit, it supports polarity output, independent pin mask and brake functions.

The EPWM generator also supports input capture function. It supports latch EPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

### 6.12.2 Features

#### 6.12.2.1 EPWM Function Features

- Supports maximum clock frequency up to 192MHz
- Supports up to two EPWM modules, each module provides 6 output channels
- Supports independent mode for EPWM output/Capture input channel
- Supports complementary mode for 3 complementary paired EPWM output channel
  - Dead-time insertion with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution EPWM counter
  - Up, down and up/down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each EPWM pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, SRAM parity error, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed

- Supports interrupt on the following events:
  - EPWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger EADC/DAC on the following events:
  - EPWM counter matches 0, period value or compared value
  - EPWM counter matches free trigger comparator compared value (only for EADC)
  - Supports EPWM trigger EADC event prescaler feature
- Supports EPWM output accumulator stop counter mode (M48xGC/M48xE8)
- Supports Fault Detect function (M48xGC/M48xE8)

6.12.2.2 *Capture Function Features*

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for EPWM all channels

### 6.13 Basic PWM Generator and Capture Timer (BPWM)

#### 6.13.1 Overview

The chip provides two BPWM generators — BPWM0 and BPWM1. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for EADC0/1 to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

#### 6.13.2 Features

##### 6.13.2.1 BPWM Function Features

- Supports maximum clock frequency up to 192MHz.
- Supports up to two BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger EADC0/1 in the following events:
  - BPWM counter matches 0, period value or compared value

##### 6.13.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

|                          | M48xID/M487KMCAN | M48xGC/M48xE8 |
|--------------------------|------------------|---------------|
| Trigger numbers for EADC | 1                | 2             |

Table 6.13-1 BPWM Features Comparison Table

## 6.14 Quadrature Encoder Interface (QEI)

### 6.14.1 Overview

There are two QEI controllers in this device. The Quadrature Encoder Interface (QEI) decodes speed of rotation and motion sensor information. It can be used in any application that uses a quadrature encoder for feedback.

### 6.14.2 Features

#### 6.14.2.1 Quadrature Encoder Interface (QEI) Features

- Up to two QEI controllers, QEI0 and QEI1.
- Two QEI phase inputs, QEA and QEB; One Index input.
- A 32-bit up/down Quadrature Encoder Pulse Counter (QEI\_CNT)
- A 32-bit software-latch Quadrature Encoder Pulse Counter Hold Register (QEI\_CNTHOLD)
- A 32-bit Quadrature Encoder Pulse Counter Index Latch Register (QEI\_CNTLATCH)
- A 32-bit Quadrature Encoder Pulse Counter Compare Register (QEI\_CNTCMP) with a Pre-set Maximum Count Register (QEI\_CNTMAX)
- One QEI control register (QEI\_CTL) and one QEI Status Register (QEI\_STATUS)
- Four Quadrature encoder pulse counter operation modes
  - Support x4 free-counting mode
  - Support x2 free-counting mode
  - Support x4 compare-counting mode
  - Support x2 compare-counting mode
- Encoder Pulse Width measurement mode
- Input frequency of QEA/QEB/IDX without noise filter must lower than PCLK/4
- Input frequency of QEA/QEB/IDX with noise filter must lower than Noise Filter Clk/8

## 6.15 Enhanced Input Capture Timer (ECAP)

### 6.15.1 Overview

The chip provides up to two units of Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

### 6.15.2 Features

- Up to two Input Capture Timer/Counter units, CAP0 and CAP1.
- Each unit has 3 input channels.
- Each unit has its own interrupt vector.
- Each input channel has its own capture counter hold register.
- 24-bit Input Capture up-counting timer/counter.
- With noise filter in front end of input ports.
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Captured events reset and/or reload capture counter.
- Supports compare-match function.

## 6.16 UART Interface Controller (UART)

### 6.16.1 Overview

The chip provides three channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, LIN, RS-485 and Single-wire function modes and auto-baud rate measuring function.

### 6.16.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (UART\_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - 9600 bps for UART\_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection
  - Programmable STOP bit, 1, 1.5, or 2 STOP bit generation
- Supports IrDA SIR function mode
  - 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0/UART1 with LIN function)
  - LIN master/slave mode
  - Programmable break generation function for transmitter
  - Break detection function for receiver
- Supports RS-485 function mode
  - RS-485 9-bit mode
  - Hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function
- Supports Single-wire function mode.

| UART Feature                                 | UART0/UART1     | UART2 ~ UART7   | SC_UART         | USCI-UART              |
|--|-----------------|-----------------|-----------------|------------------------|
| FIFO   | 16 Bytes        | 16 Bytes        | 4 Bytes         | TX: 1byte<br>RX: 2byte |
| Auto Flow Control (CTS/RTS)                  | √               | √               | -               | √                      |
| IrDA   | √               | √               | -               | -                      |
| LIN  | √               | -               | -               | -                      |
| RS-485 Function Mode                         | √               | √               | -               | √                      |
| nCTS Wake-up                                 | √               | √               | -               | √                      |
| Imcoming Data Wake-up                        | √               | √               | -               | √                      |
| Received Data FIFO reached threshold Wake-up | √               | √               | -               | -                      |
| RS-485 Address Match (AAD mode) Wake-up      | √               | √               | -               | -                      |
| Auto-Baud Rate Measurement                   | √               | √               | -               | √                      |
| STOP bit Length                              | 1, 1.5, 2 bit   | 1, 1.5, 2 bit   | 1, 2 bit        | 1, 2 bit               |
| Word Length                                  | 5, 6, 7, 8 bits | 5, 6, 7, 8 bits | 5, 6, 7, 8 bits | 6~13 bits              |
| Even / Odd Parity                            | √               | √               | √               | √                      |
| Stick Bit                                    | √               | √               | -               | -                      |
| <b>Note:</b> √= Supported                    |                 |                 |                 |                        |

Table 6.16-1 M480 Series UART Features

## 6.17 Ethernet MAC Controller (EMAC)

### 6.17.1 Overview

This chip provides an Ethernet MAC Controller (EMAC) for Network application. The Ethernet MAC controller consists of IEEE 802.3/Ethernet protocol engine with internal CAM function for recognizing Ethernet MAC addresses, Transmit-FIFO, Receive-FIFO, TX/RX state machine controller, time stamping engine for IEEE 1588, Magic Packet parsing engine and status controller. The EMAC supports both the MII and RMI (Reduced MII) interface to connect with external Ethernet PHY.

### 6.17.2 Features

- Supports IEEE Std. 802.3 CSMA/CD protocol
- Supports Ethernet frame time stamping for IEEE Std. 1588 – 2002 protocol
- Supports both half and full duplex for 10 Mbps or 100 Mbps operation
- Supports RMI interface
- Supports MII Management function to control external Ethernet PHY
- Supports pause and remote pause function for flow control
- Supports long frame (more than 1518 bytes) and short frame (less than 64 bytes) reception
- Supports 16 entries CAM function for Ethernet MAC address recognition
- Supports Magic Packet recognition to wake system up from Power-down mode
- Supports 256 bytes transmit FIFO and 256 bytes receive FIFO
- Supports DMA function



## 6.18 Smart Card Host Interface (SC)

### 6.18.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal. It can also be set as UART mode to communicate with other device.

### 6.18.2 Features

- ISO 7816-3 T = 0, T = 1 compliant
- EMV2000 compliant
- Three ISO 7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- One 24-bit timer and two 8-bit timers for Answer to Request (ATR) and waiting times processing
- Supports auto direct / inverse convention function
- Supports transmitter and receiver error retry and error number limiting function
- Supports hardware activation sequence process, and the time between PWR on and CLK start is configurable
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detected the card removal
- Supports UART mode
  - Full duplex, asynchronous communications
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads
  - Supports programmable baud rate generator
  - Supports programmable receiver buffer trigger level
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SCn\_EGT[7:0])
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1- or 2- stop bit generation

## 6.19 I<sup>2</sup>S Controller (I<sup>2</sup>S)

### 6.19.1 Overview

The I<sup>2</sup>S controller consists of I<sup>2</sup>S protocol to interface with external audio CODEC. Two 16-level depth FIFO for reading path and writing path respectively are capable of handling 8/16/24/32 bits audio data sizes. A PDMA controller handles the data movement between FIFO and memory.

### 6.19.2 Features

- Supports Master mode and Slave mode
- Capable of handling 8, 16, 24 and 32 bits data sizes in each audio channel
- Supports monaural and stereo audio data
- Supports I<sup>2</sup>S protocols: Philips standard, MSB-justified, and LSB-justified data format
- Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
- PCM protocol supports TDM multi-channel transmission in one audio sample, and the number of data channel can be set as 2, 4, 6, or 8
- Provides two 16-level FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports two PDMA requests, one for transmitting and the other for receiving

## 6.20 Serial Peripheral Interface (SPI)

### 6.20.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. Each SPI controller also supports I<sup>2</sup>S mode to connect external audio CODEC.

### 6.20.2 Features

- SPI Mode
  - Up to four sets of SPI controllers
  - Supports Master or Slave mode operation
  - Master mode up to 96 MHz (when chip works at  $V_{DD} = 2.7\sim 3.6V$ )
  - Slave mode up to 96 MHz when SPI master device supports adjustment function of RX data sampling clock (when chip works at  $V_{DD} = 2.7\sim 3.6V$ )
  - Slave mode up to 48 MHz when SPI master device does not support adjustment function of RX data sampling clock (when chip works at  $V_{DD} = 2.7\sim 3.6V$ )
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I<sup>2</sup>S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I<sup>2</sup>S and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

## 6.21 Quad Serial Peripheral Interface (QSPI)

### 6.21.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode and the controller supports the PDMA function to access the data buffer.

### 6.21.2 Features

- Supports Master or Slave mode operation
- Master mode up to 96 MHz (when chip works at  $V_{DD} = 2.7V\sim 3.6V$ )
- Slave mode up to 96 MHz when SPI master device supports adjustment function of RX data sampling clock (when chip works at  $V_{DD} = 2.7V\sim 3.6V$ )
- Slave mode up to 48 MHz when SPI master device does not support adjustment function of RX data sampling clock (when chip works at  $V_{DD} = 2.7V\sim 3.6V$ )
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports Transmit Double Transfer Rate Mode (TX DTR mode)
- Supports receive-only mode

## 6.22 SPI Synchronous Serial Interface Controller (SPI Master mode)

### 6.22.1 Overview

The SPI Synchronous serial Interface Controller for SPI master mode performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data received from MCU. This SPI controller can drive one external peripheral (External SPI Flash) and it is seen as the SPI master mode. It can generate an interrupt signal when data transfer is finished and can be cleared by writing 1 to the interrupt flag. The active level of device/slave select signal can be chosen to low active or high active, which depends on the peripheral. Writing a divisor into the SPIM\_CTL1 register can program the frequency of serial clock output to the peripheral.

In SPI Flash controller, normal I/O mode contains four 32-bit transmit/receive buffers, and can provide 1 to 4 burst mode operation. The number of bits in each transaction can be 8, 16, 24, or 32; data can be transmitted/received up to four successive transactions in one transfer.

By DMA write mode, user can move data from SRAM to external SPI Flash component. In DMA read mode, user can move data from external SPI Flash component to SRAM. In direct memory mapping mode (DMM mode), this SPI Flash controller will translate the AHB bus commands into SPI Flash operations without MCU setting related SPI Flash command. Therefore users can access external SPI Flash as a ROM module.

In direct memory mapping mode with cache off mode, it will pre-fetch 4-word Flash data after a direct memory mapping access. when using direct memory mapping mode with cache on mode, it will use 32 Kbytes cache memory to reduce the number of accessing external SPI Flash component and the performance of SPI Flash access can be improved. To improve the read operation of SPI Flash without increasing the serial clock frequency, this SPI Flash controller supports DTR/DDR (Double Transfer Rate/Double Data Rate) read command codes that support Standard/Dual/Quad SPI modes. The one byte command code is still latched into the device on the rising edge of the serial clock similar to all other SPI commands. Once a DTR/DDR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

In core coupled memory mode (CCM mode), the cache function is disabled by hardware automatically, and MCU can access this 32 Kbytes cache memory as general SRAM. For data protection, this SPI Flash controller supports cipher encryption and decryption circuits to protect data which user places into external SPI Flash when DMA read/write mode and direct memory mapping mode are used.

### 6.22.2 Features

- Supports maximum 32 Mbytes SPI Flash size
- Supports SPI master mode
- Supports Direct Memory Mapping Mode and Normal I/O Mode
- Supports 8/16/24/32 bits transaction for Normal I/O mode
- Provides burst mode operation in Normal I/O mode, which can transmit/receive data up to four successive transactions in one transfer
- Supports DMA mode read/write
- Supports standard (1-bit), dual (2-bit), and quad (4-bit) I/O transfer mode
- Supports Double Transfer Rate (DTR) / Double Data Rate (DDR) transfer mode
- Supports 32 Kbytes cache memory
- Supports 32 Kbytes Core Coupled Memory (CCM) when cache function disable
- Supports Cipher encryption/decryption
- One slave/device select line for external SPI Flash component

## 6.23 I<sup>2</sup>C Serial Interface Controller (I<sup>2</sup>C)

### 6.23.1 Overview

I<sup>2</sup>C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I<sup>2</sup>C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I<sup>2</sup>C controllers which support Power-down wake-up function.

### 6.23.2 Features

The I<sup>2</sup>C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I<sup>2</sup>C bus include:

- Supports up to three I<sup>2</sup>C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports High speed mode 3.4Mbps
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I<sup>2</sup>C interrupt if the I<sup>2</sup>C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition ( four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports setup/hold time programmable
- Supports Bus Management (SM/PM compatible) function

## 6.24 USCI - Universal Serial Control Interface Controller (USCI)

### 6.24.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I<sup>2</sup>C functional protocol.

### 6.24.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I<sup>2</sup>C

## 6.25 USCI – UART Mode

### 6.25.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter are independent, and the transmission and reception can be started separately.

The UART controller also provides auto flow control. There are three conditions to wake up the system.

### 6.25.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA transfer
- Supports Wake-up function (Incoming Data and nCTS Wakeup Only)

## 6.26 USCI - SPI Mode

### 6.26.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI\_CTL[2:0]) = 0x1

This SPI protocol can operate as master or Slave mode by setting the SLAVE (USPI\_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown below.

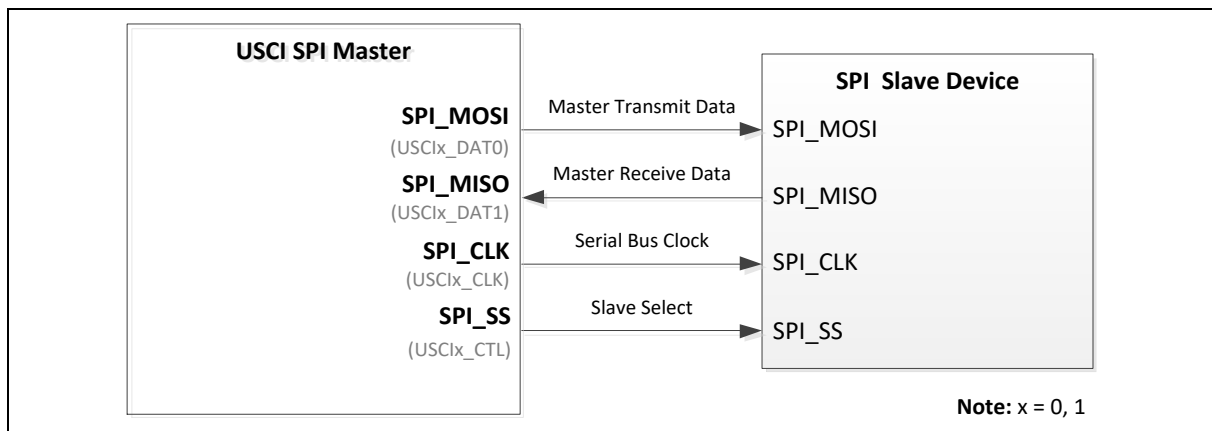


Figure 6-22 SPI Master Mode Application Block Diagram

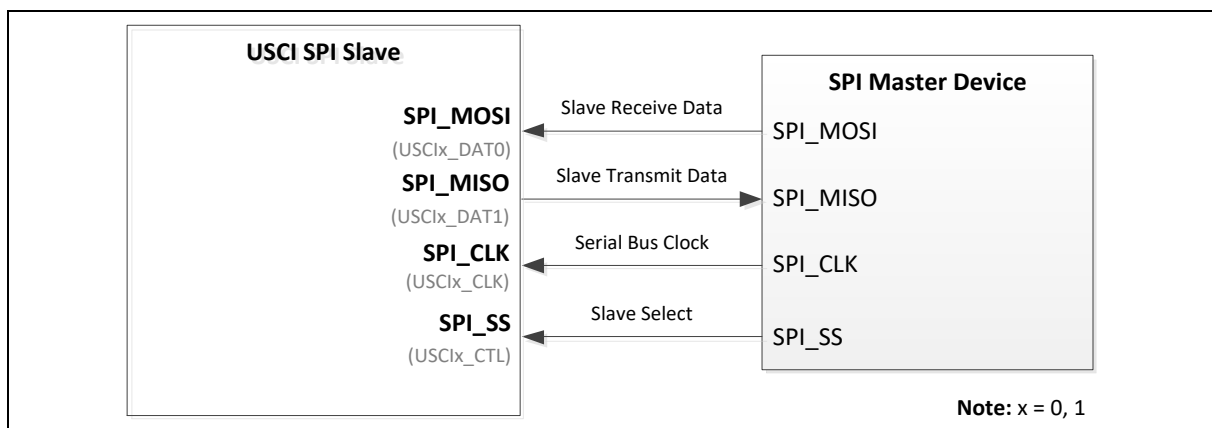


Figure 6-23 SPI Slave Mode Application Block Diagram



### 6.26.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master =  $f_{PCLK} / 2$ , Slave <  $f_{PCLK} / 5$ )
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

## 6.27 USCI - I<sup>2</sup>C Mode

### 6.27.1 Overview

On I<sup>2</sup>C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6-24 for more detailed I<sup>2</sup>C BUS Timing.

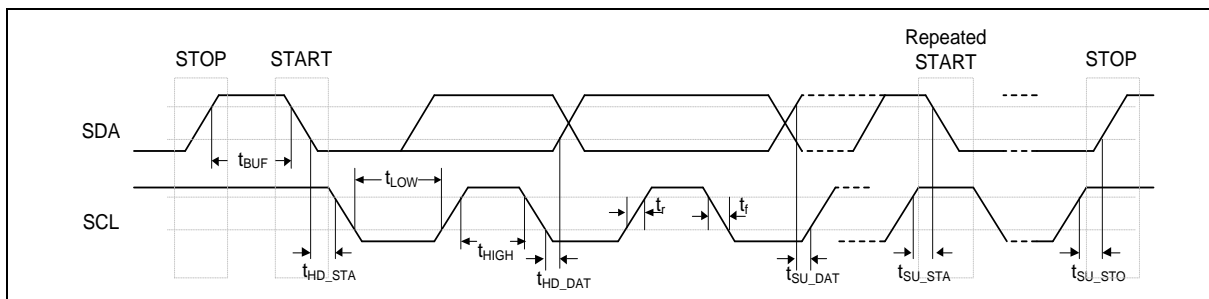


Figure 6-24 I<sup>2</sup>C Bus Timing

The device's on-chip I<sup>2</sup>C provides the serial interface that meets the I<sup>2</sup>C bus standard mode specification. The I<sup>2</sup>C port handles byte transfers autonomously. The I<sup>2</sup>C mode is selected by FUNMODE (UI2C\_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I<sup>2</sup>C bus via two pins: SDA and SCL. When I/O pins are used as I<sup>2</sup>C ports, user must set the pins function to I<sup>2</sup>C in advance.

**Note:** Pull-up resistor is needed for I<sup>2</sup>C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I<sup>2</sup>C operation mode.

### 6.27.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by START signal or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

## 6.28 Controller Area Network (CAN)

### 6.28.1 Overview

The C\_CAN consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface. The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1 Mbps. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C\_CAN can be accessed directly by the software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

### 6.28.2 Features

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 Mbps
- 32 Message Objects
- Each Message Object has its own identifier mask
- Programmable FIFO mode (concatenation of Message Objects)
- Maskable interrupt
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation
- 16-bit module interfaces to the AMBA APB bus
- Supports wake-up function

## 6.29 Secure Digital Host Controller (SDH)

### 6.29.1 Overview

The Secure Digital Host Controller (SD Host) has DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD/SDHC. The SDHOST controller can support SD/SDHC and cooperated with DMAC to provide a fast data transfer between system memory and cards.

### 6.29.2 Features

- AMBA AHB master/slave interface compatible, for data transfer and register read/write.
- Supports single DMA channel.
- Supports hardware Scatter-Gather function.
- Using single 128 Bytes shared buffer for data exchange between system memory and cards.
- Synchronous design for DMA with single clock domain, AHB bus clock (HCLK).
- Interface with DMAC for register read/write and data transfer.
- Supports SD/SDHC card.
- Completely asynchronous design for Secure Digital with two clock domains, HCLK and Engine clock, note that frequency of HCLK should be higher than the frequency of peripheral clock.
- 

|                                 | M48xID/M487KMCAN | M48xGC/M48xE8 |
|---------------------------------|------------------|---------------|
| Secure Digital Host Controllers | 2                | 1             |

Table 6.29-1 SDH Features Comparison Table

## 6.30 External Bus Interface (EBI)

### 6.30.1 Overview

This chip is equipped with an external bus interface (EBI) for external device use. To save the connections between an external device and a chip, EBI is operating at address bus and data bus multiplex mode. The EBI supports three chip selects that can connect three external devices with different timing setting requirements.

### 6.30.2 Features

- Supports up to three memory banks
- Supports dedicated external chip select pin with polarity control for each bank
- Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
- Supports 8-/16-bit data width
- Supports byte write in nresetdata width mode
- Supports Address/Data multiplexed Mode
- Supports Timing parameters individual adjustment for each memory block
- Supports LCD interface i80 mode
- Supports PDMA mode
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)
- Supports address bus and data bus separate mode

## 6.31 USB 1.1 Device Controller (USBD)

### 6.31.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/ isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1 Kbytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD\_BUFSEGx).

There are 12 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of "Endpoint Control" is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the no-event-wake-up, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD\_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USBD\_EPSTS0 and USBD\_EPSTS1) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD\_SE0), the USB controller will force the output of USB\_D+ and USB\_D- to level low and its function is disabled. After disable the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1*.

### 6.31.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 5 different interrupt events (SOF, NEVWK, VBUSDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Supports 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1 Kbyte buffer size
- Provides remote wake-up capability

## 6.32 High Speed USB 2.0 Device Controller (HSUSBD)

### 6.32.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is compliant with USB 2.0 specification and it contains 12 configurable endpoints in addition to control endpoint. These endpoints could be configured to BULK, INTERRUPT or ISO. The USB device controller has a built-in DMA to relieve the load of CPU.

### 6.32.2 Features

- USB Specification reversion 2.0 compliant
- Supports 12 configurable endpoints in addition to Control Endpoint
- Each of the endpoints can be Isochronous, Bulk or Interrupt and either IN or OUT direction
- Three different operation modes of an in-endpoint – Auto Validation mode, Manual Validation mode, Fly mode
- Supports DMA operation
- 4092 Bytes Configurable RAM used as endpoint buffer
- Supports Endpoint Maximum Packet Size up to 1024 bytes

## 6.33 USB 1.1 Host Controller (USBH)

### 6.33.1 Overview

This chip is equipped with a USB 1.1 Host Controller (USBH) that supports Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port over current detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting over current of attached USB devices.

### 6.33.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 1.1.
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports both full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt and Isochronous transfers.
- Supports an integrated Root Hub.
- Supports a USB host port shared with USB device (OTG function).
- Supports port power control and port over current detection.
- Supports DMA for real-time data transfer.



## 6.34 USB 2.0 Host Controller (USBH)

### 6.34.1 Overview

This chip is equipped with a USB 2.0 HS/FS Host Controller (USBH) that supports Enhanced Host Controller Interface (EHCI) and Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port over current detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting over current of attached USB devices.

### 6.34.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 2.0.
- Supports Enhanced Host Controller Interface (EHCI) Specification Revision 1.0
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers.
- Supports an integrated Root Hub.
- Supports a port routing logic to route full/low speed device to OHCI controller.
- Supports two USB host port shared with USB device (OTG function).
- Supports port power control and port over current detection.
- Supports DMA for real-time data transfer.

## 6.35 USB On-The-Go (OTG)

### 6.35.1 Overview

The OTG controller interfaces to USB PHY and USB controllers which consist of a USB 1.1 host controller and a USB 2.0 FS device controller. The OTG controller supports HNP and SRP protocols defined in the “On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 2.0 Specification”.

USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID-dependent or OTG Device mode defined in USBROLE (SYS\_USBPHY[1:0]). In Host-only mode, USB frame acts as USB host. USB frame can support both full-speed and low-speed transfer. In Device-only mode, USB frame acts as USB device. USB frame only supports full-speed transfer. In ID-dependent mode, USB frame can be USB Host or USB device depending on USB\_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. USB frame only supports full-speed transfer when OTG device acts as a peripheral.

### 6.35.2 Features

- Built-in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID-dependent: The role of USB frame is only dependent on USB\_ID pin value--as USB Host (USB\_ID pin is low) or USB Device (USB\_ID pin is high). Not support HNP or SRP protocol.
  - OTG device: dependent on USB\_ID pin status to be A-device (USB\_ID pin is low) or B-device (USB\_ID pin is high). Support HNP and SRP protocols.

## 6.36 High Speed USB On-The-Go (HSOTG)

### 6.36.1 Overview

The HSOTG controller interfaces to USB PHY and USB controllers which consist of a USB 2.0 host controller and a USB 2.0 HS device controller. The OTG controller supports HNP and SRP protocols defined in the “On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 1.3 Specification”.

USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID-dependent or OTG Device mode defined in HSUSBROLE (SYS\_USBPHY[17:16]). In Host-only mode, USB frame acts as USB host. USB frame can support high-speed, full-speed and low-speed transfer. In Device-only mode, USB frame acts as USB device. USB frame supports high-speed and full-speed transfer. In ID-dependent mode, USB frame can be USB Host or USB device depends on USB\_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. USB frame supports high-speed and full-speed transfer when OTG device acts as a peripheral.

### 6.36.2 Features

- Built in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID-dependent: The role of USB frame is only dependent on USB\_ID pin value--as USB Host (USB\_ID pin is low) or USB Device (USB\_ID pin is high). Not support HNP or SRP protocol.
  - OTG device: dependent on USB\_ID pin status to be A-device (USB\_ID pin is low) or B-device (USB\_ID pin is high). Support HNP and SRP protocols.

## 6.37 CRC Controller (CRC)

### 6.37.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

### 6.37.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT:  $X^{16} + X^{12} + X^5 + 1$
  - CRC-8:  $X^8 + X^2 + X + 1$
  - CRC-16:  $X^{16} + X^{15} + X^2 + 1$
  - CRC-32:  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

## 6.38 Cryptographic Accelerator (CRYPTO)

### 6.38.1 Overview

The Crypto (Cryptographic Accelerator) includes a secure pseudo random number generator (PRNG) core and supports AES, DES/TDES, SHA, HMAC and ECC algorithms.

The PRNG core supports 64 bits, 128 bits, 192 bits, and 256 bits random number generation.

The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode.

The DES/TDES accelerator is an implementation fully compliant with the DES and Triple DES encryption/decryption algorithm. The DES/TDES accelerator supports ECB, CBC, CFB, OFB, and CTR mode.

The SHA accelerator is an implementation fully compliant with the SHA-160, SHA-224, SHA-256, SHA-384 and SHA-512 and corresponding HMAC algorithms.

The ECC accelerator is an implementation fully compliant with elliptic curve cryptography by using polynomial basis in binary field and prime field.

### 6.38.2 Features

- PRNG
  - Supports 64 bits, 128 bits, 192 bits, and 256 bits random number generation
- AES
  - Supports FIPS NIST 197
  - Supports SP800-38A and addendum
  - Supports 128, 192, and 256 bits key
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode
  - Supports key expander
- DES
  - Supports FIPS 46-3
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, and CTR mode
- TDES
  - Supports FIPS NIST 800-67
  - Implemented according to the X9.52 standard
  - Supports two keys or three keys mode
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, and CTR mode
- SHA
  - Supports FIPS NIST 180, 180-2
  - Supports SHA-160, SHA-224, SHA-256, SHA-384 and SHA-512

- HMAC
  - Supports FIPS NIST 180, 180-2
  - Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384 and HMAC-SHA-512
- ECC
  - Supports both prime field GF(p) and binary field GF(2<sup>m</sup>)
  - Supports NIST P-192, P-224, P-256, P-384 and P-521
  - Supports NIST B-163, B-233, B-283, B-409 and B-571
  - Supports NIST K-163, K-233, K-283, K-409 and K-571
  - Supports point multiplication, addition and doubling operations in GF(p) and GF(2<sup>m</sup>)
  - Supports modulus division, multiplication, addition and subtraction operations in GF(p)

| Engine   | Mode                           | M48xID/M487KMCAN | M48xGC/M48xE8 |
|----------|--------------------------------|------------------|---------------|
| PRNG     |                                | ●                | ●             |
| AES      |                                | ●                | ●             |
| DES/TDES |                                | ●                |               |
| SHA/HMAC | SHA-160                        | ●                |               |
|          | SHA-224                        | ●                |               |
|          | SHA-256                        | ●                |               |
|          | SHA-384                        | ●                |               |
|          | SHA-512                        | ●                |               |
| ECC      | P-192/224/256                  | ●                |               |
|          | P-384/521                      | ●                |               |
|          | B-163/233                      | ●                |               |
|          | B-283/409/571                  | ●                |               |
|          | K-163/233                      | ●                |               |
|          | K-283/409/571                  | ●                |               |
|          | Curve25519                     |                  |               |
|          | Side-channel attack protection |                  |               |

Table 6.38-1 Crypto Features Comparison Table at Different Chip

## 6.39 Camera Capture Interface Controller (CCAP)

### 6.39.1 Overview

The camera capture interface controller (CCAP) is designed to capture image data from a sensor. After capturing or fetching image data, it processes the image data. Then, the embedded DMA controller will move the data from the internal FIFO to system memory with AHB bus.

### 6.39.2 Features

- CCIR601 & CCIR656 & 4-bit interfaces supported for connection to CMOS image sensor
- YUV422 and RGB565 color format supported for data-in from CMOS sensor
- YUV422, RGB565, RGB555 and Y-only color supported for packet data output.
- Single interrupt source to interrupt controller from maskable interrupt source: Address Match, Bus Master Transfer Error, Video Frame End
- Embedded DMA controller supported to transfer data from internal FIFO to system memory through AHB bus
- CROP function supported to crop input image to the required size for digital application.
- Frame rate scaling-down supported
- Image scaling-down supported
- Bit luma output with 8-bit threshold setting supported.

## 6.40 Enhanced 12-bit Analog-to-Digital Converter (EADC)

### 6.40.1 Overview

The chip contains one or two 12-bit successive approximation analog-to-digital converter (SAR EADC converter) with 16 external input channels and 3 internal channels. The EADC0/1 converter can be started by software trigger, EPWM0/1 triggers, BPWM0/1 triggers, timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC (End of conversion) pulse trigger and external pin (EADC0/1\_ST) input signal.

### 6.40.2 Features

- Analog input voltage range: 0~  $V_{REF}$  (Max to 3.6V)
- Reference voltage from  $V_{REF}$  pin.
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 16 single-end analog external input channels or 8 pair differential analog input channels
- Up to 3 internal channels, they are band-gap voltage ( $V_{BG}$ ), temperature sensor ( $V_{TEMP}$ ), and Battery power ( $V_{BAT}$ )
- Four EADC interrupts (ADINT0~3) with individual interrupt vector addresses for each EADC
- Maximum EADC clock frequency is 72 MHz for each EADC
- Up to 5.14 MSPS conversion rate for each EADC at the same time
- Configurable EADC internal sampling time for each EADC
- 12-bit, 10-bit, 8-bit, 6-bit configurable resolution for each EADC
- Supports calibration and load calibration words capability for each EADC
- Supports internal reference voltage  $V_{REF}$ : 1.6V, 2.0V, 2.5V, and 3.0V.
- Supports three power saving modes:
  - Deep Power-down mode
  - Power-down mode
  - Standby mode
- Up to 19 sample modules
  - Each of sample modules which is configurable for EADC converter channel (EADC0/1\_CH0~15) and trigger source for each EADC
  - Sample module 16~18 is fixed for EADC0channel 16, 17, 18 input sources as band-gap voltage, temperature sensor, and battery power ( $V_{BAT}$ )
  - Double buffer for sample control logic module 0~3
  - Configurable sampling time for each sample module
  - Conversion results are held in 19 data registers with valid and overrun indicators



- Any EADC conversion of each EADC can be started by:
  - Write 1 to SWTRGn (EADC0/1\_SWTRG[n], n = 0~18)
  - External pin EADC0/1\_ST
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - EPWM/BPWM triggers
- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

|                | M48xID/M487KMCAN | M48xGC/M48xE8 |
|----------------|------------------|---------------|
| Number of EADC | 1                | 2             |

Table 6.40-1 EADC Features Comparison Table

## 6.41 Digital to Analog Converter (DAC)

### 6.41.1 Overview

The DAC module is a 12-bit, voltage output digital-to-analog converter. It can be configured to 12- or 8-bit output mode and can be used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impedance and drive external loads directly without having to add an external operational amplifier.

### 6.41.2 Features

- Analog output voltage range: 0~AV<sub>DD</sub>.
- Supports 12- or 8-bit output mode.
- Rail to rail settle time 6 $\mu$ s.
- Supports up to two 12-bit 1 MSPS voltage type DAC.
- Reference voltage from internal reference voltage (INT\_VREF), V<sub>REF</sub> pin.
- DAC maximum conversion updating rate 1 MSPS.
- Supports voltage output buffer mode and bypass voltage output buffer mode.
- Supports software and hardware trigger, including Timer0~3, EPWM0, EPWM1, and external trigger pin to start DAC conversion.
- Supports PDMA mode.
- Supports group mode of synchronized update capability for two DACs.

## 6.42 Analog Comparator Controller (ACMP)

### 6.42.1 Overview

The chip provides two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

### 6.42.2 Features

- Analog input voltage range: 0 ~ AV<sub>DD</sub> (voltage of AV<sub>DD</sub> pin)
- Up to two rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV, 10mV, 20mV and 30mV
- Supports wake-up function
- Supports programmable propagation speed and low power consumption
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ◆ ACMP0\_P0, ACMP0\_P1, ACMP0\_P2, or ACMP0\_P3
  - 4 negative sources:
    - ◆ ACMP0\_N
    - ◆ Comparator Reference Voltage (CRV)
    - ◆ Internal band-gap voltage (VBG)
    - ◆ DAC0 output (DAC0\_OUT)
- ACMP1 supports
  - 4 multiplexed I/O pins at positive sources:
    - ◆ ACMP1\_P0, ACMP1\_P1, ACMP1\_P2, or ACMP1\_P3
  - 4 negative sources:
    - ◆ ACMP1\_N
    - ◆ Comparator Reference Voltage (CRV)
    - ◆ Internal band-gap voltage (VBG)
    - ◆ DAC0 output (DAC0\_OUT)
- Shares one ACMP interrupt vector for all comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for EPWM
- Supports window compare mode and window latch mode

## 6.43 OP Amplifier (OPA)

### 6.43.1 Overview

This device is equipped with three operational amplifiers. Users can enable each of them individually, by their application purpose. One of these OP amplifier outputs is connected to ADC channel for measurement requirement.

### 6.43.2 Features

- Analog input voltage range:  $0 \sim V_{DD}$ .
- Supports up to 3 operator amplifiers.
- Supports to use Schmitt trigger buffer output for simple comparator function.
- Supports to Schmitt trigger buffer output interrupts.

## 6.44 Peripherals Interconnection

### 6.44.1 Overview

Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interact without CPU saves CPU resources, reduces power consumption, operates with no software latency and fast responds.

### 6.44.2 Peripherals Interconnect Matrix Table

| Source      | Destination |     |      |      |      |      |         |         |          |     |
|-------------|-------------|-----|------|------|------|------|---------|---------|----------|-----|
|             | BPWM        | DAC | EADC | ECAP | EPWM | HIRC | IRCTRIM | HIRC48M | TIMERPWM | QEI |
| ACMP        | -           | -   | -    | -    | 3    | -    | -       | -       | 3,6      |     |
| BOD         | -           | -   | -    | -    | 3    | -    | -       | -       | 3        |     |
| BPWM        | 4           | -   | 1    | -    | 4    | -    | -       | -       | -        |     |
| Clock Fail  | -           | -   | -    | -    | 3    | -    | -       | -       | 3        |     |
| CPU Lockup  | -           | -   | -    | -    | 3    | -    | -       | -       | 3        |     |
| EADC        | -           | -   | -    | -    | 3    | -    | -       | -       | -        |     |
| EPWM        | 4           | 1   | 1    | -    | 4    | -    | -       | -       | -        |     |
| IRCTRIM     | -           | -   | -    | -    | -    | 2    | -       | 2       | -        |     |
| LIRC        | -           | -   | -    | -    | -    | -    | -       | -       | 6        |     |
| LXT         | -           | -   | -    | -    | -    | -    | 2       | -       | -        |     |
| QEI         | -           | -   | -    | 8    | -    | -    | -       | -       | -        |     |
| SRAM        | -           | -   | -    | -    | 3    | -    | -       | -       | 3        |     |
| TIMERPWM    | 5           | 1   | 1    | -    | 5    | -    | -       | -       | 7        | 9   |
| USB11Device | -           | -   | -    | -    | -    | -    | 2       | -       | -        |     |

Table 6.44-1 Peripherals Interconnect Matrix table

### 6.44.3 Functional Description

#### 6.44.3.1 From EPWM, TIMER to EADC/DAC

##### EPWM Trigger EADC Conversion

EPWM can be one of the EADC conversion trigger source.

Setting the EADC external hardware trigger input source from EPWM trigger is described in TRM section 6.40.5.8.

##### EPWM Trigger DAC Conversion

EPWM can also be used to trigger DAC conversion.

Setting the DAC hardware trigger input source from EPWM trigger is described in TRM section 6.41.5.6.

The detailed EPWM trigger conditions are described in TRM section 6.12.5.27.

**BPWM Trigger EADC Conversion**

BPWM can be one of the EADC conversion trigger source.

Setting the EADC external hardware trigger input source from BPWM trigger is described in TRM section 6.40.5.8.

The detailed BPWM trigger conditions are described in TRM section 6.13.5.16.

**Timer Trigger EADC Conversion**

Timer0 ~ Timer3 can be one of the EADC conversion trigger source. When timer counter value matches the timer compared value or when the TMx\_EXT pin edge transition meets setting, timer will trigger the ADC to start the conversion.

Setting the EADC external hardware trigger input source from timer trigger is described in TRM section 6.40.5.9.

**Timer Trigger DAC Conversion**

Setting the DAC hardware trigger input source from TIMER trigger is described in TRM section 6.41.5.6.

The detailed Timer trigger conditions are described in TRM section 6.8.5.10.

***6.44.3.2 From LXT and USB 1.1 Device to HIRC TRIM & RC 48 MHz*****Use LXT or USB Synchronous Mode to System Auto-trim HIRC Circuit**

This chip supports auto-trim function: the HIRC trim (12 MHz RC oscillator) and RC 48 MHz oscillator, according to the accurate external 32.768 kHz crystal oscillator or internal USB synchronous mode, automatically gets accurate output frequency, 0.25 % deviation within all temperature ranges.

The detail of HIRC trim setting is described in section 6.2.9

***6.44.3.3 From ACMP, BOD, Clock Fail, SRAM Parity Error and CPU Lockup to EPWM/ TIMERPWM*****EPWM Brake Source**

EPWM brake source can be ACMP0/1\_O output signal or EADC result monitor or several different system fail conditions include clock fail, Brown-out detect, and Core lockup and SRAM Parity Error. When system fault, EPWM brake signal generated, EPWM output will be set to protect the power switch controlled by EPWM.

The detailed setting of EPWM brake function is described in TRM section 6.12.5.23.

**TIMERPWM Brake Source**

TIMERPWM brake source can be ACMP0/1\_O output signal or several different system fail conditions include clock fail, Brown-out detect, and Core lockup and SRAM Parity Error. When system fault, EPWM brake signal generated, EPWM output will be set to protect the power switch controlled by EPWM.

The detailed setting of TIMERPWM brake function is described in TRM section 6.8.6.17.

6.44.3.4 *From EPWM/ BPWM to EPWM/ BPWM*

**EPWM Synchronous Start Function**

Select synchronous source from EPWM0 or EPWM1 or BPWM0 or BPWM1, and select EPWM channels. The chosen EPWM channels will start counting at the same time once the synchronous start function is enabled and CNTSEN(EPWM\_SSTRG[0]) is set.

The detailed setting of EPWM synchronous start function is described in TRM section 6.12.5.19.

**BPWM Synchronous Start Function**

Select synchronous source from EPWM0 or EPWM1 or BPWM0 or BPWM1, and select BPWM channels. The chosen BPWM channels will start counting at the same time once the synchronous start function is enabled and CNTSEN(BPWM\_SSTRG[0]) is set.

The detailed setting of BPWM synchronous start function is described in TRM section 6.13.5.11.

6.44.3.5 *From TIMER to EPWM/BPWM*

**Timer Generates Trigger Pulses as EPWM External Clock Source**

Timer0 ~ Timer3 can generate trigger pulses as EPWM/BPWM external clock source.

When timer counter value matches the timer compared value or when the TMx\_EXT pin edge transition meets setting, timer can generate a trigger pulse by setting described in TRM section 6.8.5.10.

The setting of EPWM/BPWM clock source are described in TRM section 6.13.3 / 6.12.3.

6.44.3.6 *From ACMP and LIRC to Timer Capture Function*

**Measure the Time Interval of ACMP0/1 Output Signal or LIRC Clock Speed**

Sets the timer capture source from ACMP0/1 output signal or LIRC clock and measures the time interval of the signal by using timer capture function. Users can use the results of time interval to trim LIRC through software or to get the ACMP0/1 output pulse width.

The detail of time capture function setting is described in TRM section 6.8.5.8 and 6.8.5.9.

6.44.3.7 *From Timer0/2 to Timer1/3*

**Inter-Timer Trigger Capture Mode**

Timer0/2 will be forced in event counting mode, counting with external event, and will generate an internal signal (INTR\_TMR\_TRG) to trigger Timer1/3 start or stop counting. The Timer1/3 will be forced in capture mode and start/stop trigger-counting by Timer0/2 counter status.

The detail of inter-timer trigger capture mode is described in TRM section 6.8.5.11.

6.44.3.8 *From QEI to ECAP*

**ECAP Input Noise Filter**

The architecture of ECAP input noise filter is similar to that one used for QEI. With 6 sampling-rate options, it supports a wide range of filtering noise, the duration of filtered noise and the duration of the signal that is guaranteed to be sampled.

The detailed setting of modulation is described in TRM section 6.14.5.1.

#### 6.44.3.9 From TIMER to QEI

##### **TIMER TIF Event to QEI**

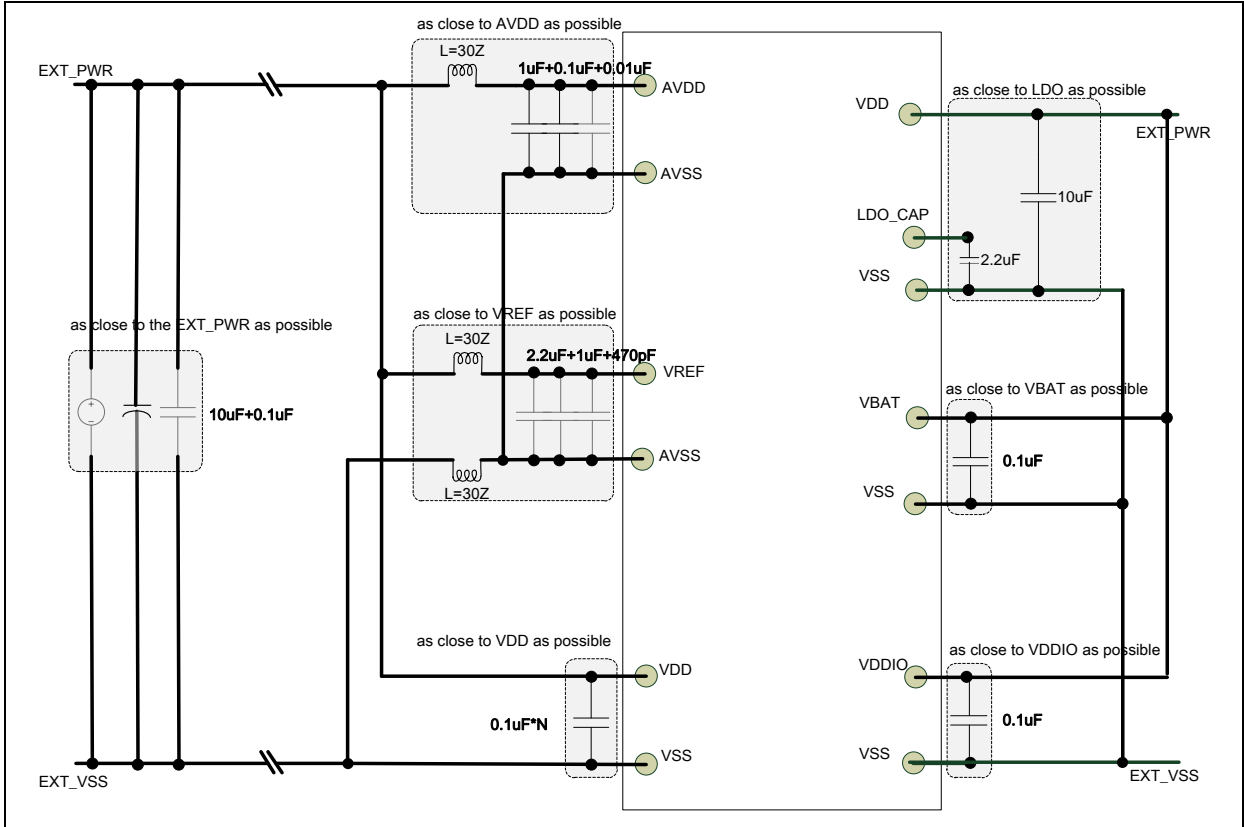
When QEI bit HOLDCNT(QEI\_CTL[24]) set, the CNT(QEI\_CNT[31:0]) content will be captured into QEI Counter Hold Register CNTHOLD(QEI\_CNTHOLD[31:0]), the data will be held until the next HOLDCNT (QEI\_CTL[24]) trigger comes. The bit HOLDCNT can be set by writing 1 to it or the rising edge of timers interrupt flags TIF (TIMERx\_INTSTS[0]) The detailed setting of modulation is described in TRM section 6.14.5.11.

The detailed setting of modulation is described in TRM section 6.8.5.1.



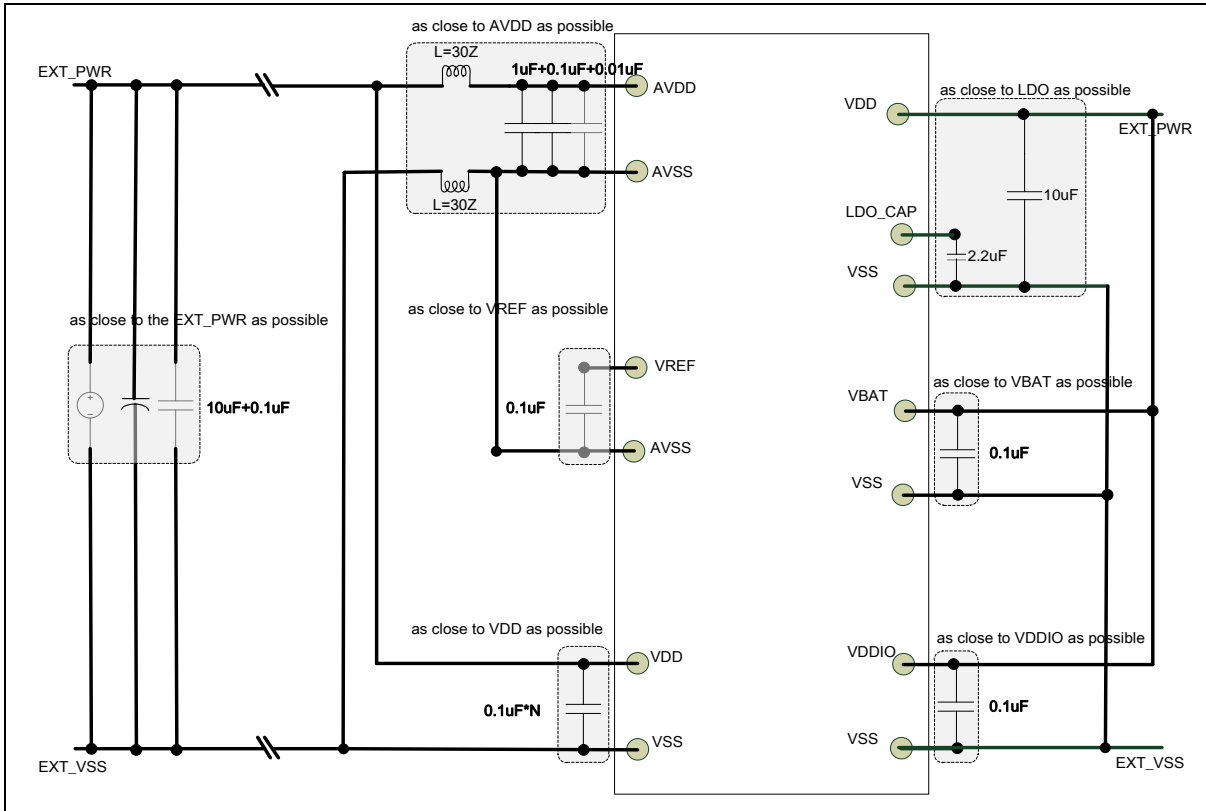
## 7 APPLICATION CIRCUIT

### 7.1 Power Supply Scheme with External V<sub>REF</sub>



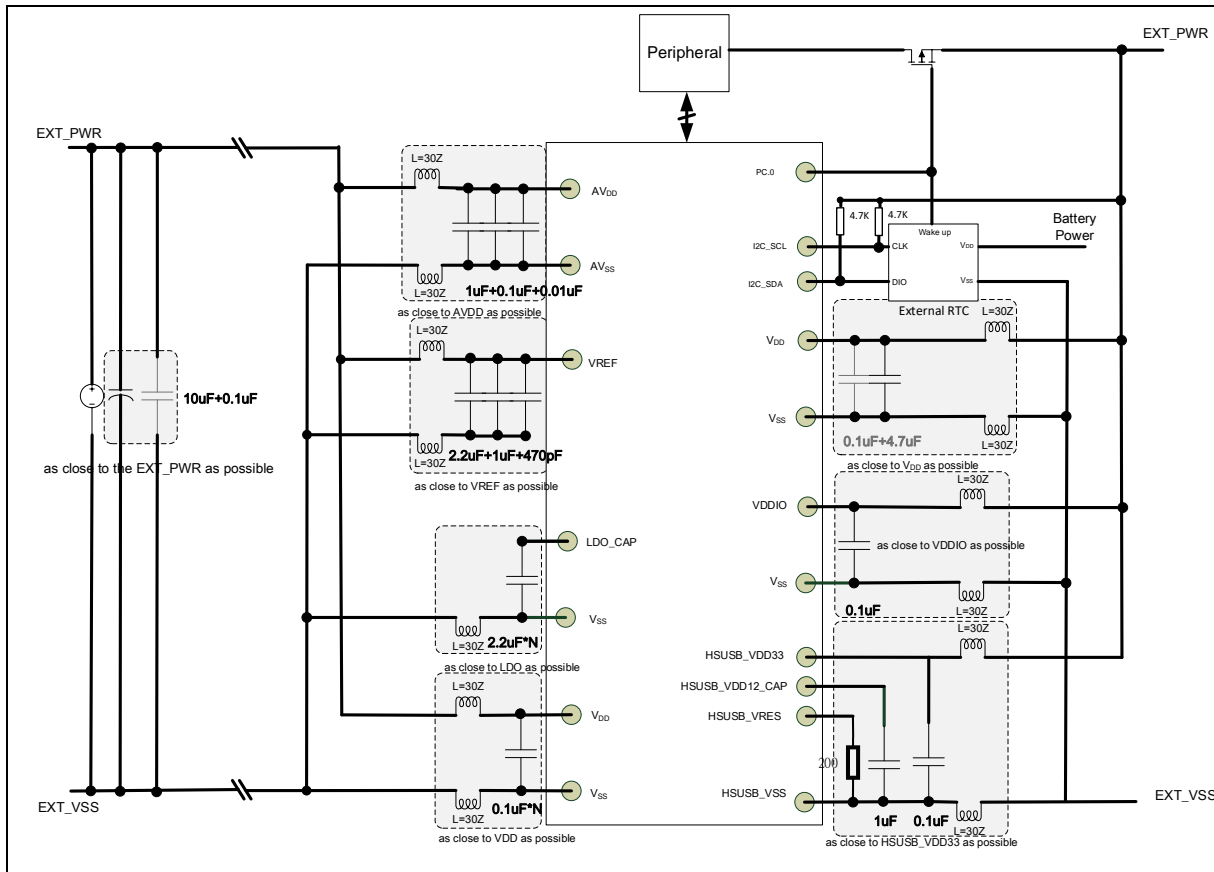
**Note:** Total capacitance of LDO\_CAP pin is 2.2uF.

7.2 Power Supply Scheme with Internal V<sub>REF</sub>



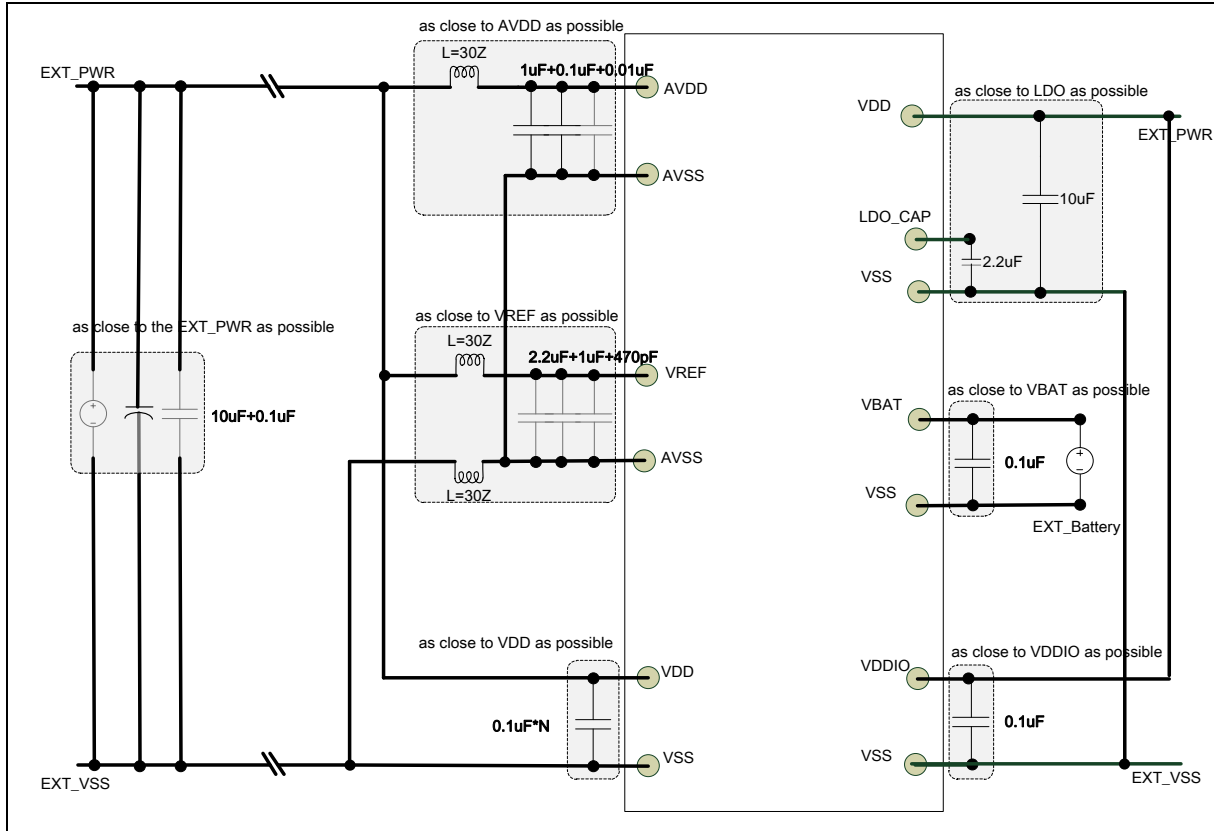
**Note:** Total capacitance of LDO\_CAP pin is 2.2uF.

7.3 Power Supply Scheme with V<sub>REF</sub> and External RTC with Battery Power



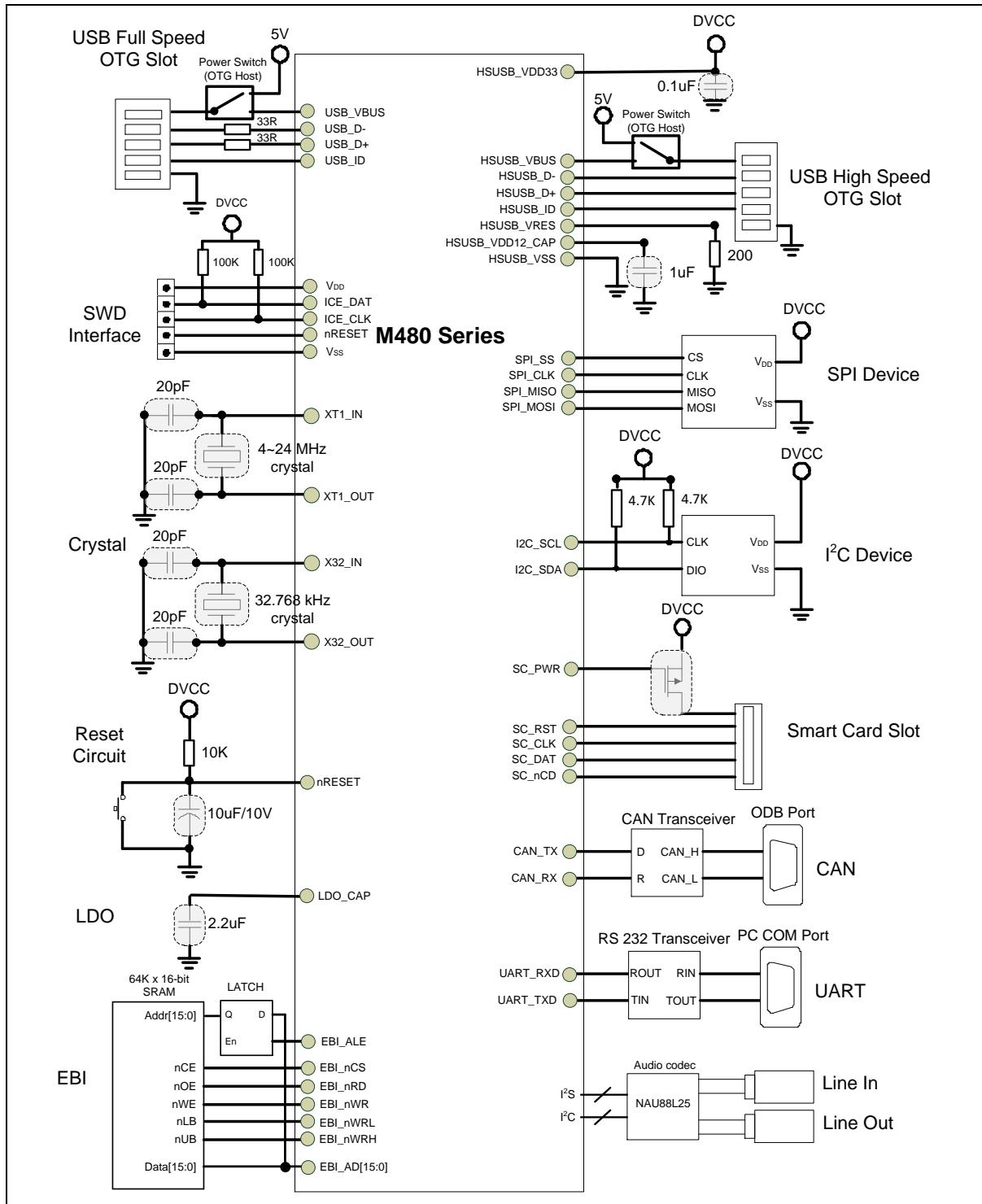
**Note:** Total capacitance of LDO\_CAP pin is 2.2uF.

7.4 Power Supply Scheme with V<sub>REF</sub> and Internal RTC with Battery Power



**Note:** Total capacitance of LDO\_CAP pin is 2.2uF.

7.5 Peripheral Application Scheme



**Note 1:** USB\_ID, HSUSB\_ID could be floating using USB or USB HS without OTG.

**Note 2:** It is recommended to use 100 kΩ pull-up resistor on both ICE\_DAT and ICE\_CLK pin.

**Note 3:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

**Note 4:** Total capacitance of LDO\_CAP pin is 2.2uF.

## 8 ELECTRICAL CHARACTERISTICS FOR M48XID/M487KMCAN

### 8.1 Absolute Maximum Ratings

#### 8.1.1 Voltage Characteristics

| Parameter            | Symbol  | Min  | Max      | Unit |
|----------------------|---|------|----------|------|
| $V_{DD}-V_{SS}$ [*1] | DC Power Supply                                       | -0.3 | 4        | V    |
| $V_{DDIO}-V_{SS}$    | $V_{DDIO}$ Power Supply                               | -0.3 | 4        | V    |
| $ V_{DDX} - V_{DD} $ | Variations between different power pins               |      | 50       | mV   |
| $ V_{DD} - AV_{DD} $ | Allowed voltage difference for $V_{DD}$ and $AV_{DD}$ |      | 50       | mV   |
| $ V_{SSX} - V_{SS} $ | Variations between different ground pins              |      | 50       | mV   |
| $ V_{SS} - AV_{SS} $ | Allowed voltage difference for $V_{SS}$ and $AV_{SS}$ |      | 50       | mV   |
| $V_{IN}$             | Input Voltage on 5V-tolerance GPIO                    |      | 5.5      | V    |
|                      | Input Voltage on RTC domain (PF.6 ~ PF.11)            |      | $V_{DD}$ | V    |
|                      | Input Voltage on any other pin[*2]                    |      | $V_{DD}$ | V    |

**Note:**

- All main power ( $V_{DD}$ ,  $AV_{DD}$ ) and ground ( $V_{SS}$ ,  $AV_{SS}$ ) pins must always be connected to the external power supply, in the permitted range.
- Non 5V-tolerance PIN: PA.8 ~ 15; PB.0 ~ 15; PD.10, 11, 12; PF.2, 3, 4, 5; All USB High Speed PIN and nRESET PIN.

Table 8.1-1 Voltage Characteristics

#### 8.1.2 Current Characteristics

| Symbol     | Parameter                                 | Min | Max | Unit |
|------------|---|-----|-----|------|
| $I_{DD}$   | Maximum Current into $V_{DD}$             |     | 200 | mA   |
| $I_{DDIO}$ | Maximum Current into $V_{DDIO}$           |     | 100 |      |
| $I_{SS}$   | Maximum Current out of $V_{SS}$           |     | 100 |      |
| $I_{IO}$   | Maximum Current sunk by a I/O Pin         |     | 20  |      |
|            | Maximum Current Sourced by a I/O Pin      |     | 20  |      |
|            | Maximum Current Sunk by Total I/O Pins    |     | 100 |      |
|            | Maximum Current Sourced by Total I/O Pins |     | 100 |      |

Table 8.1-2 Current Characteristics

**8.1.3 Thermal Characteristics**

The average junction temperature can be calculated by using the following equation:

$$T_J = T_A + (P_D \times \theta_{JA})$$

- $T_A$  = ambient temperature (°C)
- $\theta_{JA}$  = thermal resistance junction-ambient (°C/Watt)
- $P_D$  = sum of internal and I/O power dissipation

| Symbol   | Description   | Min | Typ  | Max | Unit    |
|--|---|-----|------|-----|---------|
| $T_A$  | Operating ambient temperature (M48xID)                        | -40 | -    | 105 | °C      |
|  | Operating ambient temperature (M487KMCAN)                     | -40 | -    | 85  |         |
| $T_J$  | Operating junction temperature                                | -40 | -    | 125 |         |
| $T_{ST}$   | Storage temperature   | -65 | -    | 150 |         |
|  | Thermal resistance junction-ambient<br>33-pin QFN(5x5 mm)     | -   | 39.6 | -   | °C/Watt |
|  | Thermal resistance junction-ambient<br>48-pin LQFP(7x7 mm)    | -   | 60   | -   | °C/Watt |
|  | Thermal resistance junction-ambient<br>64-pin LQFP(7x7 mm)    | -   | 58   | -   | °C/Watt |
|  | Thermal resistance junction-ambient<br>128-pin LQFP(14x14 mm) | -   | 38.5 | -   | °C/Watt |
|  | Thermal resistance junction-ambient<br>144-pin LQFP(14x14 mm) | -   | 36.9 | -   | °C/Watt |
| <b>Note:</b>   |   |     |      |     |         |
| 1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions |   |     |      |     |         |

Table 8.1-3 Thermal Characteristics

**8.1.4 EMC Characteristics**

**8.1.4.1 Electrostatic discharge (ESD)**

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

**8.1.4.2 Static latchup**

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin





8.1.4.3 Electrical fast transients (EFT)

In some application circuit component will produce fast and narrow high-frequency transients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International Electrotechnical Commission (IEC).

| Symbol     | Parameter  | Conditions   | Maximum Value | Unit |
|------------|--|--|---------------|------|
| $V_{EFTB}$ | 1. Fast transient voltage burst limits to be applied through 100 pF + 47uF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance<br>2. to be applied through 2.2uF on LDO_Pin and $V_{SS}$ pins | $V_{DD} = 3.3\text{ V}$ , LQFP144, $T_A = +25\text{ }^\circ\text{C}$ , $f_{HCLK} = 160\text{ MHz}$ | 4.4           | kV   |

Table 8.1-4 EMS Characteristics

| Symbol   | Ratings   | Conditions                        | Maximum Value       | Unit |
|--|---|-----------------------------------|---------------------|------|
| $V_{ESD(HBM)}$   | Electrostatic discharge voltage (human body model)    | $T_A = +25\text{ }^\circ\text{C}$ | 1 <sup>[*1]</sup>   | kV   |
| $V_{ESD(CDM)}$   | Electrostatic discharge voltage (charge device model) | $T_A = +25\text{ }^\circ\text{C}$ | 0.5 <sup>[*1]</sup> |      |
| <b>Note:</b>   |   |                                   |                     |      |
| 1. Guaranteed by characterization results, not tested in production. |   |                                   |                     |      |

Table 8.1-5 ESD Characteristics

| Symbol   | Parameter             | Conditions                        | Value | Unit |
|--|-----------------------|-----------------------------------|-------|------|
| LU   | Static latch-up class | $T_A = +25\text{ }^\circ\text{C}$ | 400mA | mA   |
| <b>Note:</b>   |                       |                                   |       |      |
| 1. Guaranteed by characterization results, not tested in production. |                       |                                   |       |      |

Table 8.1-6 Electrical Characteristics

**8.1.5 Package Moisture Sensitivity(MSL)**

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

| Pacakge  | MSL   |
|--|-------|
| 33-pin QFN(5x5 mm) <sup>[*1]</sup>             | MSL 3 |
| 48-pin LQFP(7x7 mm) <sup>[*1]</sup>            | MSL 3 |
| 64-pin LQFP(7x7 mm) <sup>[*1]</sup>            | MSL 3 |
| 128-pin LQFP(14x14 mm) <sup>[*1]</sup>         | MSL 3 |
| 144-pin LQFP(20x20mm) <sup>[*1]</sup>          | MSL 3 |
| <b>Note:</b>                                   |       |
| 1. Determined according to IPC/JEDEC J-STD-020 |       |

Table 8.1-7 Package Moisture Sensitivity(MSL)

8.1.6 Soldering Profile

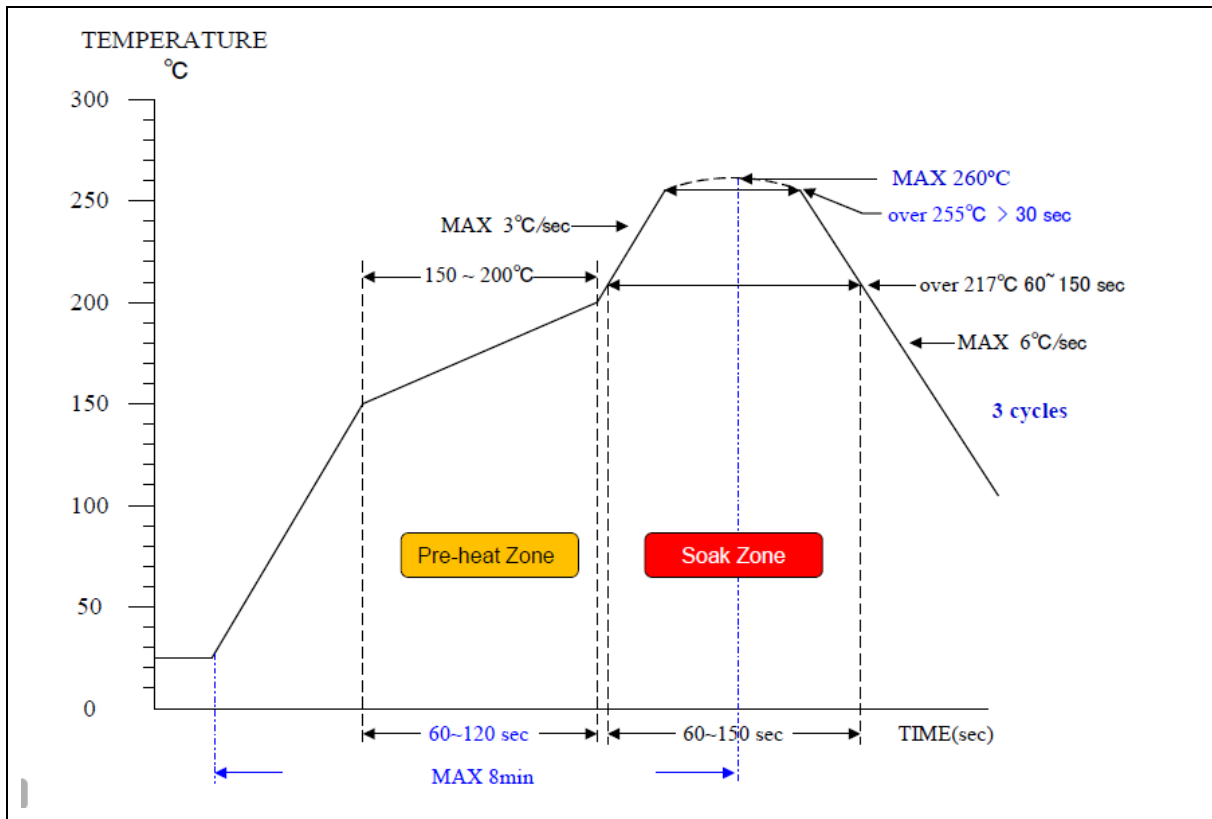


Figure 8.1-8 Soldering Profile From J-STD-020C

| Profile Feature                          | Pb Free Package     |
|--|---------------------|
| Average ramp-up rate (217°C to peak)     | 3°C/sec. max        |
| Preheat temperature 150°C ~200°C         | 60 sec. to 120 sec. |
| Temperature maintained above 217°C       | 60 sec. to 150 sec. |
| Time with 5°C of actual peak temperature | > 30 sec.           |
| Peak temperature range                   | 260°C               |
| Ramp-down rate                           | 6°C/sec ax.         |
| Time 25°C to peak temperature            | 8 min. max          |
| <b>Note:</b>                             |                     |
| 1. Determined according to J-STD-020C    |                     |

Table 8.1-9 Soldering Profile

### 8.2 General Operating Conditions

(V<sub>DD</sub>-V<sub>SS</sub> = 1.8 ~ 3.6V, T<sub>A</sub> = 25°C, HCLK = 192 MHz unless otherwise specified.)

| Symbol                 | Parameter   | Conditions  | Min             | Typ  | Max  | Unit |
|------------------------|---|---|-----------------|------|------|------|
| f <sub>HCLK</sub>      | Internal AHB clock frequency  |   |                 |      | 192  | MHz  |
| V <sub>DD</sub>        | Operation Voltage (M48xID)  |   | 1.8             |      | 3.6  | V    |
| V <sub>DD</sub>        | Operation Voltage (M487KMCAN)   |   | 2.7             |      | 3.6  |      |
| AV <sub>DD</sub>       | Analog Operation Voltage  |   | V <sub>DD</sub> |      |      |      |
| V <sub>DDIO</sub>      | Power supply for PA.0 ~ 5   |   | 1.8             |      | 3.6  |      |
| V <sub>LDO</sub>       | LDO Output Voltage  |   |                 | 1.26 |      |      |
| V <sub>BG</sub>        | Band-gap Voltage  | V <sub>DD</sub> = 1.8 V ~ 3.6 V   | 1.16            |      | 1.25 |      |
| C <sub>LDO</sub>       | LDO Output capacitance on each pin  |   |                 | 2.2  |      | uF   |
| I <sub>RUSH</sub> [*1] | InRush current on voltage regulator power-on (POR or wakeup from Standby) | VDD bypass CAP = 0.1uF, LDO_CAP = 2.2uF   | -               | 617  | -    | mA   |
|                        |   | VDD closed to LDO_CAP pin bypass CAP = 10uF; others VDD bypass CAP = 0.1uF, LDO_CAP = 2.2uF | -               | 450  | -    |      |
| t <sub>VDD</sub>       | V <sub>DD</sub> rise time rate  |   | 10              | -    |      | μs/V |
|                        | V <sub>DD</sub> fall time rate  | BOD Disabled, LVR Enabled[*2]   | 400             | -    |      |      |
|                        |   | BOD Disabled, LVR Enabled[*3]   | 500             |      |      |      |
|                        |   | BOD 1.6V Enabled  | 80              |      |      |      |
|                        |   | BOD 3.0V Enabled  | 80              |      |      |      |

**Note:**

- Guaranteed by design, not tested in production
- LVR in active mode
- LVR in low power mode

### 8.3 DC Electrical Characteristics

#### 8.3.1 Typical Current Consumption(M48xID)

- ALL GPIO pins are in push pull mode, output high.
- LDO = 1.26V
- The maximum values are obtained for  $V_{DD} = 3.6\text{ V}$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25\text{ }^\circ\text{C}$  and  $V_{DD} = 3.3\text{ V}$  unless otherwise specified.
- $V_{DD} = AV_{DD} = V_{DDIO}$
- When the peripherals are enabled HCLK is the system clock,  $f_{PCLK0,1} = f_{HCLK}/2$ .
- Program run while(1){} from Flash.

| Symbol     | Conditions  | $F_{HCLK}$ | HXT/LXT    | HIRC/LIRC | PLL  | Typ                              | Unit |
|------------|---|------------|------------|-----------|------|----------------------------------|------|
|            |   |            |            |           |      | $T_A = 25\text{ }^\circ\text{C}$ |      |
| $I_{DD}$   | Normal Run, executed from Flash, $V_{DD} = 3.3\text{V}$ , all peripherals disable                 | 192 MHz    | 12 MHz     | -         | V    | 34.00                            | mA   |
|            |   | 160 MHz    | 12 MHz     | -         | V    | 28.76                            |      |
|            |   | 144 MHz    | 12 MHz     | -         | V    | 26.00                            |      |
|            |   | 120 MHz    | 12 MHz     | -         | V    | 22.21                            |      |
|            |   | 12 MHz     | 12 MHz     | -         | -    | 3.49                             |      |
|            |   | 192 MHz    | -          | 12 MHz    | V    | 33.29                            |      |
|            |   | 160 MHz    | -          | 12 MHz    | V    | 28.11                            |      |
|            |   | 144 MHz    | -          | 12 MHz    | V    | 25.51                            |      |
|            |   | 120 MHz    | -          | 12 MHz    | V    | 21.59                            |      |
|            |   | 12 MHz     | -          | 12 MHz    | -    | 2.98                             |      |
|            |   | 32.768 kHz | 32.768 kHz | -         | -    | 0.57                             |      |
|            | 10 kHz  | -          | 10 kHz     | -         | 0.57 |                                  |      |
|            | Normal run, External clock, executed from Flash, $V_{DD} = 3.3\text{V}$ , all peripherals enabled | 192 MHz    | -          | 12 MHz    | V    | 70.05                            |      |
|            |   | 160 MHz    | -          | 12 MHz    | V    | 58.99                            |      |
|            |   | 144 MHz    | -          | 12 MHz    | V    | 53.43                            |      |
|            |   | 120 MHz    | -          | 12 MHz    | V    | 45.04                            |      |
|            |   | 12 MHz     | -          | 12 MHz    | -    | 5.60                             |      |
|            |   | 192 MHz    | 12 MHz     | -         | V    | 70.70                            |      |
|            |   | 160 MHz    | 12 MHz     | -         | V    | 60.41                            |      |
|            |   | 144 MHz    | 12 MHz     | -         | V    | 53.75                            |      |
|            |   | 120 MHz    | 12 MHz     | -         | V    | 46.04                            |      |
|            |   | 12 MHz     | 12 MHz     | -         | -    | 5.85                             |      |
| 32.768 kHz |   | 32.768 kHz | -          | -         | 0.58 |                                  |      |
| 10 kHz     | -   | 10 kHz     | -          | 0.57      |      |                                  |      |

Table 8.3-1 Current Consumption in Normal Run Mode

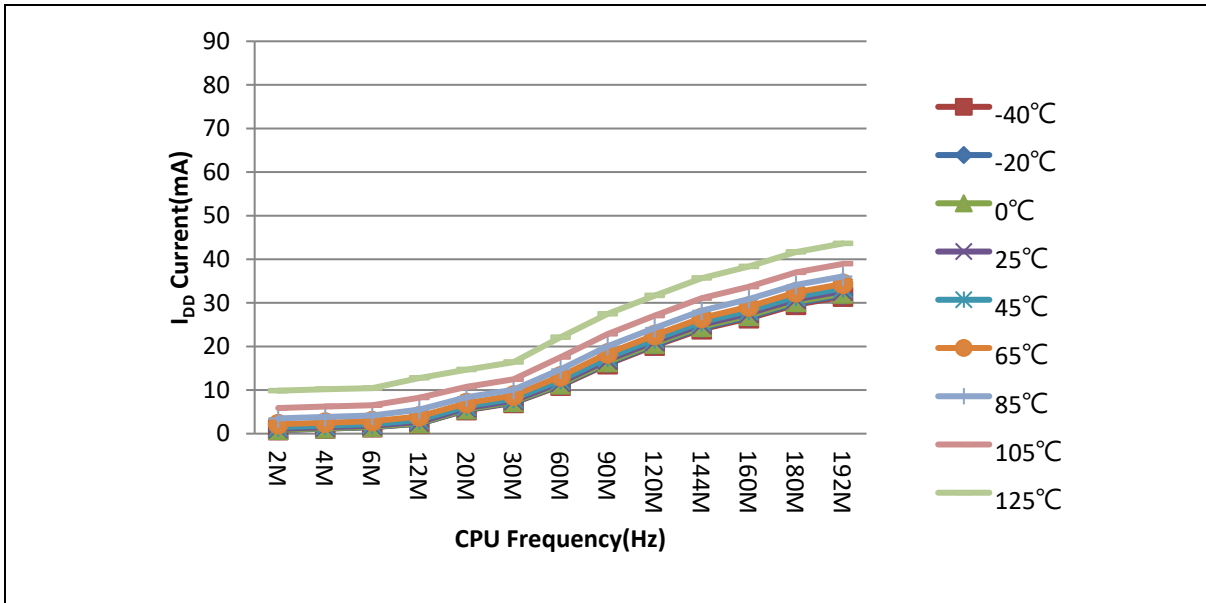


Figure 8-1 Current Consumption Versus Temperature in Normal Run Mode,  $V_{DD} = 3.3V$  , All Peripherals Disabled, PLL Source From HIRC

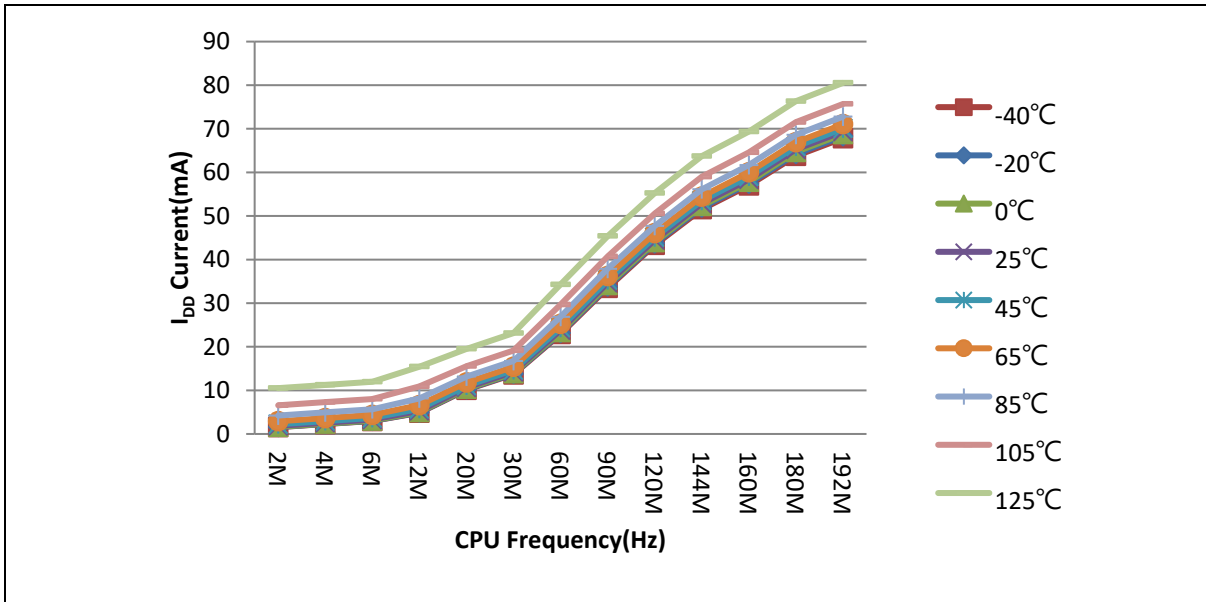


Figure 8-2 Current Consumption Versus Temperature in Normal Run Mode,  $V_{DD} = 3.3V$  , All Peripherals Enabled, PLL Source From HIRC

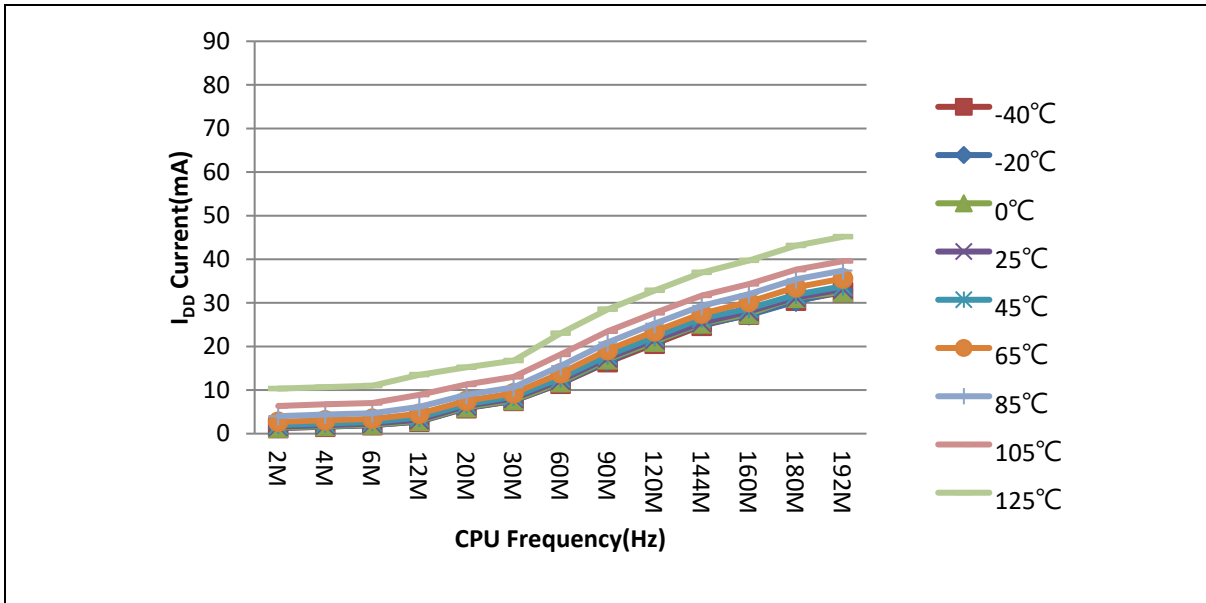


Figure 8-3 Current Consumption Versus Temperature in Normal Run Mode,  $V_{DD} = 3.3V$  , All Peripherals Disabled, PLL Source From HXT

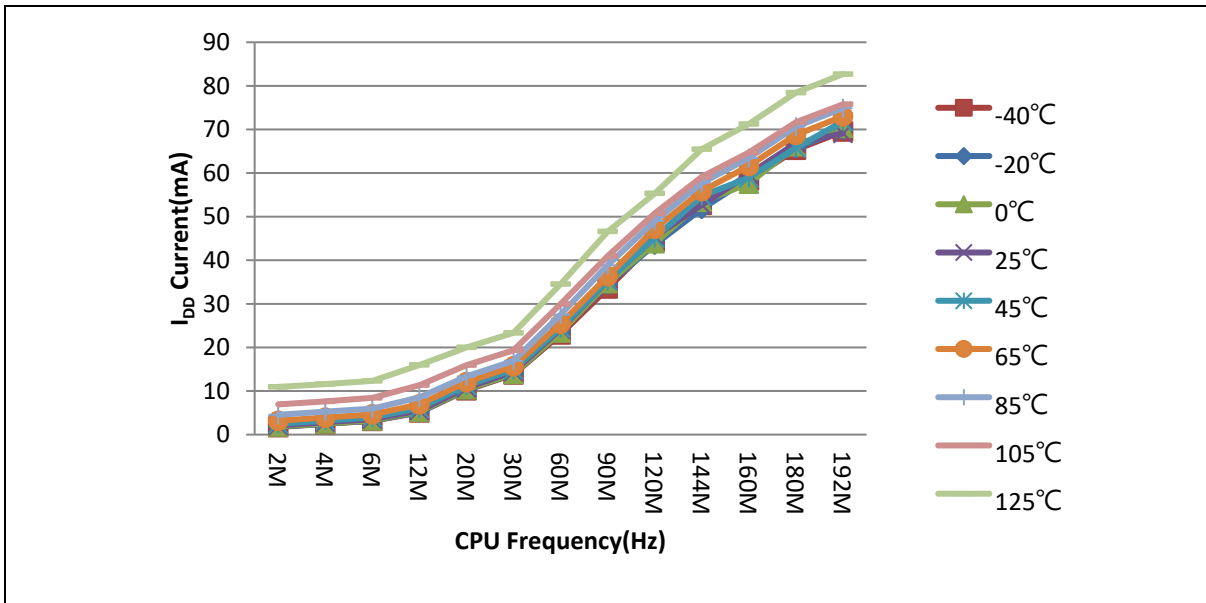


Figure 8-4 Current Consumption Versus Temperature in Normal Run Mode,  $V_{DD} = 3.3V$  , All Peripherals Enabled, PLL Source From HXT

| Symbol          | Conditions  | F <sub>HCLK</sub> | HXT/LXT    | HIRC/LIRC | PLL | Typ                    | Unit |
|-----------------|---|-------------------|------------|-----------|-----|------------------------|------|
|                 |   |                   |            |           |     | T <sub>A</sub> = 25 °C |      |
| I <sub>DD</sub> | Idle mode, executed from Flash, V <sub>DD</sub> = 3.3V, all peripherals disable                 | 192 MHz           | 12 MHz     | -         | V   | 10.32                  | mA   |
|                 |   | 160 MHz           | 12 MHz     | -         | V   | 8.95                   |      |
|                 |   | 144 MHz           | 12 MHz     | -         | V   | 8.23                   |      |
|                 |   | 120 MHz           | 12 MHz     | -         | V   | 7.23                   |      |
|                 |   | 12 MHz            | 12 MHz     | -         | -   | 1.98                   |      |
|                 |   | 192 MHz           | -          | 12 MHz    | V   | 9.76                   |      |
|                 |   | 160 MHz           | -          | 12 MHz    | V   | 8.40                   |      |
|                 |   | 144 MHz           | -          | 12 MHz    | V   | 7.72                   |      |
|                 |   | 120 MHz           | -          | 12 MHz    | V   | 6.70                   |      |
|                 |   | 12 MHz            | -          | 12 MHz    | -   | 1.47                   |      |
|                 |   | 32.768 kHz        | 32.768 kHz | -         | -   | 0.57                   |      |
|                 |   | 10 kHz            | -          | 10 kHz    | -   | 0.57                   |      |
|                 | Idle mode, External clock, executed from Flash, V <sub>DD</sub> = 3.3V, all peripherals enabled | 192 MHz           | -          | 12 MHz    | V   | 49.64                  |      |
|                 |   | 160 MHz           | -          | 12 MHz    | V   | 41.82                  |      |
|                 |   | 144 MHz           | -          | 12 MHz    | V   | 37.89                  |      |
|                 |   | 120 MHz           | -          | 12 MHz    | V   | 31.96                  |      |
|                 |   | 12 MHz            | -          | 12 MHz    | -   | 4.03                   |      |
|                 |   | 192 MHz           | 12 MHz     | -         | V   | 50.36                  |      |
|                 |   | 160 MHz           | 12 MHz     | -         | V   | 42.75                  |      |
|                 |   | 144 MHz           | 12 MHz     | -         | V   | 38.29                  |      |
|                 |   | 120 MHz           | 12 MHz     | -         | V   | 32.70                  |      |
|                 |   | 12 MHz            | 12 MHz     | -         | -   | 4.52                   |      |
|                 |   | 32.768 kHz        | 32.768 kHz | -         | -   | 0.58                   |      |
|                 |   | 10 kHz            | -          | 10 kHz    | -   | 0.57                   |      |

Table 8.3-2 Current Consumption in Idle Mode



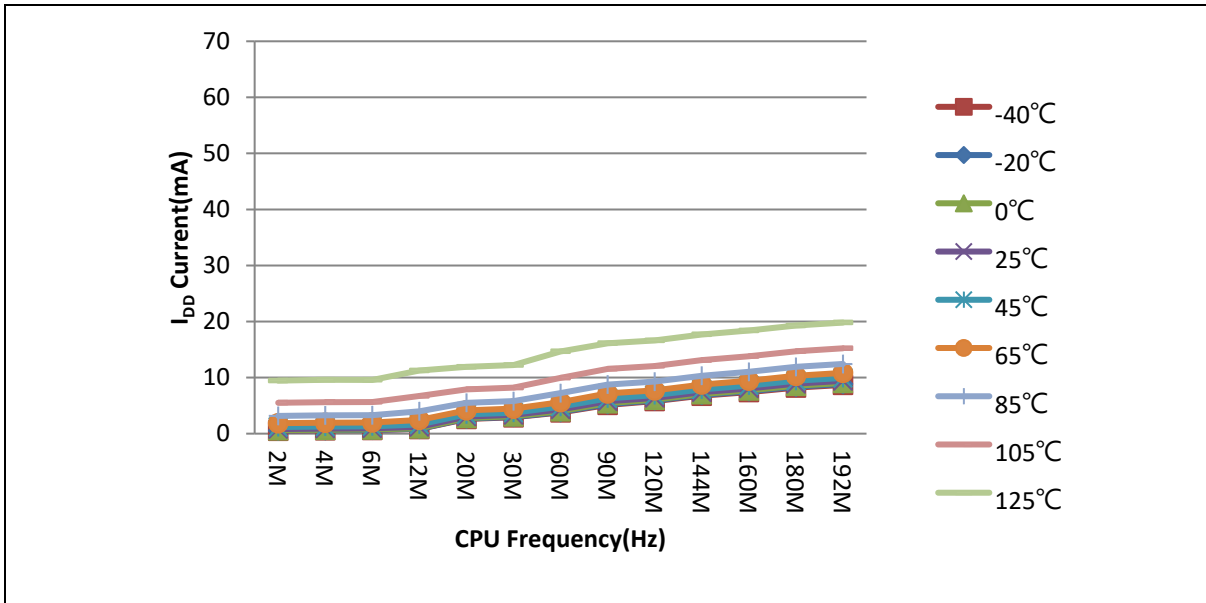


Figure 8-5 Current Consumption Versus Temperature in Idle Mode,  $V_{DD} = 3.3V$  , All Peripherals Disabled, PLL Source From HIRC

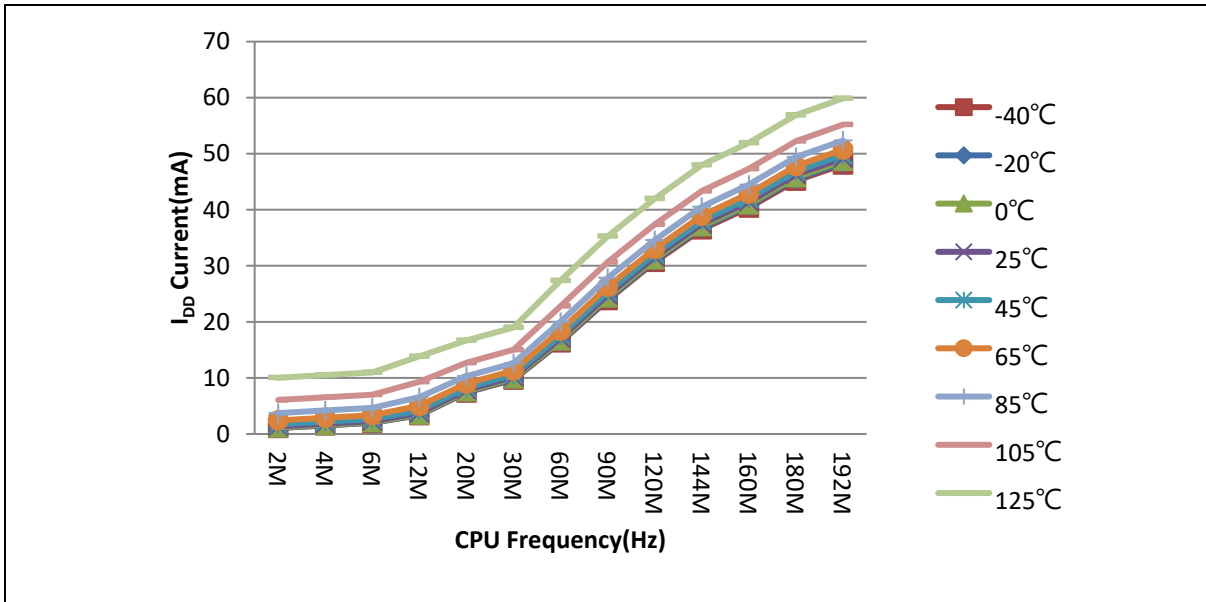


Figure 8-6 Current Consumption Versus Temperature in Idle Mode,  $V_{DD} = 3.3V$  , All Peripherals Enabled, PLL Source From HIRC

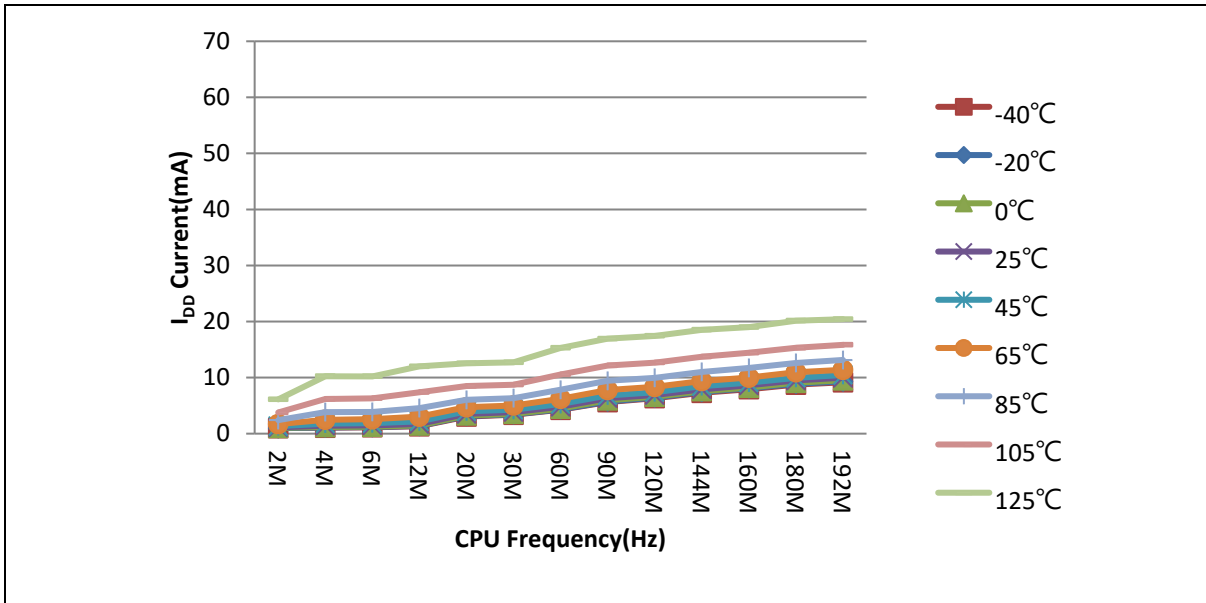


Figure 8-7 Current Consumption Versus Temperature in Idle Mode,  $V_{DD} = 3.3V$  , All Peripherals Disabled, PLL Source From HXT

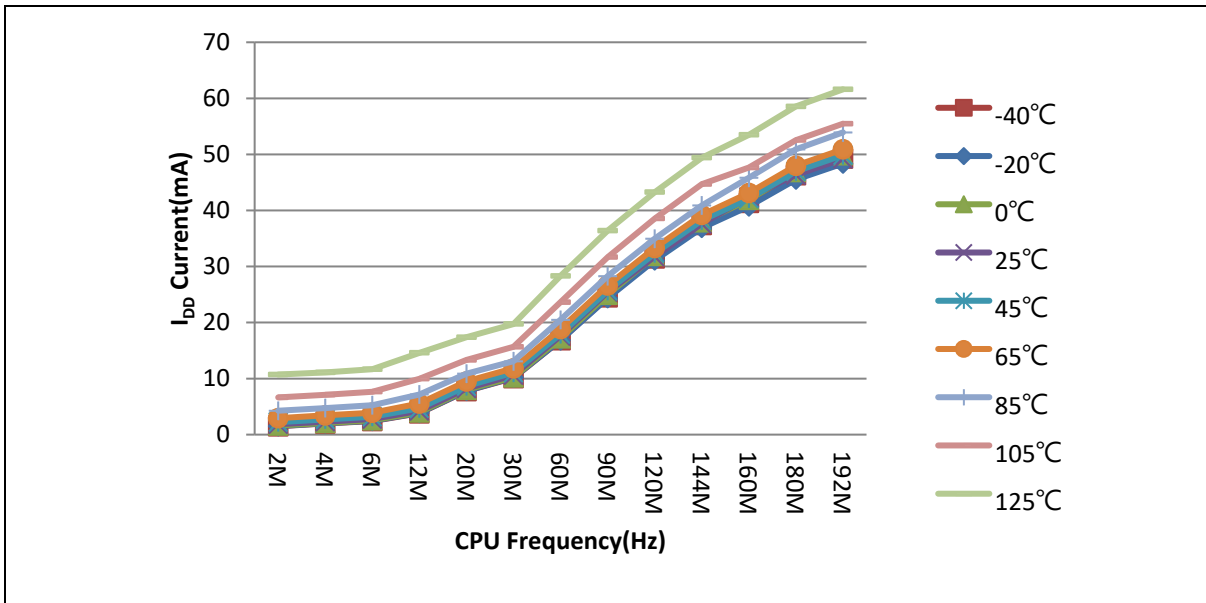


Figure 8-8 Current Consumption Versus Temperature in Idle Mode,  $V_{DD} = 3.3V$  , All Peripherals Enabled, PLL Source From HXT

| Symbol                | Conditions   | LXT | LIRC | PLL | Typ                    | Unit |
|-----------------------|--|-----|------|-----|------------------------|------|
|                       |  |     |      |     | T <sub>A</sub> = 25 °C |      |
| I <sub>DD_FWPD</sub>  | Fast wake-up Power-down mode, V <sub>DD</sub> = 3.3V, all peripherals disabled             | -   | -    | -   | 0.49                   | mA   |
|                       | Fast wake-up Power-down mode, V <sub>DD</sub> = 3.3V, RTC/WDT/Timer/UART enable            | V   | -    | -   | 0.49                   |      |
|                       | Fast wake-up Power-down mode, V <sub>DD</sub> = 3.3V, RTC/WDT/Timer enable                 | -   | V    | -   | 0.49                   |      |
|                       | Fast wake-up Power-down mode, V <sub>DD</sub> = 3.3V, WDT/Timer use LIRC, RTC/UART use LXT | V   | V    | -   | 0.49                   |      |
| I <sub>DD_PD</sub>    | Power-down mode, V <sub>DD</sub> = 3.3V, all peripherals disabled                          | -   | -    | -   | 0.37                   | mA   |
|                       | Power-down mode, V <sub>DD</sub> = 3.3V, RTC/WDT/Timer/UART enable                         | V   | -    | -   | 0.37                   |      |
|                       | Power-down mode, V <sub>DD</sub> = 3.3V, RTC/WDT/Timer use LIRCT                           | -   | V    | -   | 0.37                   |      |
|                       | Power-down mode, V <sub>DD</sub> = 3.3V, WDT/Timer use LIRC, RTC/UART use LX               | V   | V    | -   | 0.37                   |      |
| I <sub>DD_LLDPD</sub> | Low leakage Power-down mode, V <sub>DD</sub> = 3.3V, all peripherals disabled              | -   | -    | -   | 0.14                   | mA   |
|                       | Low leakage Power-down mode, V <sub>DD</sub> = 3.3V, RTC/WDT/Timer/UART enable             | V   | -    | -   | 0.37                   |      |
|                       | Low leakage Power-down mode, V <sub>DD</sub> = 3.3V, RTC/WDT/Timer enable                  | -   | V    | -   | 0.37                   |      |
|                       | Low leakage Power-down mode, V <sub>DD</sub> = 3.3V, WDT/Timer use LIRC, RTC/UART use LX   | V   | V    | -   | 0.37                   |      |
| I <sub>DD_SPD0</sub>  | Standby Power-down mode (SPD0), V <sub>DD</sub> = 3.3V, all peripherals disabled           | -   | -    | -   | 0.04                   | mA   |
|                       | Standby Power-down mode (SPD0), V <sub>DD</sub> = 3.3V, RTC enable                         | V   | -    | -   | 0.04                   |      |
|                       | Standby Power-down mode (SPD0), V <sub>DD</sub> = 3.3V, RTC enable                         | -   | V    | -   | 0.04                   |      |

| Symbol   | Conditions   | LXT | LIRC | PLL | Typ                    | Unit |
|--|--|-----|------|-----|------------------------|------|
|  |  |     |      |     | T <sub>A</sub> = 25 °C |      |
| I <sub>DD_SPD1</sub>   | Standby Power-down mode (SPD1), V <sub>DD</sub> = 3.3V, all peripherals disabled | -   | -    | -   | 0.03                   | mA   |
|  | Standby Power-down mode (SPD1), V <sub>DD</sub> = 3.3V, RTC enable               | V   | -    | -   | 0.03                   |      |
|  | Standby Power-down mode (SPD1), V <sub>DD</sub> = 3.3V, RTC enable               | -   | V    | -   | 0.03                   |      |
| I <sub>DD_DPD</sub>  | Deep Power-down mode (DPD), V <sub>DD</sub> = 3.3V, all peripherals disabled     | -   | -    | -   | 0.95                   | uA   |
| <b>Note:</b>   |  |     |      |     |                        |      |
| 1. V <sub>DD</sub> = AV <sub>DD</sub> = V <sub>DDIO</sub> = 3.3V |  |     |      |     |                        |      |

Table 8.3-3 Chip Current Consumption in Power-down Mode

**8.3.2 Typical Current Consumption(M487KMCAN)**

Normal Run Mode (CPU Normal Run that executed code from SPI Flash thru SPIM)

- ALL GPIO pins are in push pull mode, output high.
- LDO = 1.26V
- The maximum values are obtained for  $V_{DD} = 3.6$  V and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25$  °C and  $V_{DD} = 3.3$  V unless otherwise specified.
- $V_{DD} = AV_{DD} = V_{DDIO}$
- When the peripherals are enabled HCLK is the system clock,  $f_{PCLK0,1} = f_{HCLK}/2$ .
- Program run while(1){} from SPI Flash.

| Symbol          | Conditions   | F <sub>HCLK</sub> | HXT/LXT | HIRC/LIRC | PLL | Typ                    | Unit |
|-----------------|--|-------------------|---------|-----------|-----|------------------------|------|
|                 |  |                   |         |           |     | T <sub>A</sub> = 25 °C |      |
| I <sub>DD</sub> | Normal Run, executed from SPI Flash, V <sub>DD</sub> = 3.3V, all peripherals disable                 | 192 MHz           | 12 MHz  | -         | V   | 50.1                   | mA   |
|                 |  | 160 MHz           | 12 MHz  | -         | V   | 42.2                   |      |
|                 |  | 144 MHz           | 12 MHz  | -         | V   | 38.3                   |      |
|                 |  | 120 MHz           | 12 MHz  | -         | V   | 33.2                   |      |
|                 |  | 192 MHz           | -       | 12 MHz    | V   | 50.1                   |      |
|                 |  | 160 MHz           | -       | 12 MHz    | V   | 42.2                   |      |
|                 |  | 144 MHz           | -       | 12 MHz    | V   | 38.3                   |      |
|                 |  | 120 MHz           | -       | 12 MHz    | V   | 33.2                   |      |
|                 | Normal run, External clock, executed from SPI Flash, V <sub>DD</sub> = 3.3V, all peripherals enabled | 192 MHz           | -       | 12 MHz    | V   | 72.5                   |      |
|                 |  | 160 MHz           | -       | 12 MHz    | V   | 60.9                   |      |
|                 |  | 144 MHz           | -       | 12 MHz    | V   | 55.1                   |      |
|                 |  | 120 MHz           | -       | 12 MHz    | V   | 47.3                   |      |
|                 |  | 192 MHz           | 12 MHz  | -         | V   | 72.3                   |      |
|                 |  | 160 MHz           | 12 MHz  | -         | V   | 60.7                   |      |
|                 |  | 144 MHz           | 12 MHz  | -         | V   | 54.9                   |      |
|                 |  | 120 MHz           | 12 MHz  | -         | V   | 47.1                   |      |

Table 8.3-4 Current Consumption in Normal Run Mode (Cache-on)

| Symbol          | Conditions   | F <sub>HCLK</sub> | HXT/LXT | HIRC/LIRC | PLL | Typ                    | Unit |
|-----------------|--|-------------------|---------|-----------|-----|------------------------|------|
|                 |  |                   |         |           |     | T <sub>A</sub> = 25 °C |      |
| I <sub>DD</sub> | Normal Run, executed from SPI Flash, V <sub>DD</sub> = 3.3V, all peripherals disable                 | 192 MHz           | 12 MHz  | -         | V   | 35.5                   | mA   |
|                 |  | 160 MHz           | 12 MHz  | -         | V   | 30.3                   |      |
|                 |  | 144 MHz           | 12 MHz  | -         | V   | 27.7                   |      |
|                 |  | 120 MHz           | 12 MHz  | -         | V   | 24.8                   |      |
|                 |  | 192 MHz           | -       | 12 MHz    | V   | 35.5                   |      |
|                 |  | 160 MHz           | -       | 12 MHz    | V   | 30.3                   |      |
|                 |  | 144 MHz           | -       | 12 MHz    | V   | 27.7                   |      |
|                 |  | 120 MHz           | -       | 12 MHz    | V   | 24.8                   |      |
|                 | Normal run, External clock, executed from SPI Flash, V <sub>DD</sub> = 3.3V, all peripherals enabled | 192 MHz           | -       | 12 MHz    | V   | 57.7                   |      |
|                 |  | 160 MHz           | -       | 12 MHz    | V   | 48.9                   |      |
|                 |  | 144 MHz           | -       | 12 MHz    | V   | 44.4                   |      |
|                 |  | 120 MHz           | -       | 12 MHz    | V   | 38.6                   |      |
|                 |  | 192 MHz           | 12 MHz  | -         | V   | 57.4                   |      |
|                 |  | 160 MHz           | 12 MHz  | -         | V   | 48.5                   |      |
| 144 MHz         | 12 MHz   | -                 | V       | 44.1      |     |                        |      |
| 120 MHz         | 12 MHz   | -                 | V       | 38.4      |     |                        |      |

Table 8.3-5 Current Consumption in Normal Run Mode (Cache-off)

| Symbol          | Conditions  | F <sub>HCLK</sub> | HXT/LXT | HIRC/LIRC | PLL | Typ                    | Unit |
|-----------------|---|-------------------|---------|-----------|-----|------------------------|------|
|                 |   |                   |         |           |     | T <sub>A</sub> = 25 °C |      |
| I <sub>DD</sub> | Idle mode, executed from SPI Flash, V <sub>DD</sub> = 3.3V, all peripherals disable                 | 192 MHz           | 12 MHz  | -         | V   | 26.7                   | mA   |
|                 |   | 160 MHz           | 12 MHz  | -         | V   | 22.6                   |      |
|                 |   | 144 MHz           | 12 MHz  | -         | V   | 20.5                   |      |
|                 |   | 120 MHz           | 12 MHz  | -         | V   | 18.4                   |      |
|                 |   | 192 MHz           | -       | 12 MHz    | V   | 26.7                   |      |
|                 |   | 160 MHz           | -       | 12 MHz    | V   | 22.6                   |      |
|                 |   | 144 MHz           | -       | 12 MHz    | V   | 20.5                   |      |
|                 |   | 120 MHz           | -       | 12 MHz    | V   | 18.4                   |      |
|                 | Idle mode, External clock, executed from SPI Flash, V <sub>DD</sub> = 3.3V, all peripherals enabled | 192 MHz           | -       | 12 MHz    | V   | 51.7                   |      |
|                 |   | 160 MHz           | -       | 12 MHz    | V   | 43.5                   |      |
|                 |   | 144 MHz           | -       | 12 MHz    | V   | 39.4                   |      |
|                 |   | 120 MHz           | -       | 12 MHz    | V   | 34.1                   |      |
|                 |   | 192 MHz           | 12 MHz  | -         | V   | 51.3                   |      |
|                 |   | 160 MHz           | 12 MHz  | -         | V   | 43.1                   |      |
|                 |   | 144 MHz           | 12 MHz  | -         | V   | 39.0                   |      |
|                 |   | 120 MHz           | 12 MHz  | -         | V   | 33.7                   |      |

Table 8.3-6 Current Consumption in Idle Mode (Cache-on)

Idle Mode (CPU Keeps in Idle Mode that executed code from SPI Flash thru SPIM and SPI Flash enters the Standby by /CS pin = High)

| Symbol          | Conditions  | F <sub>HCLK</sub> | HXT/LXT | HIRC/LIRC | PLL | Typ                    | Unit |
|-----------------|---|-------------------|---------|-----------|-----|------------------------|------|
|                 |   |                   |         |           |     | T <sub>A</sub> = 25 °C |      |
| I <sub>DD</sub> | Idle mode, executed from Flash, V <sub>DD</sub> = 3.3V, all peripherals disable                 | 192 MHz           | 12 MHz  | -         | V   | 13.98                  | mA   |
|                 |   | 160 MHz           | 12 MHz  | -         | V   | 11.98                  |      |
|                 |   | 144 MHz           | 12 MHz  | -         | V   | 10.98                  |      |
|                 |   | 120 MHz           | 12 MHz  | -         | V   | 10.43                  |      |
|                 |   | 192 MHz           | -       | 12 MHz    | V   | 13.98                  |      |
|                 |   | 160 MHz           | -       | 12 MHz    | V   | 11.98                  |      |
|                 |   | 144 MHz           | -       | 12 MHz    | V   | 10.98                  |      |
|                 |   | 120 MHz           | -       | 12 MHz    | V   | 10.44                  |      |
|                 | Idle mode, External clock, executed from Flash, V <sub>DD</sub> = 3.3V, all peripherals enabled | 192 MHz           | -       | 12 MHz    | V   | 39.17                  |      |
|                 |   | 160 MHz           | -       | 12 MHz    | V   | 32.97                  |      |
|                 |   | 144 MHz           | -       | 12 MHz    | V   | 29.87                  |      |
|                 |   | 120 MHz           | -       | 12 MHz    | V   | 26.16                  |      |
|                 |   | 192 MHz           | 12 MHz  | -         | V   | 38.71                  |      |
|                 |   | 160 MHz           | 12 MHz  | -         | V   | 32.49                  |      |
|                 |   | 144 MHz           | 12 MHz  | -         | V   | 29.41                  |      |
|                 |   | 120 MHz           | 12 MHz  | -         | V   | 25.68                  |      |

Table 8.3-7 Current Consumption in Idle Mode (Cache-off)



Power-down Mode (CPU runs the Power-down Mode that executed code from embedded Flash after SPI Flash entered the power-down by the Power-down command (B9h))

| Symbol                | Conditions   | LXT | LIRC | PLL | Typ                    | Unit |
|-----------------------|--|-----|------|-----|------------------------|------|
|                       |  |     |      |     | T <sub>A</sub> = 25 °C |      |
| I <sub>DD_FWPD</sub>  | Fast wake-up Power-down mode, V <sub>DD</sub> = 3.3V, all peripherals disabled             | -   | -    | -   | 0.49                   | mA   |
|                       | Fast wake-up Power-down mode, V <sub>DD</sub> = 3.3V, RTC/WDT/Timer/UART enable            | V   | -    | -   | 0.49                   |      |
|                       | Fast wake-up Power-down mode, V <sub>DD</sub> = 3.3V, RTC/WDT/Timer enable                 | -   | V    | -   | 0.49                   |      |
|                       | Fast wake-up Power-down mode, V <sub>DD</sub> = 3.3V, WDT/Timer use LIRC, RTC/UART use LXT | V   | V    | -   | 0.49                   |      |
| I <sub>DD_PD</sub>    | Power-down mode, V <sub>DD</sub> = 3.3V, all peripherals disabled                          | -   | -    | -   | 0.37                   | mA   |
|                       | Power-down mode, V <sub>DD</sub> = 3.3V, RTC/WDT/Timer/UART enable                         | V   | -    | -   | 0.37                   |      |
|                       | Power-down mode, V <sub>DD</sub> = 3.3V, RTC/WDT/Timer use LIRCT                           | -   | V    | -   | 0.37                   |      |
|                       | Power-down mode, V <sub>DD</sub> = 3.3V, WDT/Timer use LIRC, RTC/UART use LX               | V   | V    | -   | 0.37                   |      |
| I <sub>DD_LLDPD</sub> | Low leakage Power-down mode, V <sub>DD</sub> = 3.3V, all peripherals disabled              | -   | -    | -   | 0.14                   | mA   |
|                       | Low leakage Power-down mode, V <sub>DD</sub> = 3.3V, RTC/WDT/Timer/UART enable             | V   | -    | -   | 0.37                   |      |
|                       | Low leakage Power-down mode, V <sub>DD</sub> = 3.3V, RTC/WDT/Timer enable                  | -   | V    | -   | 0.37                   |      |
|                       | Low leakage Power-down mode, V <sub>DD</sub> = 3.3V, WDT/Timer use LIRC, RTC/UART use LX   | V   | V    | -   | 0.37                   |      |
| I <sub>DD_SPD0</sub>  | Standby Power-down mode (SPD0), V <sub>DD</sub> = 3.3V, all peripherals disabled           | -   | -    | -   | 0.04                   | mA   |
|                       | Standby Power-down mode (SPD0), V <sub>DD</sub> = 3.3V, RTC enable                         | V   | -    | -   | 0.04                   |      |
|                       | Standby Power-down mode (SPD0), V <sub>DD</sub> = 3.3V, RTC enable                         | -   | V    | -   | 0.04                   |      |

| Symbol   | Conditions   | LXT | LIRC | PLL | Typ                    | Unit |
|--|--|-----|------|-----|------------------------|------|
|  |  |     |      |     | T <sub>A</sub> = 25 °C |      |
| I <sub>DD_SPD1</sub>   | Standby Power-down mode (SPD1), V <sub>DD</sub> = 3.3V, all peripherals disabled | -   | -    | -   | 0.04                   | mA   |
|  | Standby Power-down mode (SPD1), V <sub>DD</sub> = 3.3V, RTC enable               | V   | -    | -   | 0.04                   |      |
|  | Standby Power-down mode (SPD1), V <sub>DD</sub> = 3.3V, RTC enable               | -   | V    | -   | 0.04                   |      |
| <b>Note:</b>   |  |     |      |     |                        |      |
| 1. V <sub>DD</sub> = AV <sub>DD</sub> = V <sub>DDIO</sub> = 3.3V |  |     |      |     |                        |      |

Table 8.3-8 Chip Current Consumption in Power-down Mode

**8.3.3 On-chip Peripheral Current Consumption**

- ALL GPIO pins are in push pull mode, output high.
- LDO = 1.26V
- The typical values for TA= 25 °C and V<sub>DD</sub> = AV<sub>DD</sub> = 3.3 V unless otherwise specified.
- When the peripherals are enabled HCLK is the system clock, f<sub>HCLK</sub> = 192 MHz, f<sub>PCLK0,1</sub> = f<sub>HCLK</sub>/2.

| Peripheral        | I <sub>DD</sub> | Unit |
|-------------------|-----------------|------|
| DAC               | 58.4            | uA   |
| ADC               | 338.6           |      |
| ACMP01            | 85.2            |      |
| OPA               | 123.3           |      |
| QEI0              | 74.2            |      |
| QEI1              | 81.9            |      |
| ECAP0             | 74.3            |      |
| ECAP1             | 69.8            |      |
| EPWM0             | 907             |      |
| EPWM1             | 896.5           |      |
| BPWM0             | 263.8           |      |
| BPWM1             | 245.2           |      |
| WDT               | 49.6            |      |
| SD0               | 1416.1          |      |
| SD1               | 1263.6          |      |
| SC0               | 66.6            |      |
| SC1               | 76.6            |      |
| SC2               | 73.6            |      |
| I <sup>2</sup> S0 | 102.1           |      |
| SPIM              | 14681.1         |      |
| QSPI0             | 291.1           |      |
| SPI0              | 315.5           |      |
| SPI1              | 261.2           |      |
| SPI2              | 137.2           |      |
| SPI3              | 138.7           |      |
| UART0             | 150.6           |      |
| UART1             | 209.1           |      |
| UART2             | 220.0           |      |

| Peripheral   | I <sub>DD</sub> | Unit |
|--|-----------------|------|
| UART3  | 160.5           |      |
| UART4  | 186.5           |      |
| UART5  | 177.5           |      |
| I <sup>2</sup> C0  | 34.4            |      |
| I <sup>2</sup> C1  | 26.6            |      |
| I <sup>2</sup> C2  | 32.7            |      |
| CAN0   | 280.5           |      |
| CAN1   | 257.6           |      |
| USCI0  | 211.9           |      |
| USCI1  | 205.4           |      |
| EBI  | 209.6           |      |
| TMR0   | 140.5           |      |
| TMR1   | 130.1           |      |
| TMR2   | 127.1           |      |
| TMR3   | 121.2           |      |
| USB HS OTG   | 248.7           |      |
| USB FS OTG   | 503.1           |      |
| Crypto   | 1550.4          |      |
| EMAC   | 1768.1          |      |
| <b>Note:</b>   |                 |      |
| 1. Guaranteed by characterization results, not tested in production. |                 |      |

**8.3.4 Wakeup Time**

- The wakeup times given in Table 8.3-9 is measured on a wakeup phase with a 12 MHz HIRC oscillator. The clock source used to wake up the device depends from the current operating mode:
  - Fast-wakeup, power down, low leakage Power-down mode: the clock source is the RC oscillator
  - Standby and Deep Power-down mode: the clock source is the clock that was set before entering Sleep mode.
- The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
- The clock source is the RC oscillator from HIRC

| Symbol         | Parameter                                    | Typ      | Unit |
|----------------|--|----------|------|
| $t_{WU\_IDLE}$ | Wakeup from IDLE mode                        | 5 Cycles | μs   |
| $t_{WU\_FWPD}$ | Wakeup from Fast-wakeup power down mode      | 6        |      |
| $t_{WU\_NPD}$  | Wakeup from normal power down mode           | 12       |      |
| $t_{WU\_LLPD}$ | Wakeup from low leakage power down mode      | 54       |      |
| $t_{WU\_SPD0}$ | Wakeup from Standby Power-down mode 0 (SPD0) | 527      |      |
| $t_{WU\_SPD1}$ | Wakeup from Standby Power-down mode 1 (SPD1) | 527      |      |
| $t_{WU\_DPD}$  | Deep Power-down mode (DPD)                   | 489      |      |

Table 8.3-9 Low-power Mode Wakeup Timings

8.3.5 PIN DC Characteristics

| Symbol           | Parameter                             | Min.                | Typ.               | Max.                | Unit | Test Conditions   |
|------------------|---------------------------------------|---------------------|--------------------|---------------------|------|---|
| V <sub>IL1</sub> | Input Low Voltage (TTL input)         |                     |                    | 0.8                 | V    | V <sub>DD</sub> = V <sub>DDIO</sub> = 3.6 V   |
|                  |                                       |                     |                    | 0.56                | V    | V <sub>DD</sub> = V <sub>DDIO</sub> = 1.8 V   |
| V <sub>IH1</sub> | Input High Voltage (TTL input)        | 2                   |                    |                     | V    | V <sub>DD</sub> = V <sub>DDIO</sub> = 3.6V  |
|                  |                                       | 1.04                |                    |                     | V    | V <sub>DD</sub> = V <sub>DDIO</sub> = 1.8V  |
| V <sub>IL2</sub> | Input Low Voltage (Schmitt input)     |                     |                    | 0.3*V <sub>DD</sub> | V    | V <sub>DD</sub> = V <sub>DDIO</sub> = 3.6V  |
|                  |                                       |                     |                    | 0.3*V <sub>DD</sub> |      | V <sub>DD</sub> = V <sub>DDIO</sub> = 1.8V  |
| V <sub>IH2</sub> | Input High Voltage (Schmitt input)    | 0.7*V <sub>DD</sub> |                    |                     | V    | V <sub>DD</sub> = V <sub>DDIO</sub> = 3.6V  |
|                  |                                       | 0.7*V <sub>DD</sub> |                    |                     |      | V <sub>DD</sub> = V <sub>DDIO</sub> = 1.8V  |
| V <sub>HY</sub>  | Hysteresis voltage of (Schmitt input) |                     | 0.2V <sub>DD</sub> |                     | V    |   |
| I <sub>LK</sub>  | Input Leakage Current                 | -1                  |                    | 1                   | μA   | V <sub>DD</sub> = V <sub>DDIO</sub> = 3.6V, 0 < V <sub>IN</sub> < V <sub>DD</sub> , Open-drain or input only mode |
| R <sub>PU</sub>  | Input Pull Up Resistor                |                     | 50                 |                     | KΩ   | V <sub>DD</sub> = V <sub>DDIO</sub> = 3.3V  |
|                  |                                       |                     | 52                 |                     | KΩ   | V <sub>DD</sub> = V <sub>DDIO</sub> = 1.8V  |
| R <sub>PD</sub>  | Input Pull down Resistor              |                     | 50                 |                     | KΩ   | V <sub>DD</sub> = V <sub>DDIO</sub> = 3.3V  |
|                  |                                       |                     | 52                 |                     | KΩ   | V <sub>DD</sub> = V <sub>DDIO</sub> = 1.8V  |

Table 8.3-10 PIN Input Characteristics

| Symbol           | Parameter   | Min. | Typ. | Max. | Unit | Test Conditions                            |
|------------------|---|------|------|------|------|--|
| I <sub>SR4</sub> | Source Current  |      | -18  |      | mA   | V <sub>DD</sub> = V <sub>DDIO</sub> = 3.3V |
| I <sub>SR5</sub> | (Push-pull Mode, Set GPIO to output HIGH, Apply GPIO pin V <sub>IN</sub> =(V <sub>DD</sub> -0.4)V for V <sub>DD</sub> and measure the source current) |      | -10  |      | mA   | V <sub>DD</sub> = V <sub>DDIO</sub> = 1.8V |
| I <sub>SK1</sub> | Sink Current  |      | 17   |      | mA   | V <sub>DD</sub> = V <sub>DDIO</sub> = 3.3V |
| I <sub>SK2</sub> | (Push-pull Mode, Set GPIO to output LOW, Apply GPIO pin V <sub>IN</sub> =(V <sub>SS</sub> +0.4)V for V <sub>SS</sub> and measure the source current)  |      | 10   |      | mA   | V <sub>DD</sub> = V <sub>DDIO</sub> = 1.8V |
| C <sub>I/O</sub> | I/O pin capacitance   |      | 5    |      | pF   |  |

Table 8.3-11 PIN Output Characteristics

| Symbol    | Parameter   | Min.               | Typ. | Max.               | Unit       | Test Conditions  |
|-----------|---|--------------------|------|--------------------|------------|------------------|
| $V_{ILR}$ | Negative going threshold (Schmitt input), nRESET  |                    |      | $0.3 \cdot V_{DD}$ | V          | $V_{DD} = 3.3V$  |
| $V_{IHR}$ | Positive going threshold (Schmitt Input), nRESET  | $0.7 \cdot V_{DD}$ |      |                    | V          | $V_{DD} = 3.3V$  |
| $R_{RST}$ | Internal nRESET pin pull up resistor              |                    | 50   |                    | K $\Omega$ |                  |
| $t_{FR1}$ | nRESET input filtered time                        |                    | 32   |                    | $\mu S$    |                  |
| $t_{FR2}$ | nRESET input filtered time under SPD and DPD mode |                    | 300  |                    | nS         | $V_{DD} = 3.3V,$ |

Table 8.3-12 nRESET PIN Characteristics

### 8.4 AC Electrical Characteristics

#### 8.4.1 External 4~24 MHz High Speed Crystal (HXT) Characteristics

- $T_A = 25\text{ }^\circ\text{C}$  and  $V_{DD} = 3.3\text{ V}$  unless otherwise specified.

| Sym.           | Parameter                                 | Specifications |      |      |                  | Test Condition                      |
|----------------|---|----------------|------|------|------------------|-------------------------------------|
|                |   | Min.           | Typ. | Max. | Unit             |                                     |
| $V_{DD}$       | Operating Voltage                         | 1.8            |      | 3.6  | V                |                                     |
| $R_f$          | Feedback resister                         |                | 1000 |      | k $\Omega$       |                                     |
| $f_{HXT}$      | Oscillator frequency                      | 4              |      | 24   | MHz              | $V_{DD} = 1.8 \sim 3.6\text{V}$     |
| $T_{HXT}$      | Temperature Range                         | -40            |      | 105  | $^\circ\text{C}$ |                                     |
| $I_{HXT\_INV}$ | Current Consumption<br>(INV-type Crystal) |                | 650  |      | $\mu\text{A}$    | 4 MHz                               |
|                |   |                | 1600 |      |                  | 12 MHz                              |
|                |   |                | 2000 |      |                  | 16 MHz                              |
|                |   |                | 4000 |      |                  | 24 MHz                              |
| $I_{HXT\_GM}$  | Current Consumption<br>(GM-type Crystal)  |                | 160  |      | $\mu\text{A}$    | 4 MHz                               |
|                |   |                | 280  |      |                  | 12 MHz                              |
|                |   |                | 400  |      |                  | 16 MHz                              |
|                |   |                | 600  |      |                  | 24 MHz                              |
| $T_{S\_GM}$    | Stable time (GM-type)                     | 1545           |      | 1752 | $\mu\text{s}$    | 4 MHz, $-40\text{ }^\circ\text{C}$  |
|                |   | 1630           |      | 1757 |                  | 4 MHz, $25\text{ }^\circ\text{C}$   |
|                |   | 1054           |      | 1988 |                  | 4 MHz, $105\text{ }^\circ\text{C}$  |
|                |   | 484            |      | 512  |                  | 12 MHz, $-40\text{ }^\circ\text{C}$ |
|                |   | 484            |      | 544  |                  | 12 MHz, $25\text{ }^\circ\text{C}$  |
|                |   | 386            |      | 606  |                  | 12 MHz, $105\text{ }^\circ\text{C}$ |
|                |   | 349            |      | 375  |                  | 16 MHz, $-40\text{ }^\circ\text{C}$ |
|                |   | 337            |      | 399  |                  | 16 MHz, $25\text{ }^\circ\text{C}$  |
|                |   | 281            |      | 444  |                  | 16 MHz, $105\text{ }^\circ\text{C}$ |
|                |   | 259            |      | 303  |                  | 24 MHz, $-40\text{ }^\circ\text{C}$ |
|                |   | 248            |      | 330  |                  | 24 MHz, $25\text{ }^\circ\text{C}$  |
|                |   | 210            |      | 403  |                  | 24 MHz, $105\text{ }^\circ\text{C}$ |



| Sym.               | Parameter              | Specifications |            |       |      | Test Condition |
|--------------------|------------------------|----------------|------------|-------|------|----------------|
|                    |                        | Min.           | Typ.       | Max.  | Unit |                |
| T <sub>S_INV</sub> | Stable time (INV-type) | 1490           |            | 23432 | μs   | 4 MHz, -40 °C  |
|                    |                        | 1479           |            | 2352  |      | 4 MHz, 25 °C   |
|                    |                        | 1052           |            | 2105  |      | 4 MHz, 105 °C  |
|                    |                        | 464            |            | 558   |      | 12 MHz, -40 °C |
|                    |                        | 481            |            | 554   |      | 12 MHz, 25 °C  |
|                    |                        | 417            |            | 663   |      | 12 MHz, 105 °C |
|                    |                        | 317            |            | 420   |      | 16 MHz, -40 °C |
|                    |                        | 326            |            | 407   |      | 16 MHz, 25 °C  |
|                    |                        | 290            |            | 472   |      | 16 MHz, 105 °C |
|                    |                        | 226            |            | 382   |      | 24 MHz, -40 °C |
|                    |                        | 228            |            | 388   |      | 24 MHz, 25 °C  |
|                    |                        | 210            |            | 441   |      | 24 MHz, 105 °C |
|                    |                        |                | Clock Duty | 45    |      | 50             |

**Note:**

1. Guaranteed by characterization, not tested in production.
2. Recommended crystal resonators for the HXT oscillator in M480 Series MCUs
  - 2.1 EPSON FA-238A 12MHz (C<sub>L</sub>=12pF, ESR= 120 Ω), X1E000341000400
  - 2.2 EPSON FA-238A 16MHz (C<sub>L</sub>=12pF, ESR= 80 Ω), X1E000341003900
  - 2.3 EPSON FA-238A 24MHz (C<sub>L</sub>=12pF, ESR= 60 Ω), X1E000341014800

Table 8.4-1 External 4~24 MHz High Speed Crystal (HXT) Oscillator

8.4.1.1 Typical Crystal Application Circuits

| Crystal        | C1   | C2   | R       |
|----------------|------|------|---------|
| 4 MHz ~ 24 MHz | 20pF | 20pF | without |

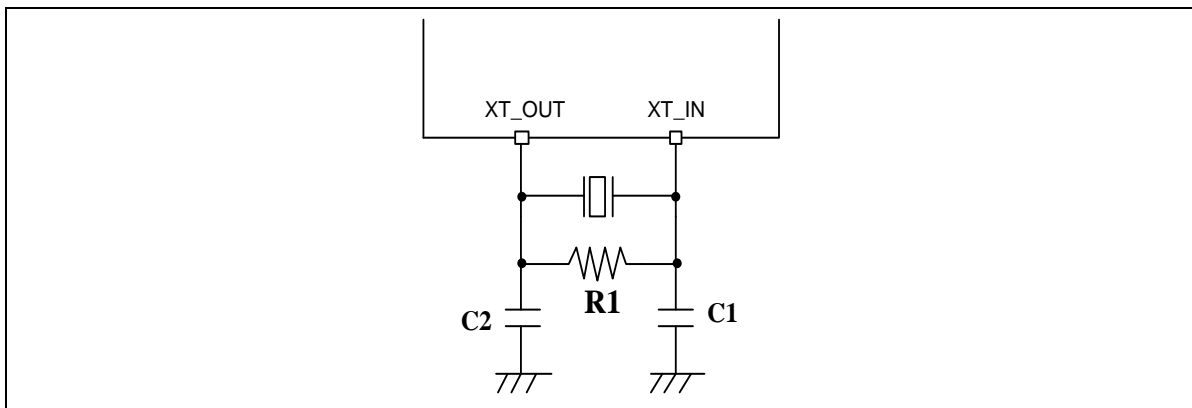


Figure 8-9 Typical Crystal Application Circuit

8.4.2 External 4~24 MHz High Speed Clock Input (OSC) Characteristics

| Sym.       | Parameter          | Specifications     |      |                    |      | Test Condition |
|------------|--------------------|--------------------|------|--------------------|------|----------------|
|            |                    | Min.               | Typ. | Max.               | Unit |                |
| $t_{CHCX}$ | Clock High Time    | 18                 |      |                    | nS   |                |
| $t_{CLCX}$ | Clock Low Time     | 18                 |      |                    | nS   |                |
| $t_{CLCH}$ | Clock Rise Time    |                    |      | 10                 | nS   |                |
| $t_{CHCL}$ | Clock Fall Time    |                    |      | 10                 | nS   |                |
| $V_{IH}$   | Input High Voltage | $0.7 \cdot V_{DD}$ |      |                    | V    |                |
| $V_{IL}$   | Input Low Voltage  |                    |      | $0.3 \cdot V_{DD}$ | V    |                |

**Note:**

1. Guaranteed by design, not tested in production
2. Duty cycle is 50%.

8.4.3 External 32.768 kHz Low Speed Crystal (LXT) Characteristics

| Sym.      | Parameter            | Specifications |        |      |              | Test Condition            |
|-----------|----------------------|----------------|--------|------|--------------|---------------------------|
|           |                      | Min.           | Typ.   | Max. | Unit         |                           |
| $V_{DD}$  | Operation Voltage    | 1.8            |        | 3.6  | V            |                           |
| $f_{LXT}$ | Oscillator frequency |                | 32.768 |      | kHz          | $V_{DD} = 1.8 \sim 3.6$ V |
| $T_{LXT}$ | Temperature          | -40            |        | 105  | $^{\circ}$ C |                           |
| $I_{LXT}$ | Operating current    |                |        | 0.5  | $\mu$ A      | $V_{DD} = 3.3$ V          |
|           | Duty cycle           | 45             |        | 55   | %            |                           |
| $T_S$     | Stable Time          |                |        | 500  | ms           |                           |

**Note:**

1. Guaranteed by characterization, not tested in production.
2. Recommended crystal resonators for the LXT oscillator in M480 Series MCUs
  - 2.1 EPSON FC-13A 32.768 kHz ( $C_L = 12.5$  pF, ESR=70 k $\Omega$ ), X1A000091000100

Table 8.4-2 External 32.768 kHz Crystal

8.4.3.1 Typical Crystal Application Circuits

| Crystal    | C1   | C2   | R1      |
|------------|------|------|---------|
| 32.768 kHz | 20pF | 20pF | without |

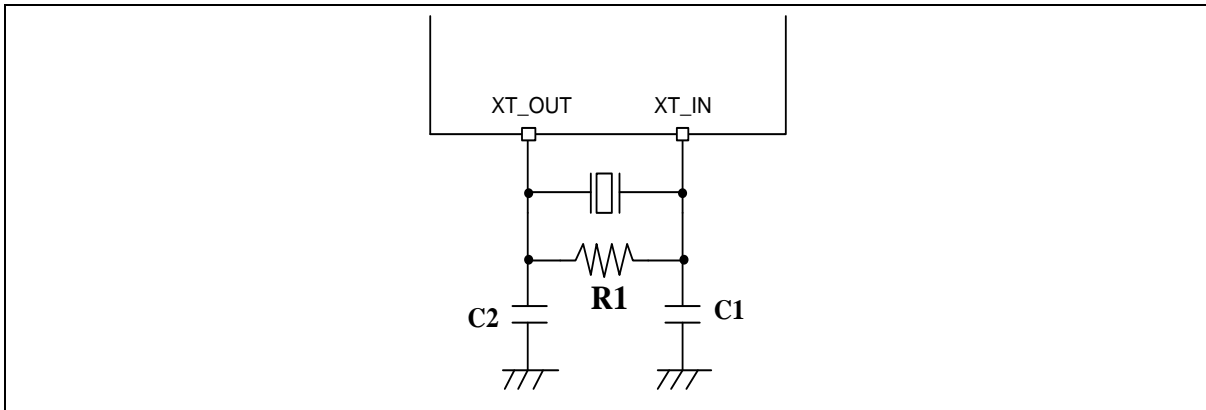
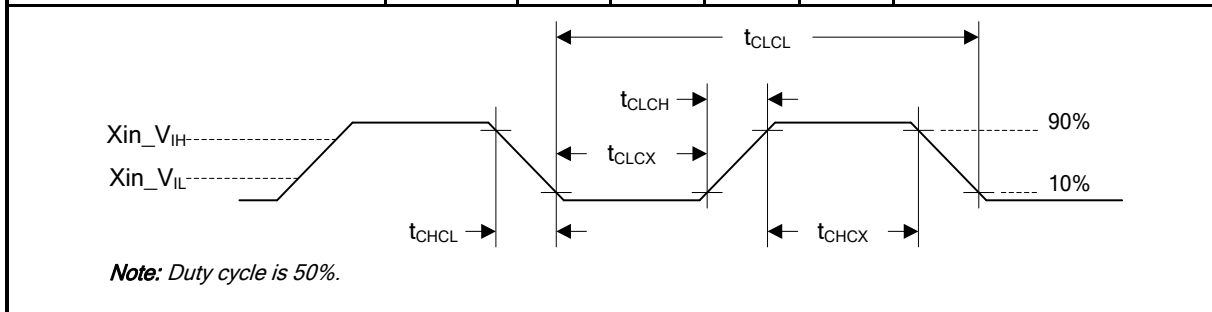


Figure 8-10 Typical Crystal Application Circuit

8.4.4 External 32.768 kHz Low Speed Clock Input (OSC) Characteristics

| Parameter                        | Sym.       | Specifications     |      |                    |      | Test Condition |
|----------------------------------|------------|--------------------|------|--------------------|------|----------------|
|                                  |            | Min.               | Typ. | Max.               | Unit |                |
| Clock High Time                  | $t_{CHCX}$ | 450                | -    | -                  | nS   |                |
| Clock Low Time                   | $t_{CLCX}$ | 450                | -    | -                  | nS   |                |
| Clock Rise Time                  | $t_{CLCH}$ |                    | -    | 50                 | nS   |                |
| Clock Fall Time                  | $t_{CHCL}$ |                    | -    | 50                 | nS   |                |
| LXT Input Pin Input High Voltage | $Xin\_VIH$ | $0.7 \cdot V_{DD}$ |      |                    | V    |                |
| LXT Input Pin Input Low Voltage  | $Xin\_VIL$ |                    |      | $0.3 \cdot V_{DD}$ | V    |                |



8.4.5 12 MHz Internal High Speed RC Oscillator (HIRC)

| Sym.  | Parameter                         | Specifications |      |      |      | Test Condition                                    |
|---|-----------------------------------|----------------|------|------|------|---|
|   |                                   | Min.           | Typ. | Max. | Unit |   |
| V <sub>HRC</sub>  | Supply voltage                    | 1.8            |      | 3.6  | V    |   |
| f <sub>HRC</sub>  | Center Frequency                  |                | 12   |      | MHz  |   |
|   | Internal Oscillator Frequency[*1] | -1             |      | 1    | %    | T <sub>A</sub> = 25 °C,<br>V <sub>DD</sub> = 3.3V |
|   |                                   | -3             |      | 3    | %    | -40°C ~ +105 °C,<br>V <sub>DD</sub> = 1.8 ~ 3.6V  |
| I <sub>HRC</sub>  | Operating current                 |                | 155  |      | μA   |   |
| T <sub>S</sub>  | Stable time                       |                |      | 4    | us   |   |
| <b>Note:</b>  |                                   |                |      |      |      |   |
| 1. Guaranteed by characterization, not tested in production |                                   |                |      |      |      |   |

8.4.6 10 kHz Internal Low Speed RC Oscillator (LIRC)

| Sym.  | Parameter                | Specifications |      |      |      | Test Condition  |
|---|--------------------------|----------------|------|------|------|---|
|   |                          | Min.           | Typ. | Max. | Unit |   |
| V <sub>LRC</sub>  | Supply voltage           | 1.8            |      | 3.6  | V    |   |
| F <sub>LRC</sub>  | Oscillator Frequency[*1] | 5              |      | 20   | kHz  | V <sub>DD</sub> =1.8V~3.6V, T <sub>A</sub> =-40~105°C |
| I <sub>LRC</sub>  | Operating current        |                |      | 0.5  | μA   | V <sub>DD</sub> = 3.3V                                |
| T <sub>S</sub>  | Stable time              |                | 200  |      | μs   |   |
| <b>Note:</b>  |                          |                |      |      |      |   |
| 1. Guaranteed by characterization, not tested in production |                          |                |      |      |      |   |

8.4.7 PLL Characteristics

| Symbol  | Parameter                   | Conditions                    | Min | Typ | Max | Unit |
|---|-----------------------------|-------------------------------|-----|-----|-----|------|
| f <sub>PLL_IN</sub>   | PLL input clock             |                               | 4   |     | 24  | MHz  |
| f <sub>PLL_OUT</sub>  | PLL multiplier output clock |                               | 50  |     | 480 | MHz  |
| T <sub>S</sub>  | PLL stable time[*1]         |                               | 100 |     | 200 | μs   |
| Jitter  | Cycle-to-cycle Jitter[*2]   | Peak to peak @ 480M           |     | 250 |     | ps   |
| I <sub>DD</sub>   | Power consumption           | V <sub>DD</sub> =3.3V@500 MHz |     |     | 3   | mA   |
| <b>Note:</b>  |                             |                               |     |     |     |      |
| 1. Guaranteed by characterization, not tested in production |                             |                               |     |     |     |      |

8.4.8 PIN AC Characteristics

- $C_L = 51 \text{ pF}$

| Px_SLEWCTL | Symbol                        | Parameter                                   | Conditions               | Typ   | Unit |
|------------|-------------------------------|---|--------------------------|-------|------|
| 00         | $t_f(\text{IO})_{\text{out}}$ | Output high to low level fall time (90~10%) | $V_{DD} = 3.6 \text{ V}$ | 4.384 | ns   |
|            |                               |   | $V_{DD} = 1.8 \text{ V}$ | 8.532 |      |
|            | $t_r(\text{IO})_{\text{out}}$ | output low to high level rise time (10~90%) | $V_{DD} = 3.6 \text{ V}$ | 4.086 |      |
|            |                               |   | $V_{DD} = 1.8 \text{ V}$ | 8.225 |      |
| 01         | $t_f(\text{IO})_{\text{out}}$ | Output high to low level fall time (90~10%) | $V_{DD} = 3.6 \text{ V}$ | 3.005 |      |
|            |                               |   | $V_{DD} = 1.8 \text{ V}$ | 6.153 |      |
|            | $t_r(\text{IO})_{\text{out}}$ | output low to high level rise time (10~90%) | $V_{DD} = 3.6 \text{ V}$ | 3.404 |      |
|            |                               |   | $V_{DD} = 1.8 \text{ V}$ | 6.29  |      |
| 10         | $t_f(\text{IO})_{\text{out}}$ | Output high to low level fall time (90~10%) | $V_{DD} = 3.6 \text{ V}$ | 3.054 |      |
|            |                               |   | $V_{DD} = 1.8 \text{ V}$ | 6.152 |      |
|            | $t_r(\text{IO})_{\text{out}}$ | output low to high level rise time (10~90%) | $V_{DD} = 3.6 \text{ V}$ | 3.389 |      |
|            |                               |   | $V_{DD} = 1.8 \text{ V}$ | 6.269 |      |

Table 8.4-3 I/O AC Characteristics

## 8.5 Analog Electrical Characteristics

### 8.5.1 LDO

| Symbol           | Parameter       | Min | Typ  | Max | Unit | Test Condition |
|------------------|-----------------|-----|------|-----|------|----------------|
| V <sub>DD</sub>  | DC Power Supply | 1.8 |      | 3.6 | V    |                |
| V <sub>LDO</sub> | Output Voltage  |     | 1.26 |     | V    |                |
| T <sub>A</sub>   | Temperature     | -40 |      | 105 | °C   |                |

**Note:**

1. It is recommended a 0.1μF bypass capacitor is connected between V<sub>DD</sub> and the closest VSS pin of the device.
2. For ensuring power stability, a 2.2μF capacitor must be connected between LDO\_CAP pin and the closest VSS pin of the device.

### 8.5.2 Low-Voltage Reset

| Symbol           | Parameter         | Min  | Typ  | Max  | Unit | Test Condition           |
|------------------|-------------------|------|------|------|------|--------------------------|
| AV <sub>DD</sub> | Supply Voltage    | 0    |      | 3.6  | V    |                          |
| T <sub>A</sub>   | Temperature       | -40  |      | 105  | °C   | -                        |
| I <sub>LVR</sub> | Operating Current |      | 0.5  |      | uA   | AV <sub>DD</sub> = 3.6V  |
| V <sub>LVR</sub> | Threshold Voltage | 1.40 | 1.48 | 1.56 | V    | T <sub>A</sub> = 105 ° C |
|                  |                   | 1.40 | 1.48 | 1.56 | V    | T <sub>A</sub> = 25 ° C  |
|                  |                   | 1.40 | 1.48 | 1.56 | V    | T <sub>A</sub> = -40 ° C |

8.5.3 Brown-out Detector

| Symbol        | Parameter                           | Min | Typ | Max | Unit | Test Condition    |
|---------------|-------------------------------------|-----|-----|-----|------|-------------------|
| $V_{DD}$      | Supply Voltage                      | 0   |     | 3.6 | V    | -                 |
| $T_A$         | Temperature                         | -40 |     | 105 | °C   | -                 |
| $I_{BOD}$     | Operating Current                   |     | 66  |     | uA   | $V_{DD} = 3.6V$   |
| $V_{BOD\_F}$  | Brown-out Voltage<br>(Falling edge) | 2.9 | 3.0 | 3.1 | V    | BODVL [2:0] = 111 |
|               |                                     | 2.7 | 2.8 | 2.9 | V    | BODVL [2:0] = 110 |
|               |                                     | 2.5 | 2.6 | 2.7 | V    | BODVL [2:0] = 101 |
|               |                                     | 2.3 | 2.4 | 2.5 | V    | BODVL [2:0] = 100 |
|               |                                     | 2.1 | 2.2 | 2.3 | V    | BODVL [2:0] = 011 |
|               |                                     | 1.9 | 2.0 | 2.1 | V    | BODVL [2:0] = 010 |
|               |                                     | 1.7 | 1.8 | 1.9 | V    | BODVL [2:0] = 001 |
|               |                                     | 1.5 | 1.6 | 1.7 | V    | BODVL [2:0] = 000 |
| $V_{BOD\_R}$  | Brown-out Voltage<br>(Rising edge)  | 3.0 | 3.1 | 3.2 | V    | BODVL [2:0] = 111 |
|               |                                     | 2.8 | 2.9 | 3.0 | V    | BODVL [2:0] = 110 |
|               |                                     | 2.6 | 2.7 | 2.8 | V    | BODVL [2:0] = 101 |
|               |                                     | 2.4 | 2.5 | 2.6 | V    | BODVL [2:0] = 100 |
|               |                                     | 2.2 | 2.3 | 2.4 | V    | BODVL [2:0] = 011 |
|               |                                     | 2.0 | 2.1 | 2.2 | V    | BODVL [2:0] = 010 |
|               |                                     | 1.8 | 1.9 | 2.0 | V    | BODVL [2:0] = 001 |
|               |                                     | 1.6 | 1.7 | 1.8 | V    | BODVL [2:0] = 000 |
| $T_{BOD\_RE}$ | Respond Time                        |     | 1   |     | ms   | Respond Time      |

8.5.4 Power-on Reset

| Symbol     | Parameter  | Min | Typ  | Max  | Unit | Test Condition |
|------------|--|-----|------|------|------|----------------|
| $T_A$      | Temperature  | -40 | -    | +105 | °C   | -              |
| $V_{POR}$  | Reset Voltage                                      |     | 1.47 |      | V    | -              |
| $RRV_{DD}$ | $V_{DD}$ Raising Rate to Ensure Power-on Reset[*1] | 10  |      |      | us/V |                |
| $FRV_{DD}$ | $V_{DD}$ Falling Rate to Ensure Power-on Reset[*1] | 320 |      |      | us/V |                |

Note:

1. Guaranteed by characterization, not tested in production

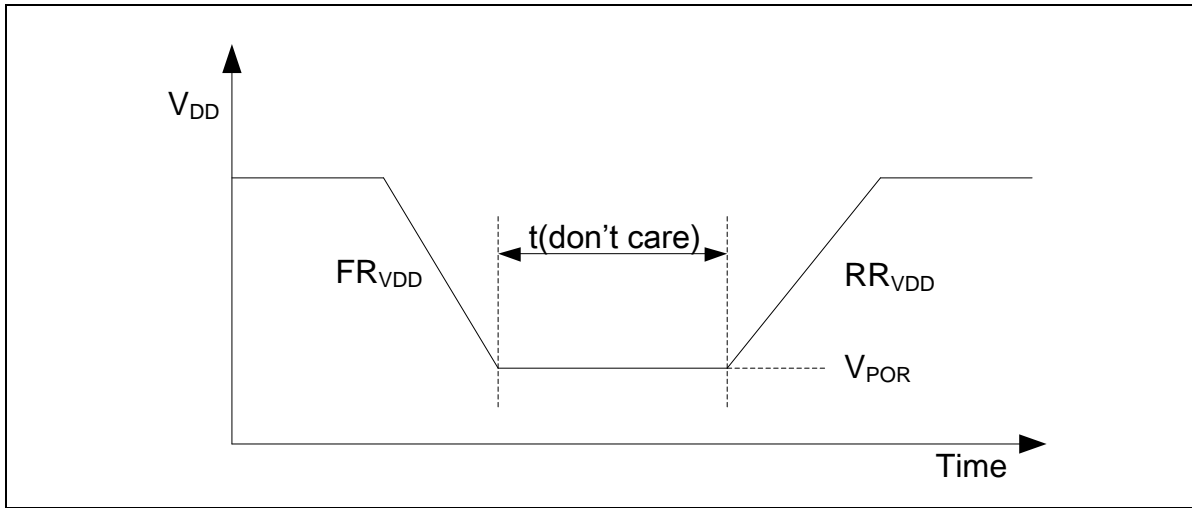


Figure 8-11 Power-up Ramp Condition

8.5.5 Internal Voltage Reference

- The maximum values are obtained for  $V_{DD} = 3.6\text{ V}$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25\text{ }^\circ\text{C}$  and  $V_{DD} = 3.3\text{ V}$  unless otherwise specified.

| Symbol  | Parameter                  | Min | Typ | Max | Unit | Comments   |
|---|----------------------------|-----|-----|-----|------|--|
| $V_{REF\_INT}$  | Internal reference voltage |     | 1.6 |     | V    |  |
|   |                            |     | 2.0 |     |      |  |
|   |                            |     | 2.5 |     |      |  |
|   |                            |     | 3.0 |     |      |  |
| $AV_{DD\_min}$  | $AV_{DD}$ minimum voltage  | 2   |     |     | V    | $V_{REF\_OUT} = 1.6\text{ v}$                        |
|   |                            | 2.2 |     |     |      | $V_{REF\_OUT} = 2.0\text{ v}$                        |
|   |                            | 2.7 |     |     |      | $V_{REF\_OUT} = 2.5\text{ v}$                        |
|   |                            | 3.2 |     |     |      | $V_{REF\_OUT} = 3.0\text{ v}$                        |
| $T_s$   | Stable time                |     | 0.7 | 2   | ms   | $C_L = 4.7\text{ }\mu\text{F}$ , $V_{REF}$ initial=0 |
|   |                            |     | 35  | 48  | us   | $C_L = 0.1\text{ }\mu\text{F}$ , $V_{REF}$ initial=0 |
| <b>Note:</b>  |                            |     |     |     |      |  |
| 1. Guaranteed by characterization, not tested in production |                            |     |     |     |      |  |



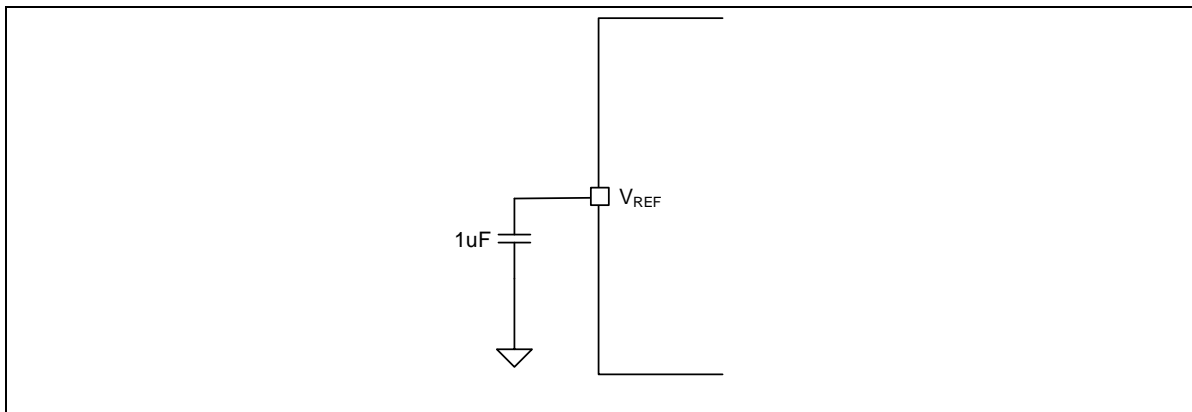


Figure 8-12 Typical Connection with Internal Voltage Reference

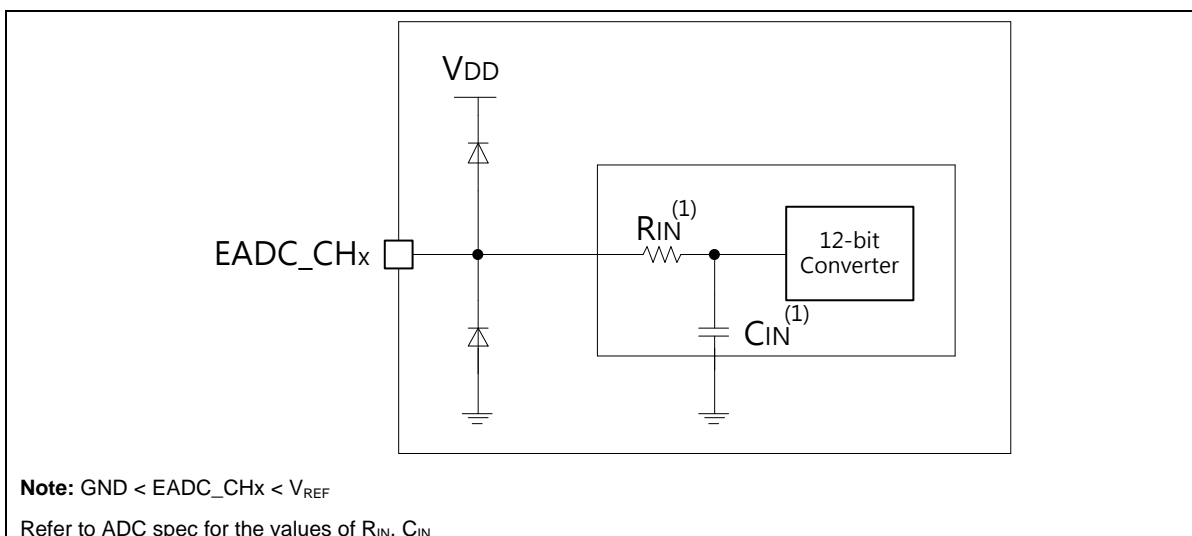
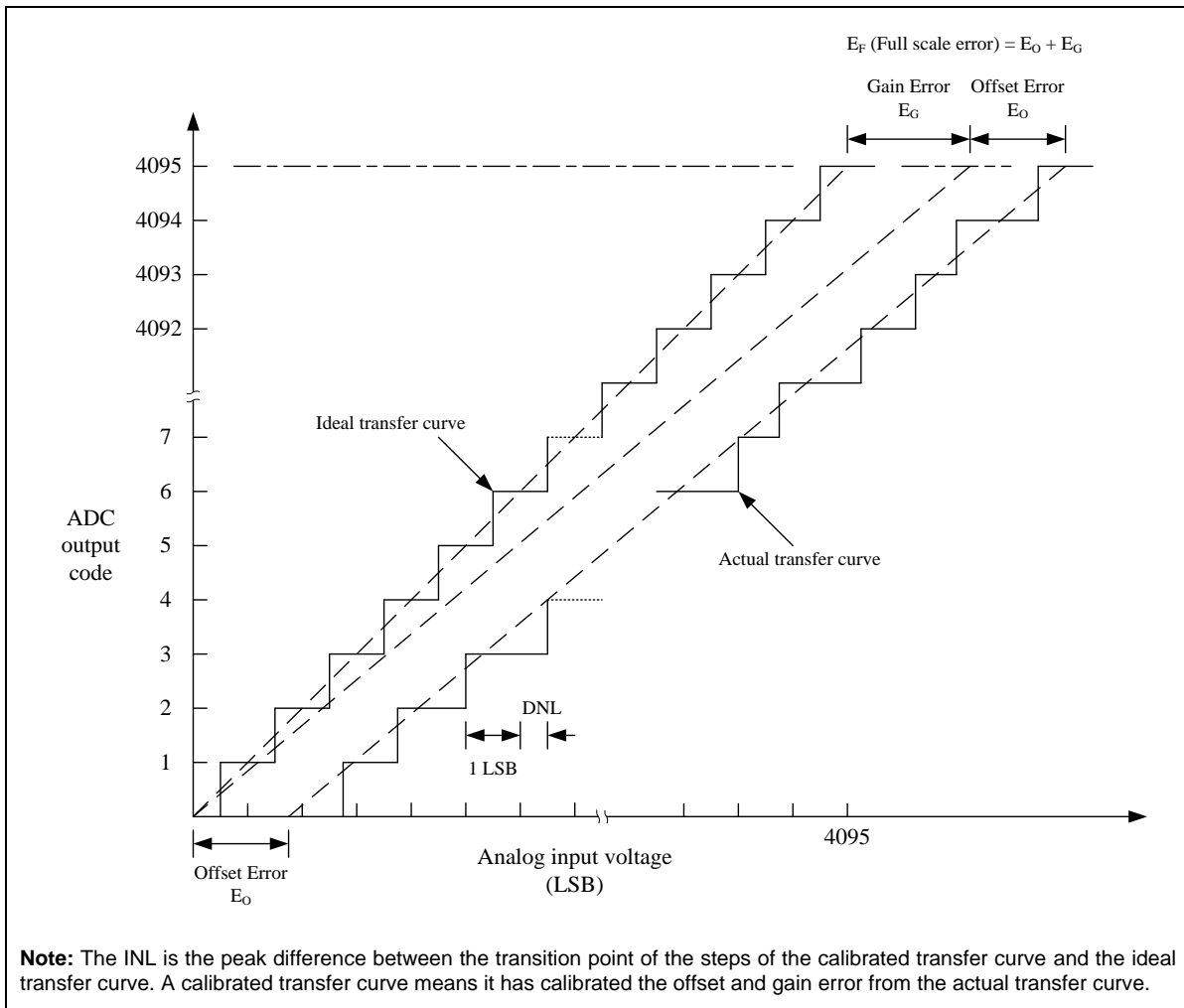
### 8.5.6 12-bit ADC

#### ***Fast Speed Channel***

| Sym.                | Parameter   | Specifications |      |                  |                    | Test Condition  |
|---------------------|---|----------------|------|------------------|--------------------|---|
|                     |   | Min.           | Typ. | Max.             | Unit               |   |
| AV <sub>DD</sub>    | Operating voltage   | 1.8            |      | 3.6              | V                  | AV <sub>DD</sub> = V <sub>DD</sub>  |
| V <sub>REF</sub>    | Reference voltage   | 1.6            |      | AV <sub>DD</sub> | V                  |   |
| T <sub>A</sub>      | Temperature   | -40            |      | 105              | °C                 |   |
| I <sub>ADC</sub>    | Operating current (AV <sub>DD</sub> current)<br>(Enable ADC and disable all other analog modules) | 478            |      | 523              | uA                 | AV <sub>DD</sub> = V <sub>DD</sub> = V <sub>REF</sub> = 3.3V<br>ADC Clock Rate = 70 MHz<br>High speed channel |
|                     | Resolution  |                |      | 12               | Bit                |   |
| V <sub>IN</sub>     | ADC channel input voltage   | 0              |      | V <sub>REF</sub> | V                  |   |
| F <sub>ADC</sub>    | ADC Clock frequency   | 0.14           |      | 70               | MHz                | High speed channel  |
| T <sub>SMP</sub>    | Sampling Time   |                | 2    |                  | 1/F <sub>ADC</sub> |   |
| T <sub>CONV</sub>   | Conversion time   |                | 14   |                  | 1/F <sub>ADC</sub> | T <sub>CONV</sub> = T <sub>SMP</sub> + 12   |
| F <sub>SPS</sub>    | Sampling Rate (F <sub>ADC</sub> /T <sub>CONV</sub> )  |                |      | 5                | MSPS               | High speed channel  |
| T <sub>PU</sub>     | Power-up time   | 20             |      |                  | μs                 |   |
| INL                 | Integral Non-Linearity Error  | -4.29          |      | -3.71            | LSB                | V <sub>REF</sub> = AV <sub>DD</sub>   |
| DNL                 | Differential Non-Linearity Error  | 3.25           |      | 3.28             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub>   |
| E <sub>G</sub>      | Gain error  | 2.25           |      | 2.31             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub>   |
| E <sub>OFFSET</sub> | Offset error  | 1.56           |      | 2.87             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub>   |
| E <sub>A</sub>      | Absolute Error  | 4.5            |      | 4.94             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub>   |
| C <sub>IN</sub>     | Internal Capacitance[*1]  |                | 5    |                  | pF                 |   |
| -                   | Monotonic   | Guaranteed     |      |                  | -                  |   |

**Low Speed Channel**

| Sym.                | Parameter   | Specifications |                  |                  |                    | Test Condition   |
|---------------------|---|----------------|------------------|------------------|--------------------|--|
|                     |   | Min.           | Typ.             | Max.             | Unit               |  |
| AV <sub>DD</sub>    | Operating voltage   | 1.8            |                  | 3.6              | V                  | AV <sub>DD</sub> = V <sub>DD</sub>   |
| V <sub>REF</sub>    | Reference voltage   |                | AV <sub>DD</sub> |                  | V                  |  |
| T <sub>A</sub>      | Temperature   | -40            |                  | 105              | °C                 |  |
| I <sub>ADC1</sub>   | Operating current (AV <sub>DD</sub> current)<br>(Enable ADC and disable all other analog modules) | 210            |                  | 231              | uA                 | AV <sub>DD</sub> = V <sub>DD</sub> = V <sub>REF</sub> = 3.3V<br>ADC Clock Rate = 28 MHz<br>low speed channel |
|                     |   | 131            |                  | 142              |                    | AV <sub>DD</sub> = V <sub>DD</sub> = V <sub>REF</sub> = 1.8V<br>ADC Clock Rate = 28 MHz<br>low speed channel |
| I <sub>ADC2</sub>   |   | 111            |                  | 123              | uA                 | AV <sub>DD</sub> = V <sub>DD</sub> = V <sub>REF</sub> = 3.3V<br>ADC Clock Rate = 14 MHz<br>low speed channel |
|                     |   | 70             |                  | 78               |                    | AV <sub>DD</sub> = V <sub>DD</sub> = V <sub>REF</sub> = 1.8V<br>ADC Clock Rate = 14 MHz<br>low speed channel |
|                     | Resolution  |                |                  | 12               | Bit                |  |
| V <sub>IN</sub>     | ADC channel input voltage   | 0              |                  | V <sub>REF</sub> | V                  |  |
| F <sub>ADC</sub>    | ADC Clock frequency   | 0.14           |                  | 70               | MHz                | Low speed channel  |
| T <sub>SMP</sub>    | Sampling Time   |                | 2                |                  | 1/F <sub>ADC</sub> |  |
| T <sub>CONV</sub>   | Conversion time   |                | 14               |                  | 1/F <sub>ADC</sub> | T <sub>CONV</sub> = T <sub>SMP</sub> + 12  |
| F <sub>SPS</sub>    | Sampling Rate (F <sub>ADC</sub> /T <sub>CONV</sub> )  |                |                  | 2                | MSPS               | Low speed channel<br><b>Note:</b> it needs more extend sampling time to slow down the sampling rate.         |
| T <sub>PU</sub>     | Power-up time   | 20             |                  |                  | μs                 |  |
| INL                 | Integral Non-Linearity Error  | -2.94          |                  | -1.32            | LSB                | V <sub>REF</sub> = AV <sub>DD</sub>  |
| DNL                 | Differential Non-Linearity Error  | 1.25           |                  | 2                | LSB                | V <sub>REF</sub> = AV <sub>DD</sub>  |
| E <sub>G</sub>      | Gain error  | 2.5            |                  | 3.12             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub>  |
| E <sub>OFFSET</sub> | Offset error  | 2.44           |                  | 3.69             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub>  |
| E <sub>A</sub>      | Absolute Error  | 4.69           |                  | 6.75             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub>  |
| C <sub>IN</sub>     | Internal Capacitance[*1]  |                | 5                |                  | pF                 |  |
| -                   | Monotonic   | Guaranteed     |                  |                  | -                  |  |



8.5.7 Temperature Sensor

| Symbol  | Parameter  | Min   | Typ   | Max   | Unit  |
|---|--|-------|-------|-------|-------|
| V <sub>DD</sub>   | Operating Voltage  | 1.8   |       | 3.6   | V     |
| T <sub>A</sub>  | Temperature Range  | -40   |       | 105   | °C    |
| I <sub>TEMP</sub>   | Current Consumption [*3]   |       | 16    |       | μA    |
| T <sub>c</sub>  | Temperature Coefficient [*3]                                       | -1.77 | -1.82 | -1.84 | mV/°C |
| V <sub>os</sub>   | Offset Voltage when T <sub>A</sub> = 0°C [*3]                      | 710.2 |       | 716.8 | mV    |
| t <sub>S</sub>  | Stable time[*2]  |       | 1     |       | μs    |
| T <sub>S_temp</sub>   | ADC sampling time when reading the temperature (5pF cap load) [*1] |       | 3     |       | μs    |
| <p><b>Note:</b></p> <ol style="list-style-type: none"> <li>1. <math>V_{TEMP} (mV) = T_c (mV/°C) \times \text{Temperature } (°C) + V_{os} (mV)</math></li> <li>2. Guaranteed by design, not tested in production</li> <li>3. Guaranteed by characteristic, not tested in production</li> </ol> |  |       |       |       |       |

8.5.8 Digital to Analog Converter (DAC)

| Symbol     | Parameter                                  | Min               | Typ | Max            | Unit       | Test Condition                                 |
|------------|--|-------------------|-----|----------------|------------|--|
| $V_{DD}$   | Analog supply voltage                      | 1.8               | -   | 3.6            | V          | -  |
| $N_R$      | Resolution                                 | 12                |     |                | bit        | -  |
| $V_{REF}$  | Reference supply voltage                   | 1.5               | -   | $V_{DD}$       | V          | $V_{REF} \leq V_{DD}$                          |
| DNL        | Differential non-linearity error[*4]       | -                 | -   | $\pm 2$        | LSB        | 12-bit mode                                    |
|            |  | -                 | -   | $\pm 0.5$      | LSB        | 8-bit mode                                     |
| INL        | Integral non-linearity error[*4]           | -                 | -   | $\pm 4$        | LSB        | 12-bit mode                                    |
|            |  | -                 | -   | $\pm 1$        | LSB        | 8-bit mode                                     |
| OE         | Offset Error[*4]                           | -                 | -   | $\pm 30$       | LSB        | 12-bit mode<br>DACOUT buffer ON                |
|            |  | -                 | -   | $\pm 4$        | LSB        | 12-bit mode<br>DACOUT buffer OFF               |
|            |  | -                 | -   | $\pm 2$        | LSB        | 8-bit mode                                     |
| GE         | Gain Error[*4]                             | -                 | -   | $\pm 5$        | LSB        | 12-bit mode<br>DACOUT buffer ON                |
|            |  | -                 | -   | $\pm 4$        | LSB        | 12-bit mode<br>DACOUT buffer OFF               |
|            |  | -                 | -   | $\pm 2$        | LSB        | 8-bit mode                                     |
| AE         | Absolute Error[*4]                         | -                 | -   | $\pm 8$        | LSB        | 12-bit mode<br>DACOUT buffer ON                |
|            |  | -                 | -   | $\pm 4$        | LSB        | 12-bit mode<br>DACOUT buffer OFF               |
|            |  | -                 | -   | $\pm 2$        | LSB        | 8-bit mode                                     |
| -          | Monotonic                                  | 10-bit guaranteed |     |                | -          | -  |
| $V_O$      | Output Voltage                             | 0.2               |     | $V_{DD} - 0.2$ | V          | DACOUT buffer ON                               |
| $R_{LOAD}$ | Resistive load[*2]                         | 7.5               | -   | -              | k $\Omega$ | DACOUT buffer ON                               |
| $R_o$      | Output impedance[*4]                       |                   | 10  | 12             | k $\Omega$ | DACOUT buffer OFF                              |
| $C_{LOAD}$ | Capacitive load[*3]                        | -                 | -   | 50             | pF         | -  |
| $I_{AVDD}$ | Current consumption on $V_{DD}$ supply[*4] | -                 | -   | 180            | $\mu A$    | $V_{DD} = 3.6V$ , no load, lowest code (0x000) |
|            |  | -                 | -   | 420            |            | $V_{DD} = 3.6V$ , no load, middle code (0x800) |

| Symbol   | Parameter                                   | Min | Typ | Max | Unit      | Test Condition   |
|--|---|-----|-----|-----|-----------|--|
| $I_{REF}$  | Current consumption on $V_{REF}$ supply[*4] | -   | 150 | 240 | $\mu A$   | $V_{REF} = 3.6V$ , no load, middle code (0x800)  |
| $T_S$  | Settling Time                               | -   | 5   | 6   | $\mu s$   | Full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value $\pm 1$ LSB,<br>$C_{LOAD} \leq 50pF$ , $R_{LOAD} \geq 7.5k\Omega$ |
| $F_s$  | Update Rate                                 | -   | -   | 1   | $M_{SPS}$ | Max. frequency for a correct DAC_OUT change from core $i$ to $i+1$ LSB, $C_{LOAD} \leq 50pF$ , $R_{LOAD} \geq 7.5k\Omega$  |
| $T_{WAKEUP}$   | Wake-up Time                                | -   | 9   | 15  | $\mu s$   | Wakeup time from OFF state. Input code between lowest and highest possible codes.<br>DAC clock source = 1 MHz  |
| PSRR   | Power Supply Rejection Ratio[*1]            | -   | -60 | -40 | dB        | No $R_{LOAD}$ , $C_{LOAD} = 50pF$  |
| <b>Note:</b> <ol style="list-style-type: none"> <li>Guaranteed by design, not tested in production.</li> <li>Resistive load between DACOUT and AVSS.</li> <li>Capacitive load at DACOUT pin.</li> <li>Guaranteed based on test during characterization.</li> </ol> |   |     |     |     |           |  |

8.5.9 Analog Comparator Controller (ACMP)

- The maximum values are obtained for  $V_{DD} = 3.6\text{ V}$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25\text{ }^\circ\text{C}$  and  $V_{DD} = 3.3\text{ V}$  unless otherwise specified.

| Symbol  | Parameter                                   | Min | Typ           | Max             | Unit             | Comments                             |
|---|---|-----|---------------|-----------------|------------------|--------------------------------------|
| $AV_{DD}$   | Analog supply voltage                       | 1.8 |               | 3.6             | V                |                                      |
| $T_A$   | Temperature                                 | -40 |               | 105             | $^\circ\text{C}$ |                                      |
| $I_{DD}$  | Operating current                           |     | 1.2           |                 | $\mu\text{A}$    | MODESEL[1:0] = 00                    |
|   |   |     | 3             |                 |                  | MODESEL[1:0] = 01                    |
|   |   |     | 10            |                 |                  | MODESEL[1:0] = 10                    |
|   |   |     | 75            |                 |                  | MODESEL[1:0] = 11                    |
| $V_{CM}$  | Input common mode voltage range [*2]        | 0.1 | 1/2 $AV_{DD}$ | $AV_{DD} - 0.1$ |                  |                                      |
| $V_{DI}$  | Differential input voltage sensitivity [*2] | 10  | 20            |                 | mV               | Hysteresis disable                   |
| $V_{offset}$                                      | Input offset voltage                        |     | 5             | 10              | mV               | Hysteresis disable,                  |
| $V_{hys}$   | Hysteresis window                           |     | 0             |                 | mV               | HYSSEL[1:0] = 00                     |
|   |   |     | 10            |                 |                  | HYSSEL[1:0] = 01                     |
|   |   |     | 20            |                 |                  | HYSSEL[1:0] = 10                     |
|   |   |     | 30            |                 |                  | HYSSEL[1:0] = 11                     |
| $A_v$   | DC voltage Gain[*1]                         |     | 70            |                 | dB               |                                      |
| $T_d$   | Propagation delay[*2]                       |     |               | 4.5             | $\mu\text{S}$    | Hysteresis disable MODESEL[1:0] = 00 |
|   |   |     |               | 2               |                  | Hysteresis disable MODESEL[1:0] = 01 |
|   |   |     |               | 0.6             |                  | Hysteresis disable MODESEL[1:0] = 10 |
|   |   |     |               | 0.2             |                  | Hysteresis disable MODESEL[1:0] = 11 |
| $T_{Setup}$                                       | Setup time[*2]                              |     |               | 4.75            | $\mu\text{S}$    | Hysteresis disable MODESEL[1:0] = 00 |
|   |   |     |               | 2.25            |                  | Hysteresis disable MODESEL[1:0] = 01 |
|   |   |     |               | 0.85            |                  | Hysteresis disable MODESEL[1:0] = 10 |
|   |   |     |               | 0.45            |                  | Hysteresis disable MODESEL[1:0] = 11 |
| <b>Note:</b>                                      |   |     |               |                 |                  |                                      |
| 1. Guaranteed by design, not tested in production |   |     |               |                 |                  |                                      |

8.5.10 OP Amplifier (OPA)

- The maximum values are obtained for  $V_{DD} = 3.6\text{ V}$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25\text{ °C}$  and  $V_{DD} = 3.3\text{ V}$  unless otherwise specified.

| Symbol  | Parameter  | Min               | Typ | Max          | Unit   | Comments  |
|---|--|-------------------|-----|--------------|--------|---|
| $A_{V_{DD}}$  | Analog supply voltage                                | 2.4               |     | 3.6          | V      |   |
| $T_A$   | Temperature  | -40               |     | 105          | °C     |   |
| $I_{DD}$  | Consumption current                                  |                   | 690 |              | μA     | $A_{V_{DD}}=3.3\text{V}$ , Temperature= $25\text{ °C}$                    |
| CMIR  | Common mode input range                              | 0                 |     | $A_{V_{DD}}$ | V      |   |
| $V_{OFFSET0}$   | Input offset voltage(maximum calibration range) [*2] |                   |     | 4            | mV     | $T_j = 25\text{°C}$ , No Load   |
|   |  |                   |     | 6            |        | $V_{CM} = A_{V_{DD}}-10\text{mV} \sim A_{V_{DD}}-0.8\text{V}$ , All Temp. |
| $V_{OFFSET1}$   | Input offset voltage(After offset calibration) [*2]  |                   |     | 3.2          |        | CALRVS =0: Other $V_{CM}$   |
|   |  |                   |     | 6.5          |        | CALRVS=0: $V_{CM} = A_{V_{DD}}-10\text{mV} \sim A_{V_{DD}}-0.8\text{V}$   |
| $V_{OFFSET2}$   | Input offset voltage(After offset calibration) [*2]  |                   |     | 3            |        | CALRVS =1: Other $V_{CM}$   |
|   |  |                   |     | 5.2          |        | CALRVS =1: $V_{CM} = A_{V_{DD}}-10\text{mV} \sim A_{V_{DD}}-0.8\text{V}$  |
| CMRR  | Common Mode Rejection Ratio [*1]                     |                   | 90  |              | dB     |   |
| PSRR  | Power Supply Rejection Ratio [*1]                    | 73                | 117 |              | dB     |   |
| GBW   | Bandwidth [*2]                                       |                   | 8.2 |              | MHz    |   |
| SR  | Slew rate [*2]                                       |                   | 4.7 |              | V/μs   |   |
| $V_{OHSAT}$   | High saturation voltage [*2]                         | $A_{V_{DD}}-0.1$  |     |              | V      | Rload=min. INPUT at $A_{V_{DD}}$  |
|   |  | $A_{V_{DD}}-0.02$ |     |              |        | Rload=20K, INPUT at $A_{V_{DD}}$  |
| $V_{OLSAT}$   | Low saturation voltage [*2]                          |                   |     | 100          | mV     | Rload=min. INPUT at 0   |
|   |  |                   |     | 20           |        | Rload=20K, INPUT at 0   |
| PM  | Phase Margin [*1]                                    |                   | 62  |              | degree |   |
| $T_{WAKEUP}$  | Wake up time from OFF state [*2]                     |                   | 2.8 | 5            | μs     |   |
| $R_{LOAD}$  | Resistive load                                       | 4                 |     |              | kΩ     |   |
| $C_{LOAD}$  | Capacitive load                                      |                   |     | 50           | pF     |   |
| <b>Note:</b>  |  |                   |     |              |        |   |
| 1. Guaranteed by characteristic, not tested in production |  |                   |     |              |        |   |



8.6 Flash DC Electrical Characteristic

| Symbol  | Parameter       | Min   | Typ | Max  | Unit                  | Test Condition     |
|---|-----------------|-------|-----|------|-----------------------|--------------------|
| $V_{FLA}^{[1]}$   | Supply Voltage  | 1.08  |     | 1.32 | V                     | $T_A = 25^\circ C$ |
| $N_{ENDUR}$   | Endurance       | 10000 | -   | -    | cycles <sup>[2]</sup> |                    |
| $T_{RET}$   | Data Retention  | 10    | -   | -    | year                  |                    |
| $T_{ERASE}$   | Page Erase Time | 92    | -   | 160  | mS                    |                    |
| $T_{MER}$   | Mass Erase Time | 201   | -   | 320  | mS                    |                    |
| $T_{PROG}$  | Program Time    |       | -   | 50   | uS                    |                    |
| $I_{DD1}$   | Read Current    | -     | -   | 4.12 | mA                    |                    |
| $I_{DD2}$   | Program Current | -     | -   | 5    | mA                    |                    |
| $I_{DD3}$   | Erase Current   | -     | -   | 5    | uA                    |                    |
| <b>Note:</b>  |                 |       |     |      |                       |                    |
| <ol style="list-style-type: none"> <li>1. <math>V_{FLA}</math> is source from chip LDO output voltage.</li> <li>2. Number of program/erase cycles.</li> <li>3. This table is guaranteed by design, not test in production.</li> </ol> |                 |       |     |      |                       |                    |

### 8.7 I<sup>2</sup>C Dynamic Characteristics

| Symbol               | Parameter                           | Standard Mode <sup>[1][2]</sup> |                     | Fast Mode <sup>[1][2]</sup> |                    | Unit |
|----------------------|-------------------------------------|---------------------------------|---------------------|-----------------------------|--------------------|------|
|                      |                                     | Min.                            | Max.                | Min.                        | Max.               |      |
| t <sub>LOW</sub>     | SCL low period                      | 4.7                             | -                   | 1.2                         | -                  | uS   |
| t <sub>HIGH</sub>    | SCL high period                     | 4                               | -                   | 0.6                         | -                  | uS   |
| t <sub>SU; STA</sub> | Repeated START condition setup time | 4.7                             | -                   | 1.2                         | -                  | uS   |
| t <sub>HD; STA</sub> | START condition hold time           | 4                               | -                   | 0.6                         | -                  | uS   |
| t <sub>SU; STO</sub> | STOP condition setup time           | 4                               | -                   | 0.6                         | -                  | uS   |
| t <sub>BUF</sub>     | Bus free time                       | 4.7 <sup>[3]</sup>              | -                   | 1.2 <sup>[3]</sup>          | -                  | uS   |
| t <sub>SU; DAT</sub> | Data setup time                     | 250                             | -                   | 100                         | -                  | nS   |
| t <sub>HD; DAT</sub> | Data hold time                      | 0 <sup>[4]</sup>                | 3.45 <sup>[5]</sup> | 0 <sup>[4]</sup>            | 0.8 <sup>[5]</sup> | uS   |
| t <sub>r</sub>       | SCL/SDA rise time                   | -                               | 1000                | 20+0.1C <sub>b</sub>        | 300                | nS   |
| t <sub>f</sub>       | SCL/SDA fall time                   | -                               | 300                 | -                           | 300                | nS   |
| C <sub>b</sub>       | Capacitive load for each bus line   | -                               | 400                 | -                           | 400                | pF   |

**Note:**

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I<sup>2</sup>C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I<sup>2</sup>C frequency.
3. I<sup>2</sup>C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

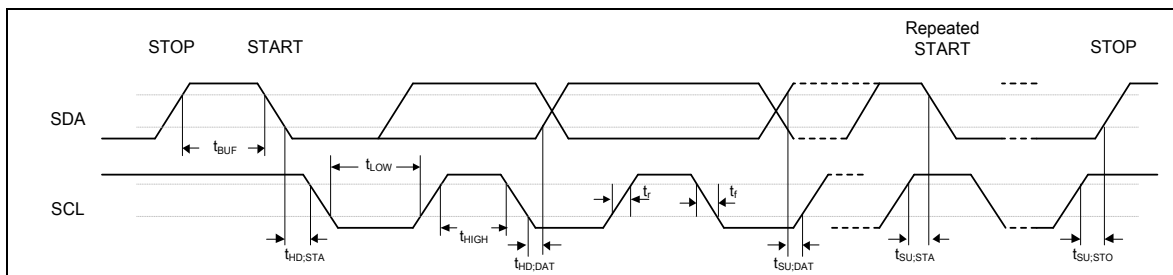


Figure 8-13 I<sup>2</sup>C Timing Diagram

### 8.8 SPI Dynamic Characteristics

| Symbol   | Parameter                   | Min. | Typ. | Max.             | Unit |
|--|-----------------------------|------|------|------------------|------|
| SPI MASTER MODE ( $V_{DD} = 3.0\sim 3.6\text{ V}$ , 30 PF LOADING CAPACITOR) |                             |      |      |                  |      |
| $t_{CLKH}$   | Clock output High time [*1] |      |      | $T_{SPICLK} / 2$ | ns   |
| $t_{CLKL}$   | Clock output Low time [*1]  |      |      | $T_{SPICLK} / 2$ | ns   |
| $t_{DS}$   | Data setup time             | 0    | -    | -                | ns   |
| $t_{DH}$   | Data hold time              | 2    | -    | -                | ns   |
| $t_V$  | Data output valid time      | -    | 0    | 1                | ns   |
| SPI MASTER MODE ( $V_{DD} = 1.8\sim 2.0\text{ V}$ , 30 PF LOADING CAPACITOR) |                             |      |      |                  |      |
| $t_{CLKH}$   | Clock output High time [*1] |      |      | $T_{SPICLK} / 2$ | ns   |
| $t_{CLKL}$   | Clock output Low time [*1]  |      |      | $T_{SPICLK} / 2$ | ns   |
| $t_{DS}$   | Data setup time             | 0    | -    | -                | ns   |
| $t_{DH}$   | Data hold time              | 2    | -    | -                | ns   |
| $t_V$  | Data output valid time      | -    | -    | 1                | ns   |
| <b>Note:</b>   |                             |      |      |                  |      |
| 1. The minimum clock period for SPICLK is 10.4 ns (96 MHz).                  |                             |      |      |                  |      |

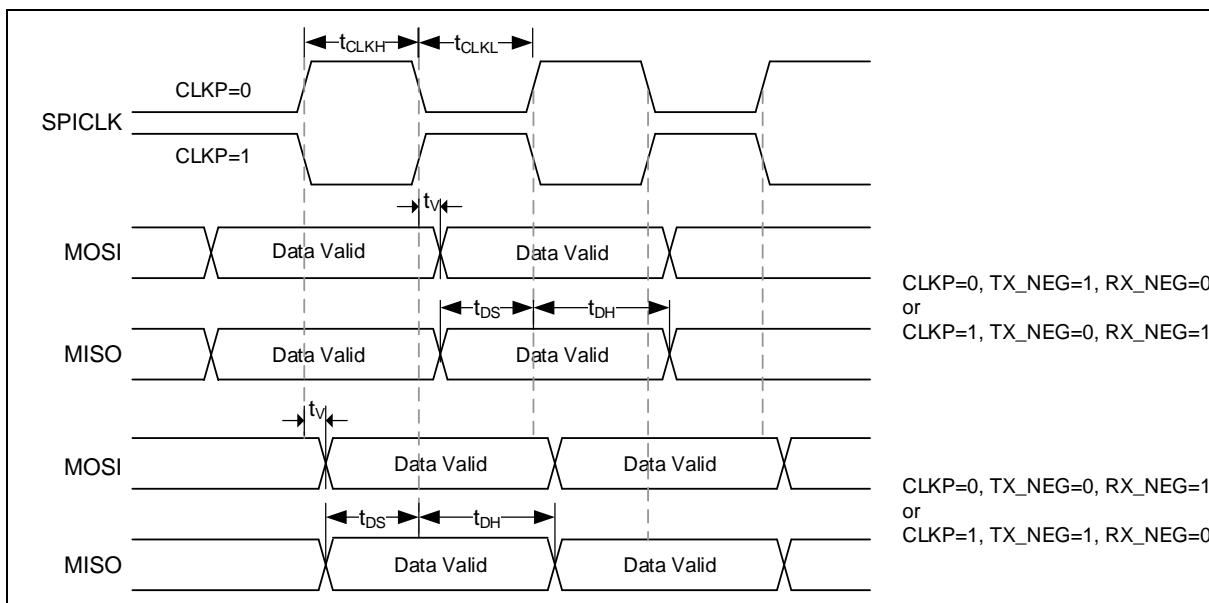


Figure 8-14 SPI Master Mode Timing Diagram

| Symbol  | Parameter                   | Min.                 | Typ. | Max.             | Unit |
|---|-----------------------------|----------------------|------|------------------|------|
| SPI SLAVE MODE ( $V_{DD} = 3.0\sim 3.6V$ , 30 PF LOADING CAPACITOR)     |                             |                      |      |                  |      |
| $t_{CLKH}$  | Clock output High time [*1] | -                    | -    | $T_{SPICLK} / 2$ | ns   |
| $t_{CLKL}$  | Clock output Low time [*1]  | -                    | -    | $T_{SPICLK} / 2$ | ns   |
| $t_{SS}$  | Slave select setup time     | $1 T_{SPICLK} + 2ns$ | -    | -                | ns   |
| $t_{SH}$  | Slave select hold time      | $1 T_{SPICLK}$       | -    | -                | ns   |
| $t_{DS}$  | Data input setup time       | 0                    | -    | -                | ns   |
| $t_{DH}$  | Data input hold time        | 2                    | -    | -                | ns   |
| $t_V$   | Data output valid time      | -                    | -    | 8                | ns   |
| $t_{CLKH}$  | Clock output High time [*1] | -                    | -    | $T_{SPICLK} / 2$ | ns   |
| SPI SLAVE MODE ( $V_{DD} = 1.8 V \sim 2.0 V$ , 30 PF LOADING CAPACITOR) |                             |                      |      |                  |      |
| $t_{CLKH}$  | Clock output High time [*1] | -                    | -    | $T_{SPICLK} / 2$ | ns   |
| $t_{CLKL}$  | Clock output Low time [*1]  | -                    | -    | $T_{SPICLK} / 2$ | ns   |
| $t_{SS}$  | Slave select setup time     | $1 T_{SPICLK} + 3ns$ | -    | -                | ns   |
| $t_{SH}$  | Slave select hold time      | $1 T_{SPICLK}$       | -    | -                | ns   |
| $t_{DS}$  | Data input setup time       | 0                    | -    | -                | ns   |
| $t_{DH}$  | Data input hold time        | 2                    | -    | -                | ns   |
| $t_V$   | Data output valid time      | -                    | -    | 10               | ns   |
| <b>Note:</b>  |                             |                      |      |                  |      |
| 1. The minimum clock period for SPICLK is 10.4 ns (96 MHz).             |                             |                      |      |                  |      |

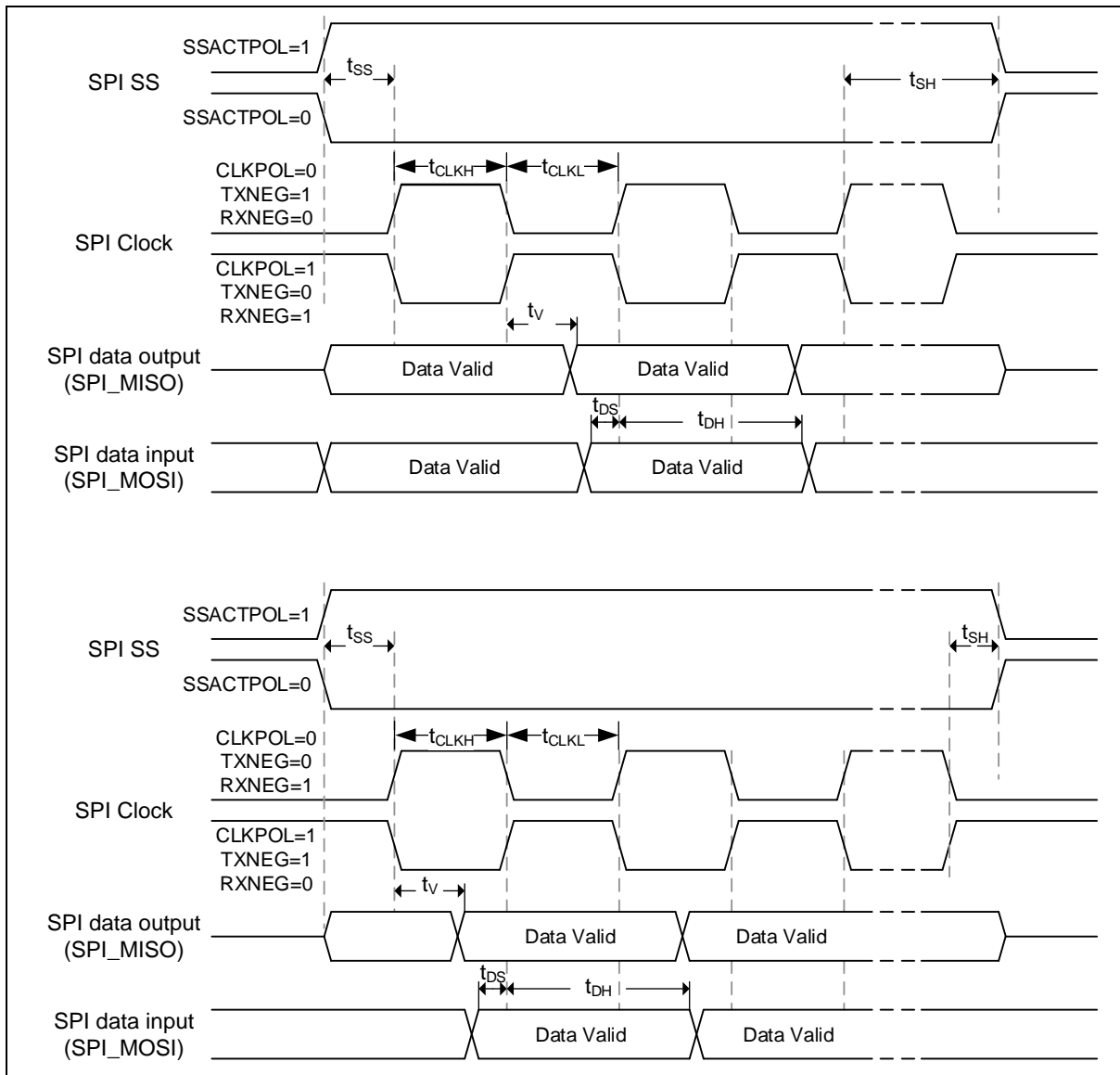


Figure 8-15 SPI Slave Mode Timing Diagram

8.9 I<sup>2</sup>S Dynamic Characteristics

| Symbol           | Parameter                                     | Min | Max | Unit | Test Conditions   |
|------------------|---|-----|-----|------|---|
| $t_{w(CKH)}$     | I <sup>2</sup> S clock high time              | 40  | -   | ns   | Master $f_{PCLK} = \text{MHz}$ , data: 24 bits, audio frequency = 256 kHz |
| $t_{w(CKL)}$     | I <sup>2</sup> S clock low time               | 40  | -   |      |   |
| $t_{v(WS)}$      | WS valid time                                 | 4   | 16  |      |   |
| $t_{h(WS)}$      | WS hold time                                  | 1   | -   |      |   |
| $t_{su(WS)}$     | WS setup time                                 | 24  | -   |      |   |
| $t_{h(WS)}$      | WS hold time                                  | 0   | -   |      |   |
| $DuCy_{(SCK)}$   | I <sup>2</sup> S slave input clock duty cycle | 30  | 70  | %    | Slave mode  |
| $t_{su(SD\_MR)}$ | Data input setup time                         | 10  | -   | ns   | Master receiver   |
| $t_{su(SD\_SR)}$ |   | 7   | -   |      | Slave receiver  |
| $t_{h(SD\_MR)}$  | Data input hold time                          | 7   | -   |      | Master receiver   |
| $t_{h(SD\_SR)}$  |   | 4   | -   |      | Slave receiver  |
| $t_{v(SD\_ST)}$  | Data output valid time                        | -   | 10  |      | Slave transmitter (after enable edge)                                     |
| $t_{h(SD\_ST)}$  | Data output hold time                         | 4   | -   |      | Slave transmitter (after enable edge)                                     |
| $t_{v(SD\_MT)}$  | Data output valid time                        | -   | 4   |      | Master transmitter (after enable edge)                                    |
| $t_{h(SD\_MT)}$  | Data output hold time                         | 0   | -   |      | Master transmitter (after enable edge)                                    |

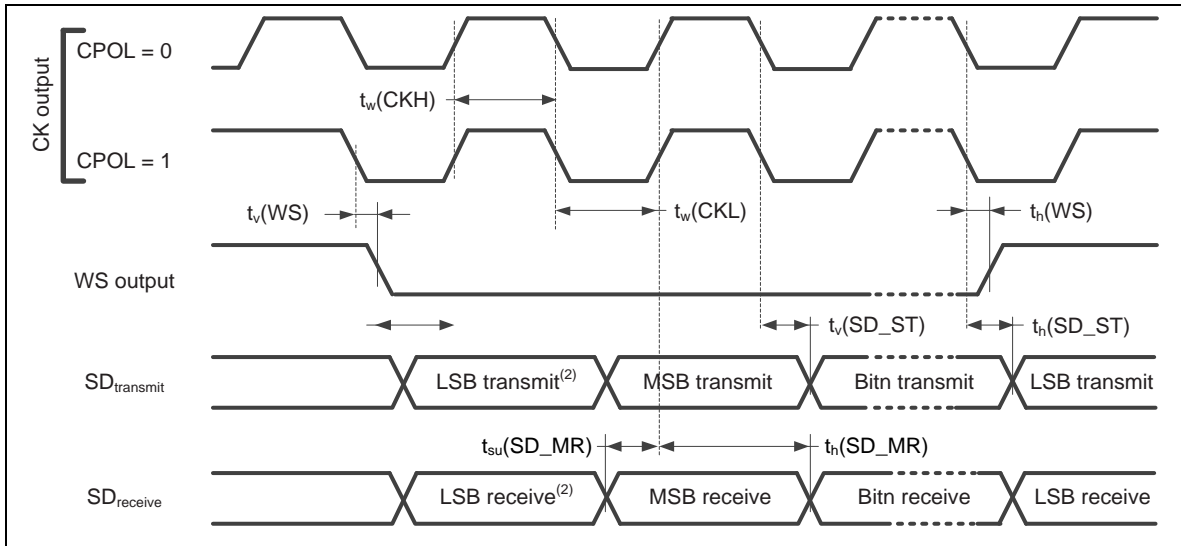


Figure 8-16 I<sup>2</sup>S Master Mode Timing Diagram

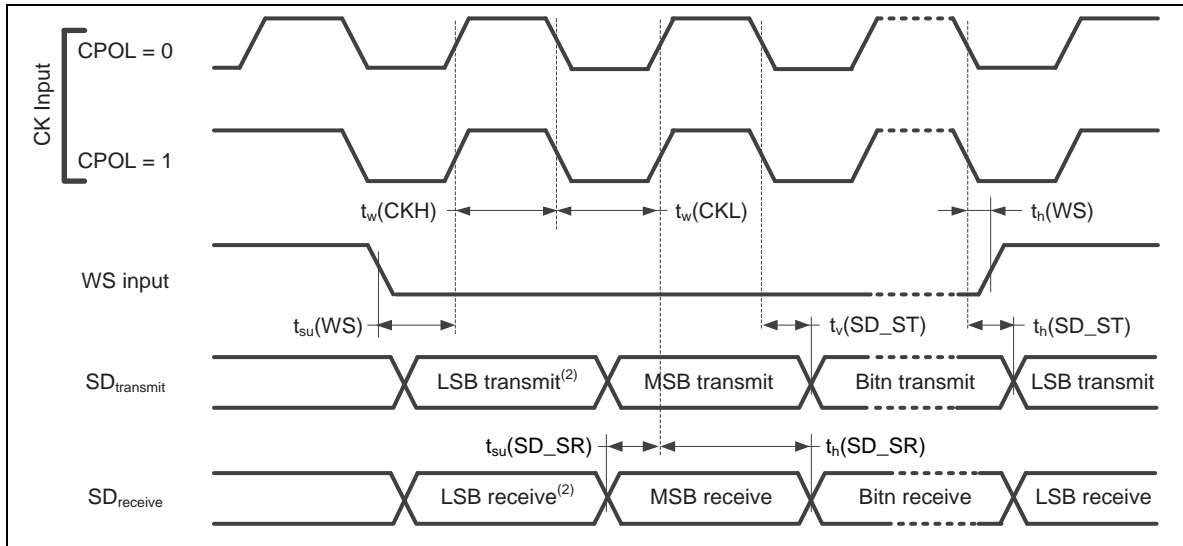


Figure 8-17 I<sup>2</sup>S Slave Mode Timing Diagram

8.10 USCI - I<sup>2</sup>C Dynamic Characteristics

| Symbol               | Parameter                           | Standard Mode <sup>[1][2]</sup> |                     | Fast Mode <sup>[1][2]</sup> |                    | Unit |
|----------------------|-------------------------------------|---------------------------------|---------------------|-----------------------------|--------------------|------|
|                      |                                     | Min.                            | Max.                | Min.                        | Max.               |      |
| t <sub>LOW</sub>     | SCL low period                      | 4.7                             | -                   | 1.2                         | -                  | uS   |
| t <sub>HIGH</sub>    | SCL high period                     | 4                               | -                   | 0.6                         | -                  | uS   |
| t <sub>SU; STA</sub> | Repeated START condition setup time | 4.7                             | -                   | 1.2                         | -                  | uS   |
| t <sub>HD; STA</sub> | START condition hold time           | 4                               | -                   | 0.6                         | -                  | uS   |
| t <sub>SU; STO</sub> | STOP condition setup time           | 4                               | -                   | 0.6                         | -                  | uS   |
| t <sub>BUF</sub>     | Bus free time                       | 4.7 <sup>[3]</sup>              | -                   | 1.2 <sup>[3]</sup>          | -                  | uS   |
| t <sub>SU; DAT</sub> | Data setup time                     | 250                             | -                   | 100                         | -                  | nS   |
| t <sub>HD; DAT</sub> | Data hold time                      | 0 <sup>[4]</sup>                | 3.45 <sup>[5]</sup> | 0 <sup>[4]</sup>            | 0.8 <sup>[5]</sup> | uS   |
| t <sub>r</sub>       | SCL/SDA rise time                   | -                               | 1000                | 20+0.1C <sub>b</sub>        | 300                | nS   |
| t <sub>f</sub>       | SCL/SDA fall time                   | -                               | 300                 | -                           | 300                | nS   |
| C <sub>b</sub>       | Capacitive load for each bus line   | -                               | 400                 | -                           | 400                | pF   |

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I<sup>2</sup>C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I<sup>2</sup>C frequency.
3. I<sup>2</sup>C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

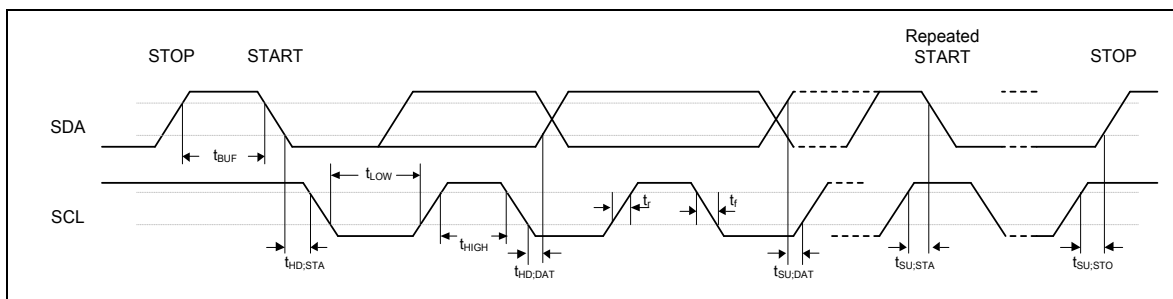


Figure 8-18 I<sup>2</sup>C Timing Diagram



8.11 USCI - SPI Dynamic Characteristics

| Symbol   | Parameter                   | Min. | Typ. | Max.             | Unit |
|--|-----------------------------|------|------|------------------|------|
| SPI MASTER MODE ( $V_{DD} = 3.0\sim 3.6\text{ V}$ , 30 PF LOADING CAPACITOR) |                             |      |      |                  |      |
| $t_{CLKH}$   | Clock output High time [*1] |      |      | $T_{SPICLK} / 2$ | ns   |
| $t_{CLKL}$   | Clock output Low time [*1]  |      |      | $T_{SPICLK} / 2$ | ns   |
| $t_{DS}$   | Data setup time             | 0    | -    | -                | ns   |
| $t_{DH}$   | Data hold time              | 2    | -    | -                | ns   |
| $t_V$  | Data output valid time      | -    | 0    | 1                | ns   |
| SPI MASTER MODE ( $V_{DD} = 1.8\sim 2.0\text{ V}$ , 30 PF LOADING CAPACITOR) |                             |      |      |                  |      |
| $t_{CLKH}$   | Clock output High time [*1] |      |      | $T_{SPICLK} / 2$ | ns   |
| $t_{CLKL}$   | Clock output Low time [*1]  |      |      | $T_{SPICLK} / 2$ | ns   |
| $t_{DS}$   | Data setup time             | 0    | -    | -                | ns   |
| $t_{DH}$   | Data hold time              | 2    | -    | -                | ns   |
| $t_V$  | Data output valid time      | -    | -    | 1                | ns   |
| <b>Note:</b>   |                             |      |      |                  |      |
| 1. The minimum clock period for SPICLK is 10.4 ns (96 MHz).                  |                             |      |      |                  |      |

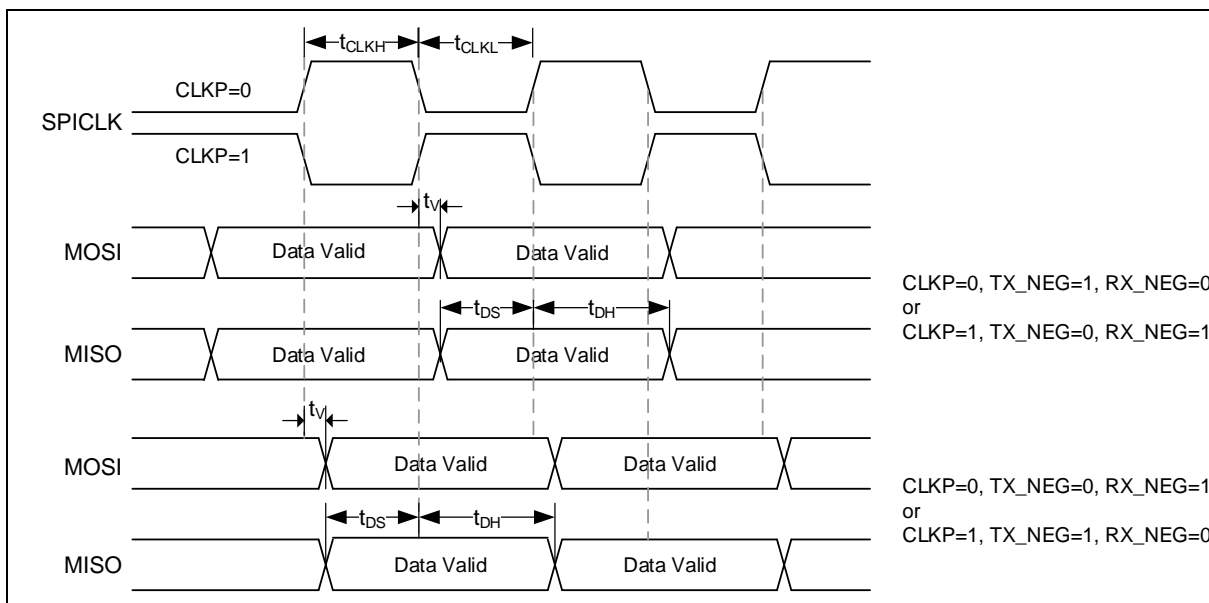


Figure 8-19 SPI Master Mode Timing Diagram

| Symbol  | Parameter                   | Min.                 | Typ. | Max.             | Unit |
|---|-----------------------------|----------------------|------|------------------|------|
| SPI SLAVE MODE ( $V_{DD} = 3.0\sim 3.6V$ , 30 PF LOADING CAPACITOR)     |                             |                      |      |                  |      |
| $t_{CLKH}$  | Clock output High time [*1] | -                    | -    | $T_{SPICLK} / 2$ | ns   |
| $t_{CLKL}$  | Clock output Low time [*1]  | -                    | -    | $T_{SPICLK} / 2$ | ns   |
| $t_{SS}$  | Slave select setup time     | $1 T_{SPICLK} + 2ns$ | -    | -                | ns   |
| $t_{SH}$  | Slave select hold time      | $1 T_{SPICLK}$       | -    | -                | ns   |
| $t_{DS}$  | Data input setup time       | 0                    | -    | -                | ns   |
| $t_{DH}$  | Data input hold time        | 2                    | -    | -                | ns   |
| $t_V$   | Data output valid time      | -                    | -    | 8                | ns   |
| $t_{CLKH}$  | Clock output High time [*1] | -                    | -    | $T_{SPICLK} / 2$ | ns   |
| SPI SLAVE MODE ( $V_{DD} = 1.8 V \sim 2.0 V$ , 30 PF LOADING CAPACITOR) |                             |                      |      |                  |      |
| $t_{CLKH}$  | Clock output High time [*1] | -                    | -    | $T_{SPICLK} / 2$ | ns   |
| $t_{CLKL}$  | Clock output Low time [*1]  | -                    | -    | $T_{SPICLK} / 2$ | ns   |
| $t_{SS}$  | Slave select setup time     | $1 T_{SPICLK} + 3ns$ | -    | -                | ns   |
| $t_{SH}$  | Slave select hold time      | $1 T_{SPICLK}$       | -    | -                | ns   |
| $t_{DS}$  | Data input setup time       | 0                    | -    | -                | ns   |
| $t_{DH}$  | Data input hold time        | 2                    | -    | -                | ns   |
| $t_V$   | Data output valid time      | -                    | -    | 10               | ns   |
| <b>Note:</b>  |                             |                      |      |                  |      |
| 1. The minimum clock period for SPICLK is 10.4 ns (96 MHz).             |                             |                      |      |                  |      |

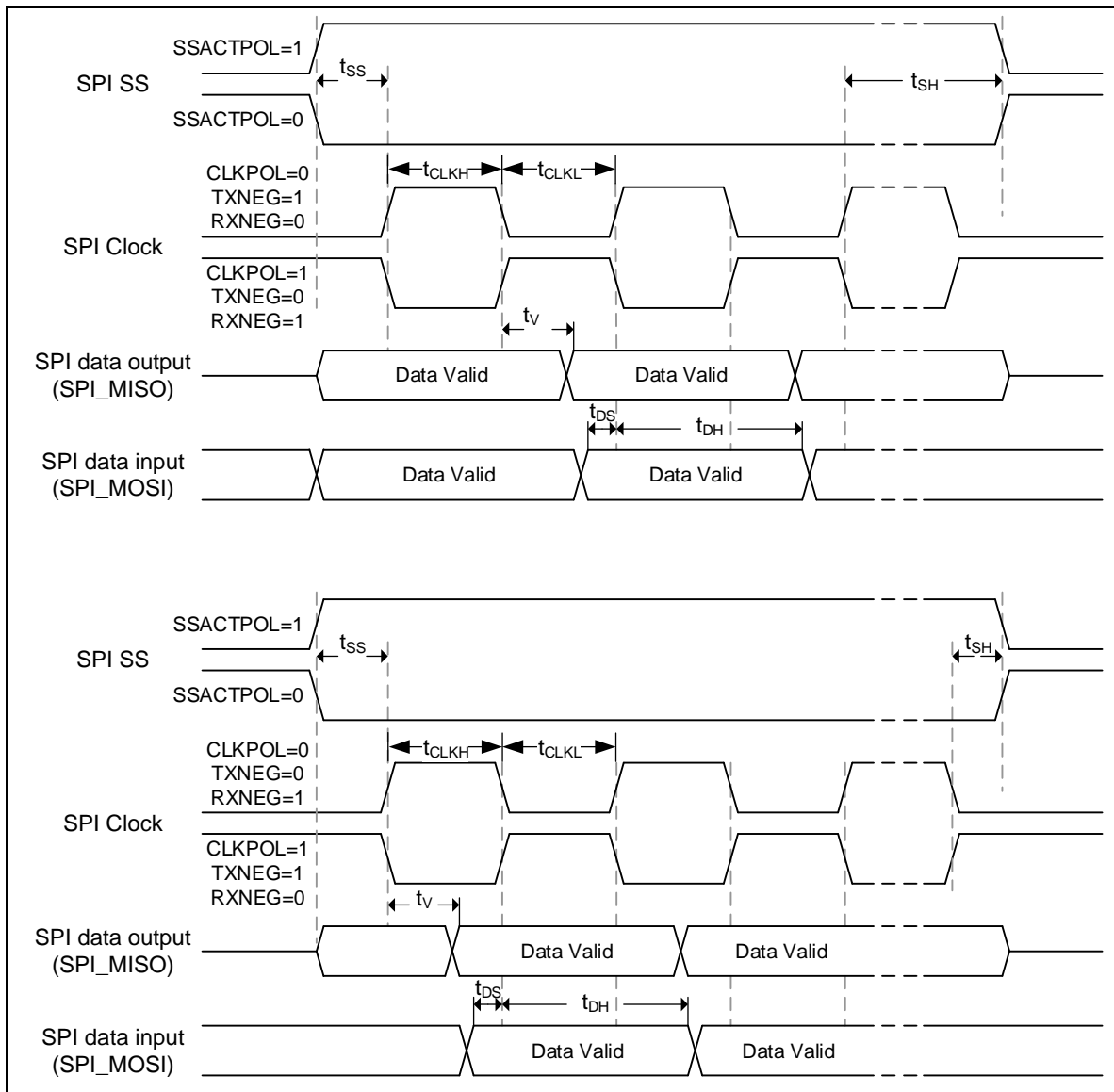


Figure 8-20 SPI Slave Mode Timing Diagram

## 8.12 USB Characteristics

### 8.12.1 USB Full-Speed

| Symbol           | Parameter   | Min.  | Typ. | Max.  | Unit | Test Conditions                |
|------------------|---|-------|------|-------|------|--------------------------------|
| V <sub>DD</sub>  | Operation Voltage                                   | 3.0   |      | 3.6   | V    |                                |
| V <sub>IH</sub>  | Input High (driven)                                 | 2.0   | -    | -     | V    | -                              |
| V <sub>IL</sub>  | Input Low   | -     | -    | 0.8   | V    | -                              |
| V <sub>DI</sub>  | Differential Input Sensitivity                      | 0.2   | -    | -     | V    | PADP-PADM                      |
| V <sub>CM</sub>  | Differential Common-mode Range                      | 0.8   | -    | 2.5   | V    | Includes V <sub>DI</sub> range |
| V <sub>SE</sub>  | Single-ended Receiver Threshold                     | 0.8   | -    | 2.0   | V    | -                              |
|                  | Receiver Hysteresis                                 | -     | 200  | -     | mV   | -                              |
| V <sub>OL</sub>  | Output Low (driven)                                 | 0     | -    | 0.3   | V    | -                              |
| V <sub>OH</sub>  | Output High (driven)                                | 2.8   | -    | 3.6   | V    | -                              |
| V <sub>CRS</sub> | Output Signal Cross Voltage                         | 1.3   | -    | 2.0   | V    | -                              |
| R <sub>PU</sub>  | Pull-up Resistor                                    | 1.425 | -    | 1.575 | kΩ   | -                              |
| R <sub>PD</sub>  | Pull-down Resistor                                  | 14.25 | -    | 15.75 | kΩ   |                                |
| V <sub>TRM</sub> | TERMINATION Voltage for Upstream port pull up (RPU) | 3.0   | -    | 3.6   | V    |                                |
| Z <sub>DRV</sub> | Driver Output Resistance                            | -     | 13   | -     | Ω    | Steady state drive*            |
| C <sub>IN</sub>  | Transceiver Capacitance                             | -     | -    | 20    | pF   | Pin to GND                     |

### 8.12.2 USB Full-Speed PHY Characteristics

| Symbol            | Parameter                   | Min. | Typ. | Max.   | Unit | Test Conditions                                     |
|-------------------|-----------------------------|------|------|--------|------|---|
| T <sub>FR</sub>   | Rise Time                   | 4    | -    | 20     | ns   | C <sub>L</sub> =50p                                 |
| T <sub>FF</sub>   | Fall Time                   | 4    | -    | 20     | ns   | C <sub>L</sub> =50p                                 |
| T <sub>FRFF</sub> | Rise and Fall Time Matching | 90   | -    | 111.11 | %    | T <sub>FRFF</sub> =T <sub>FR</sub> /T <sub>FF</sub> |

### 8.12.3 USB High-Speed Characteristics

| Symbol            | Parameter                   | Min | Typ | Max    | Unit | Test Condition                                      |
|-------------------|-----------------------------|-----|-----|--------|------|---|
| T <sub>FR</sub>   | High Speed Driver Rise Time | 500 | -   |        | ps   | CL=5pF  |
| T <sub>FF</sub>   | High Speed Driver Fall Time | 500 | -   |        | ps   | CL=5pF  |
| T <sub>FRFF</sub> | Rise and Fall Time Matching | 90  |     | 111.11 | %    | T <sub>FRFF</sub> =T <sub>FR</sub> /T <sub>FF</sub> |

### 8.13 Ethernet Characteristics

#### 8.13.1 RMIi Interface Timing

| Symbol                | Parameter   | Min | Typ             | Max  | Unit | Test Condition |
|-----------------------|---|-----|-----------------|------|------|----------------|
| $T_{P\_RMII\_REFCLK}$ | RMII_REFCLK Period  | -   | 20.0 +/- 50 ppm | -    | ns   | -              |
| $T_{H\_RMII\_REFCLK}$ | RMII_REFCLK High Time   | 8.0 | 10.0            | 12.0 | ns   | -              |
| $T_{L\_RMII\_REFCLK}$ | RMII_REFCLK Low Time  | 8.0 | 10.0            | 12.0 | ns   | -              |
| $T_{DLY\_RMII\_TX}$   | RMII_REFCLK Rising to Valid RMII_TXEN, RMII_TXDATA0 and RMII_TXDATA1 Delay  | -   | -               | 10   | ns   | -              |
| $T_{SU\_RMII\_RX}$    | RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Setup Time to RMII_REFCLK Rising  | 5   | -               | -    | ns   | -              |
| $T_{HD\_RMII\_RX}$    | RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Hold Time from RMII_REFCLK Rising | 2   | -               | -    | ns   | -              |

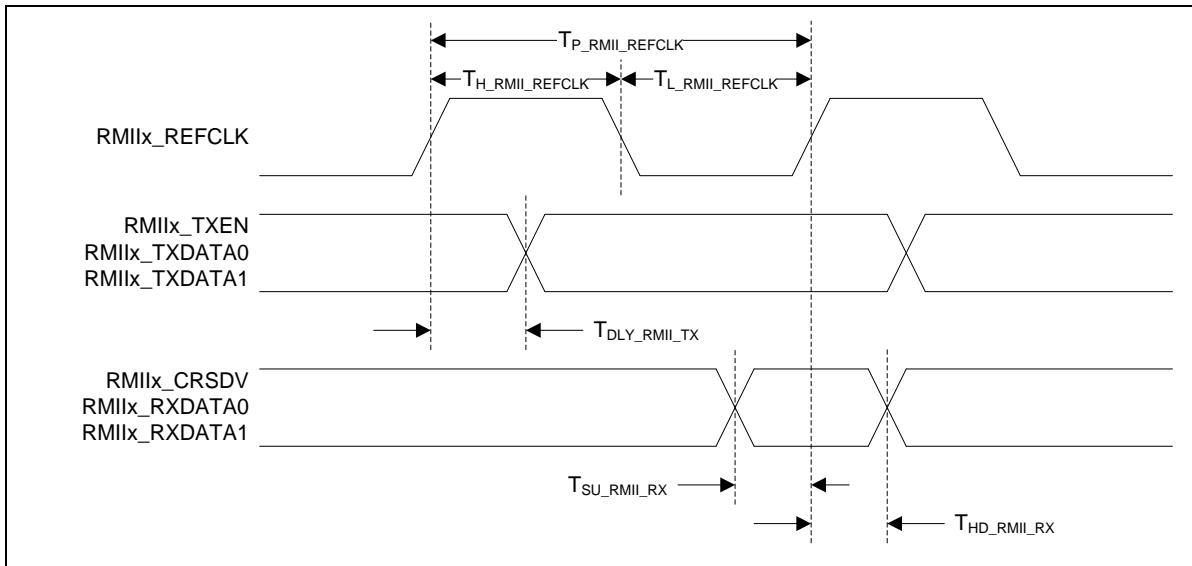


Figure 8-21 RMIi Interface Timing Diagram

8.13.2 Ethernet PHY Management Interface Timing

| Symbol                  | Parameter                                 | Min | Typ | Max | Unit | Test Condition |
|-------------------------|---|-----|-----|-----|------|----------------|
| $T_{P\_RMII\_MDC}$      | RMII_MDC Period                           | 400 | -   | -   | ns   | -              |
| $T_{H\_RMII\_MDC}$      | RMII_MDC High Time                        | 200 | -   | -   | ns   | -              |
| $T_{L\_RMII\_MDC}$      | RMII_MDC Low Time                         | 200 | -   | -   | ns   | -              |
| $T_{DLY\_RMII\_MDIOWR}$ | RMII_MDC Falling to Valid RMII_MDIO Delay | -   | -   | 10  | ns   | -              |
| $T_{SU\_RMII\_MDIORD}$  | RMII_MDIO Setup Time to RMII_MDC Rising   | 10  | -   | -   | ns   | -              |
| $T_{HD\_RMII\_MDIORD}$  | RMII_MDIO Hold Time from RMII_MDC Rising  | 10  | -   | -   | ns   | -              |

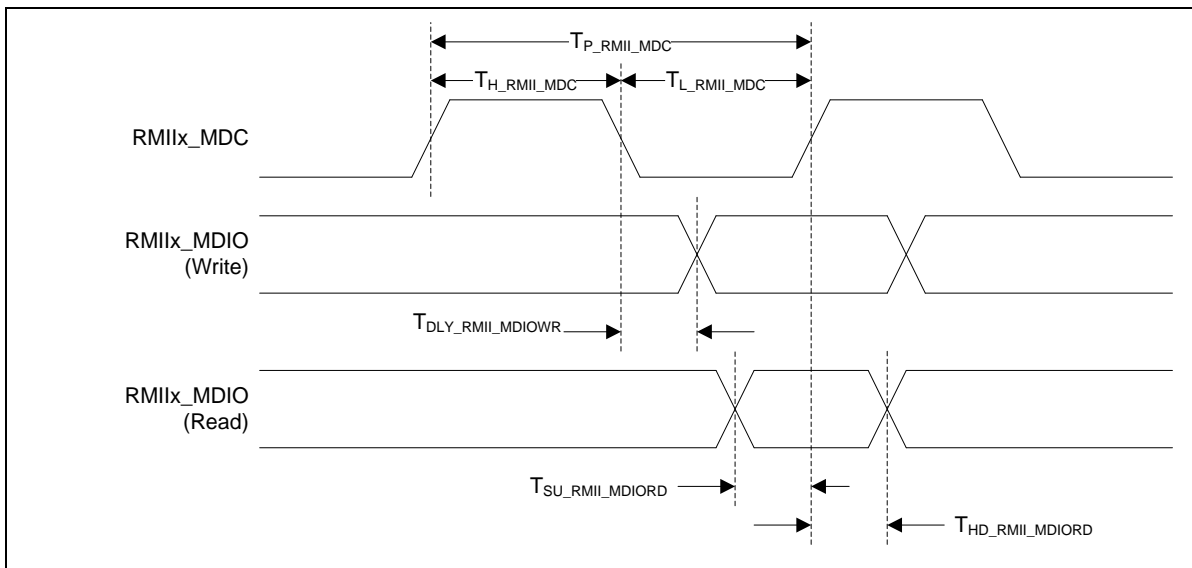


Figure 8-22 Ethernet PHY Management Interface Timing Diagram

### 8.14 SDIO Characteristics

#### 8.14.1 Default Mode Timing

| Symbol               | Parameter                                | Min   | Typ | Max | Unit | Test Condition |
|----------------------|--|-------|-----|-----|------|----------------|
| $T_{P\_SD\_CLK}$     | SD_CLK Period<br>(Data Transfer Mode)    | 40    | -   | -   | ns   | -              |
| $T_{P\_SD\_CLK\_ID}$ | SD_CLK Period<br>(Identification Mode)   | 2,500 | -   | -   | ns   | -              |
| $T_{H\_SD\_CLK}$     | SD_CLK High Time                         | -     | 20  | -   | ns   | -              |
| $T_{L\_SD\_CLK}$     | SD_CLK Low Time                          | -     | 20  | -   | ns   | -              |
| $T_{SU\_SD\_IN}$     | SD_DATA Setup Time to<br>SD_CLK Rising   | 5     | -   | -   | ns   | -              |
| $T_{HD\_SD\_IN}$     | SD_DATA Hold Time from<br>SD_CLK Rising  | 5     | -   | -   | ns   | -              |
| $T_{DLY\_SD\_OUT}$   | SD_CLK Falling to<br>Valid SD_DATA Delay | -     | -   | 14  | ns   | -              |

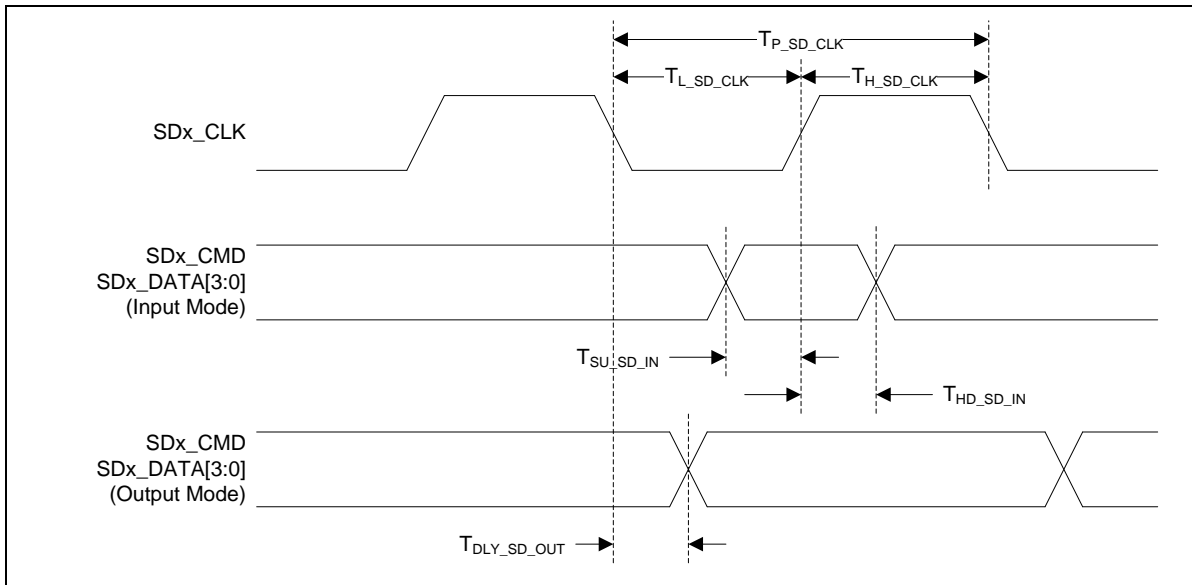


Figure 8-23 SDIO Default Mode

8.14.2 SDIO Dynamic Characteristics

| Symbol             | Parameter                             | Min | Typ | Max | Unit | Test Condition |
|--------------------|---------------------------------------|-----|-----|-----|------|----------------|
| $T_{P\_SD\_CLK}$   | SD_CLK Period                         | 20  | -   | -   | ns   | -              |
| $T_{H\_SD\_CLK}$   | SD_CLK High Time                      | 7   | -   | -   | ns   | -              |
| $T_{L\_SD\_CLK}$   | SD_CLK Low Time                       | 7   | -   | -   | ns   | -              |
| $T_{SU\_SD\_IN}$   | SD_DATA Setup Time to SD_CLK Rising   | 6   | -   | -   | ns   | -              |
| $T_{HD\_SD\_IN}$   | SD_DATA Hold Time from SD_CLK Rising  | 2   | -   | -   | ns   | -              |
| $T_{DLY\_SD\_OUT}$ | SD_CLK Falling to Valid SD_DATA Delay | -   | -   | 14  | ns   | -              |
| $T_{HD\_SD\_OUT}$  | SD_DATA Hold Time from SD_CLK Rising  | 2.5 | -   | -   | ns   | -              |

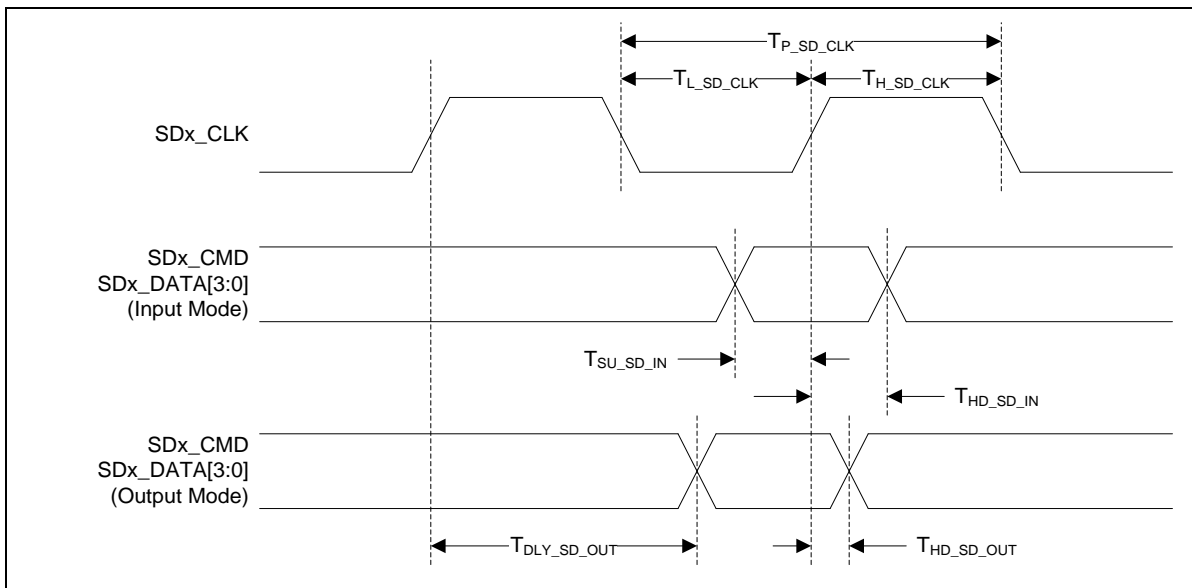


Figure 8-24 SDIO High-speed Mode



### 8.15 EBI Characteristics

#### 8.15.1 EBI Timing

| Symbol            | Parameter   | Min              | Typ | Max | Unit             | Test Condition |
|-------------------|---|------------------|-----|-----|------------------|----------------|
| $T_{IACS}$        | Address Setup Time to EBI_nCS Falling Edge            | -                | 0   | -   | $T_{HCLK}^{(1)}$ | -              |
| $T_{ICOS}$        | EBI_nCS Setup Time to EBI_nWE or EBI_nOE Falling Edge | -                | 1   | -   | $T_{HCLK}^{(1)}$ | -              |
| $T_{IACC}$        | EBI_nWE or EBI_nOE Active Low Time                    | 1 <sup>[2]</sup> | -   | 32  | $T_{HCLK}^{(1)}$ | -              |
| $T_{ICOH}$        | EBI_nCS Hold Time from EBI_nWE or EBI_nOE Rising Edge | 0                | -   | 8   | $T_{HCLK}^{(1)}$ | -              |
| $T_{SU\_EBI\_RD}$ | EBI_DATA Read Setup Time to EBI_nOE Rising Edge       | 1                | -   | -   | $T_{HCLK}^{(1)}$ | -              |

**Notes:**

1.  $T_{HCLK}$  is the period of EBI's operating clock.
2.  $T_{IACC}$  must be set for at least 21ns.

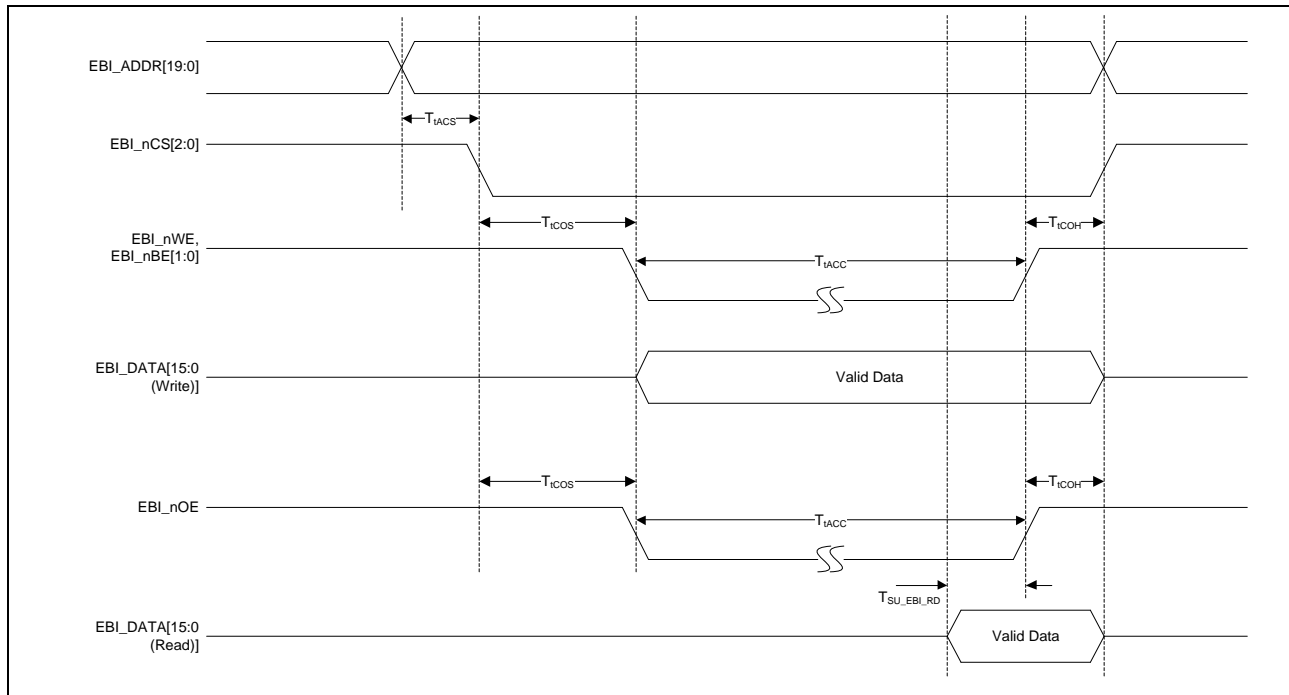


Figure 8-25 External Bus Interface Timing Diagram

8.16 SPI Flash Characteristics (M487KMCAN)

| Symbol  | Parameter                    | Min  | Typ | Max  | Unit                  | Test Condition                                      |
|---|------------------------------|------|-----|------|-----------------------|---|
| N <sub>ENDUR</sub>  | Endurance                    | 100K |     |      | cycles <sup>[1]</sup> | V <sub>DD</sub> = 3.0 V,<br>T <sub>A</sub> = +25 °C |
| T <sub>RET</sub>  | Data Retention               | 20   |     |      | year                  |   |
| T <sub>PROG</sub>   | Page Program Time(256 bytes) |      | 0.4 | 3    | ms                    |   |
| T <sub>SE</sub>   | Sector Erase Time (4KB)      |      | 45  | 400  | ms                    |   |
| T <sub>BE1</sub>  | Block Erase Time (32KB)      |      | 120 | 1600 | ms                    |   |
| T <sub>BE2</sub>  | Block Erase Time (64KB)      |      | 150 | 2000 | ms                    |   |
| T <sub>CE</sub>   | Chip Erase Time              |      | 5   | 25   | s                     |   |
| I <sub>DD1</sub>  | Current Read Data            |      | 6   | 18   | mA                    |   |
| I <sub>DD2</sub>  | Current Page Program         |      | 20  | 25   | mA                    |   |
| I <sub>DD3</sub>  | Current Sector/Block Erase   |      | 20  | 25   | mA                    |   |
| I <sub>DD3</sub>  | Current Chip Erase           |      | 20  | 25   | mA                    |   |
| <b>Note:</b> <ol style="list-style-type: none"> <li>Number of program/erase cycles.</li> <li>This table is guaranteed by design, not test in production.</li> </ol> |                              |      |     |      |                       |   |

## 9 ELECTRICAL CHARACTERISTICS FOR M48XGC/M48XE8

### 9.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

#### 9.1.1 Voltage Characteristics

| Symbol   | Description   | Min  | Max      | Unit |
|--|---|------|----------|------|
| $V_{DD}-V_{SS}[*1]$  | DC Power Supply                                       | -0.3 | 4        | V    |
| $V_{DDIO}-V_{SS}$  | $V_{DDIO}$ Power Supply                               | -0.3 | 4        | V    |
| $ V_{DDX} - V_{DD} $   | Variations between different power pins               |      | 50       | mV   |
| $ V_{DD} - AV_{DD} $   | Allowed voltage difference for $V_{DD}$ and $AV_{DD}$ |      | 50       | mV   |
| $ V_{SSX} - V_{SS} $   | Variations between different ground pins              |      | 50       | mV   |
| $ V_{SS} - AV_{SS} $   | Allowed voltage difference for $V_{SS}$ and $AV_{SS}$ |      | 50       | mV   |
| $V_{IN}$   | Input Voltage on 5V-tolerance GPIO                    |      | 5.5      | V    |
|  | Input Voltage on RTC domain (PF.6 ~ PF.11)            |      | $V_{DD}$ | V    |
|  | Input Voltage on any other pin[*2]                    |      | $V_{DD}$ | V    |
| <b>Note:</b> <ol style="list-style-type: none"> <li>All main power (<math>V_{DD}</math>, <math>AV_{DD}</math>) and ground (<math>V_{SS}</math>, <math>AV_{SS}</math>) pins must always be connected to the external power supply, in the permitted range.</li> <li>Non 5V-tolerance PIN: PA.8 ~ 15; PB.0 ~ 15; PD.10, 11, 12; PF.2, 3, 4, 5; All USB High Speed PIN and nRESET PIN.</li> </ol> |   |      |          |      |

Table 9.1-1 Voltage Characteristics

9.1.2 Current Characteristics

| Symbol                       | Description   | Min | Max | Unit |
|------------------------------|---|-----|-----|------|
| $\Sigma I_{DD}^{[*1]}$       | Maximum current into $V_{DD}$                             | -   | 200 | mA   |
| $I_{DDIO}$                   | Maximum Current into $V_{DDIO}$                           | -   | 100 |      |
| $I_{BAT}$                    | Maximum Current into $V_{BAT}$                            | -   | 100 |      |
| $\Sigma I_{SS}$              | Maximum current out of $V_{SS}$                           | -   | 100 |      |
| $I_{IO}$                     | Maximum current sunk by a I/O Pin                         | -   | 20  |      |
|                              | Maximum current sourced by a I/O Pin                      | -   | 20  |      |
|                              | Maximum current sunk by total I/O Pins <sup>[*2]</sup>    | -   | 100 |      |
|                              | Maximum current sourced by total I/O Pins <sup>[*2]</sup> | -   | 100 |      |
| $I_{INJ(PIN)}^{[*3]}$        | Maximum injected current by a I/O Pin                     | -   | ±5  |      |
| $\Sigma I_{INJ(PIN)}^{[*3]}$ | Maximum injected current by total I/O Pins                | -   | ±25 |      |

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by  $V_{IN} > A_{VDD}$  and a negative injection is caused by  $V_{IN} < V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 9.1-2 Current Characteristics

**9.1.3 Thermal Characteristics**

The average junction temperature can be calculated by using the following equation:

$$T_J = T_A + (P_D \times \theta_{JA})$$

- $T_A$  = ambient temperature (°C)
- $\theta_{JA}$  = thermal resistance junction-ambient (°C/Watt)
- $P_D$  = sum of internal and I/O power dissipation

| Symbol   | Description   | Min | Typ  | Max | Unit    |
|--|---|-----|------|-----|---------|
| $T_A$  | Operating ambient temperature                                 | -40 | -    | 105 | °C      |
| $T_J$  | Operating junction temperature                                | -40 | -    | 125 |         |
| $T_{ST}$   | Storage temperature   | -65 | -    | 150 |         |
|  | Thermal resistance junction-ambient<br>33-pin QFN(5x5 mm)     | -   | 39.6 | -   | °C/Watt |
|  | Thermal resistance junction-ambient<br>48-pin LQFP(7x7 mm)    | -   | 60   | -   | °C/Watt |
|  | Thermal resistance junction-ambient<br>64-pin LQFP(7x7 mm)    | -   | 58   | -   | °C/Watt |
|  | Thermal resistance junction-ambient<br>128-pin LQFP(14x14 mm) | -   | 38.5 | -   | °C/Watt |
| <b>Note:</b>   |   |     |      |     |         |
| 2. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions |   |     |      |     |         |

Table 9.1-3 Thermal Characteristics

**9.1.4 EMC Characteristics**

**9.1.4.1 Electrostatic discharge (ESD)**

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

**9.1.4.2 Static latchup**

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

**9.1.4.3 Electrical fast transients (EFT)**

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

| Symbol     | Description  | Conditions   | Maximum Value | Unit |
|------------|--|--|---------------|------|
| $V_{EFTB}$ | 1. Fast transient voltage burst limits to be applied through 100 pF + 47uF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance<br>2. to be applied through 2.2uF on LDO_Pin and $V_{SS}$ pins | $V_{DD} = 3.3\text{ V}$ , LQFP128, $T_A = +25\text{ }^\circ\text{C}$ , $f_{HCLK} = 192\text{ MHz}$ | 4.4           | kV   |

Table 9.1-4 EMS Characteristics

| Symbol   | Ratings   | Conditions                        | Maximum Value | Unit |
|--|---|-----------------------------------|---------------|------|
| $V_{ESD(HBM)}$   | Electrostatic discharge voltage (human body model)    | $T_A = +25\text{ }^\circ\text{C}$ | $2^{[1]}$     | kV   |
| $V_{ESD(CDM)}$   | Electrostatic discharge voltage (charge device model) | $T_A = +25\text{ }^\circ\text{C}$ | $0.5^{[1]}$   |      |
| <b>Note:</b><br>2. Guaranteed by characterization results, not tested in production. |   |                                   |               |      |

Table 9.1-5 ESD Characteristics

| Symbol   | Parameter             | Conditions                      | Value | Unit |
|--|-----------------------|---------------------------------|-------|------|
| LU   | Static latch-up class | $T_A +25\text{ }^\circ\text{C}$ | 400mA | mA   |
| <b>Note:</b><br>1. Guaranteed by characterization results, not tested in production. |                       |                                 |       |      |

Table 9.1-6 Electrical Characteristics

**9.1.5 Package Moisture Sensitivity(MSL)**

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

| Pacakge  | MSL   |
|--|-------|
| 33-pin QFN(5x5 mm) <sup>[*1]</sup>             | MSL 3 |
| 48-pin LQFP(7x7 mm) <sup>[*1]</sup>            | MSL 3 |
| 64-pin LQFP(7x7 mm) <sup>[*1]</sup>            | MSL 3 |
| 128-pin LQFP(14x14 mm) <sup>[*1]</sup>         | MSL 3 |
| <b>Note:</b>                                   |       |
| 2. Determined according to IPC/JEDEC J-STD-020 |       |

Table 9.1-7 Package Moisture Sensitivity(MSL)

9.1.6 Soldering Profile

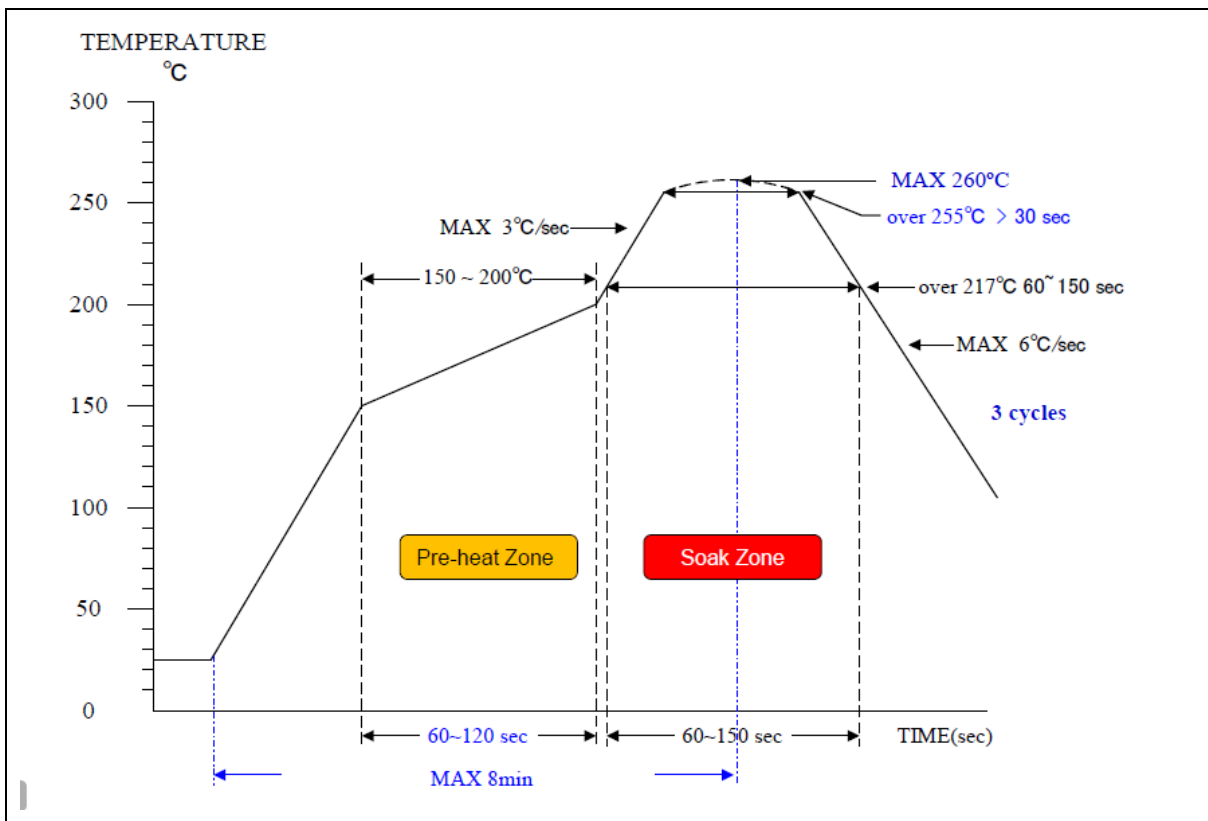


Figure 9-1 Soldering Profile From J-STD-020C

| Porfile Feature                                       | Pb Free Package     |
|---|---------------------|
| Average ramp-up rate (217°C to peak)                  | 3°C/sec. max        |
| Preheat temperature 150°C ~200°C                      | 60 sec. to 120 sec. |
| Temperature maintained above 217°C                    | 60 sec. to 150 sec. |
| Time with 5°C of actual peak temperature              | > 30 sec.           |
| Peak temperature range                                | 260°C               |
| Ramp-down rate  | 6°C/sec ax.         |
| Time 25°C to peak temperature                         | 8 min. max          |
| <b>Note:</b><br>2. Determined according to J-STD-020C |                     |

Table 9.1-8 Soldering Profile



9.2 General Operating Conditions

(V<sub>DD</sub>-V<sub>SS</sub> = 1.8 ~ 3.6V, T<sub>A</sub> = 25°C, HCLK = 192 MHz unless otherwise specified.)

| Symbol  | Parameter   | Min             | Typ  | Max              | Unit | Test Conditions  |
|---|---|-----------------|------|------------------|------|--|
| T <sub>A</sub>  | Temperature   | -40             | -    | 105              | °C   |  |
| f <sub>HCLK</sub>   | Internal AHB clock frequency  | -               | -    | 192              | MHz  |  |
| V <sub>DD</sub>   | Operation voltage   | 1.8             | -    | 3.6              | V    |  |
| V <sub>DDIO</sub>   | V <sub>DDIO</sub> Operation voltage                                       | 1.8             | -    | 3.6              |      |  |
| V <sub>BAT</sub>  | V <sub>BAT</sub> Operation voltage  | 1.8             | -    | 3.6              |      |  |
| AV <sub>DD</sub> <sup>[*1]</sup>  | Analog operation voltage  | V <sub>DD</sub> |      |                  |      |  |
| V <sub>REF</sub>  | Analog reference voltage  | 1.8             | -    | AV <sub>DD</sub> |      |  |
| V <sub>LDO</sub>  | LDO output voltage  | -               | 1.26 | -                |      |  |
| V <sub>BG</sub>   | Band-gap voltage  | 1.17            |      | 1.23             |      |  |
| C <sub>LDO</sub> <sup>[*2]</sup>  | LDO output capacitor on each pin  | 1               |      |                  |      | μF   |
|   |   | 2.2             |      |                  | μF   | LQFP48/QFN32   |
| R <sub>ESR</sub> <sup>[*3]</sup>  | ESR of C <sub>LDO</sub> output capacitor                                  | 0.1             | -    | 10               | Ω    |  |
| I <sub>RUSH</sub> <sup>[*3]</sup>   | InRush current on voltage regulator power-on (POR or wakeup from Standby) | -               | 150  | -                | mA   |  |
| E <sub>RUSH</sub> <sup>[*3]</sup>   | InRush energy on voltage regulator power-on (POR or wakeup from Standby)  | -               | 3.65 | -                | μC   | V <sub>DD</sub> = 1.8 V, T <sub>A</sub> = 105 °C, I <sub>RUSH</sub> = 146 mA for 25 μs |
| <b>Note:</b>  |   |                 |      |                  |      |  |
| 1. It is recommended to power V <sub>DD</sub> and AV <sub>DD</sub> from the same source. A maximum difference of 0.3 V between V <sub>DD</sub> and AV <sub>DD</sub> can be tolerated during power-on and power-off operation .<br>2. To ensure stability, an external 1 μF output capacitor, C <sub>LDO</sub> must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.<br>3. Guaranteed by design, not tested in production |   |                 |      |                  |      |  |

Table 9.2-1 General Operating Conditions

### 9.3 DC Electrical Characteristics

#### 9.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for  $V_{DD} = 3.6\text{ V}$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25\text{ }^\circ\text{C}$  and  $V_{DD} = 1.8\text{--}3.6\text{ V}$  unless otherwise specified.
- $V_{DD} = AV_{DD} = V_{DDIO} = V_{BAT}$
- When the peripherals are enabled HCLK is the system clock,  $f_{PCLK0,1} = f_{HCLK}/2$ .
- Program run while(1){} from Flash

| Symbol              | Conditions   | F <sub>HCLK</sub> | Typ <sup>[1]</sup>     | Max <sup>[1][2]</sup>   |                        |                         |    | Unit |
|---------------------|--|-------------------|------------------------|-------------------------|------------------------|-------------------------|----|------|
|                     |  |                   | T <sub>A</sub> = 25 °C | T <sub>A</sub> = -40 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 105 °C |    |      |
| I <sub>DD_RUN</sub> | Normal run mode, executed from Flash, all peripherals disable<br>HIRC, PLL, HXT, LIRC or LXT clock | 192 MHz           | 25.14                  | 24.11                   | 26.95                  | 54.03                   | mA |      |
|                     |  | 160 MHz           | 21.4                   | 20.27                   | 23.1                   | 49.66                   |    |      |
|                     |  | 144 MHz           | 19.19                  | 17.94                   | 20.86                  | 47                      |    |      |
|                     |  | 120 MHz           | 17.4                   | 17                      | 19.39                  | 45.94                   |    |      |
|                     |  | 12 MHz            | 3.1                    | 2.36                    | 4.55                   | 29.92                   |    |      |
|                     |  | 32.768 kHz        | 1.54                   | 0.99                    | 3.11                   | 28.20                   |    |      |
|                     |  | 10 kHz            | 1.07                   | 0.39                    | 2.63                   | 27.6                    |    |      |
|                     | Normal run mode, executed from Flash, all peripherals enable<br>HIRC, PLL, HXT, LIRC or LXT clock  | 192 MHz           | 44.72                  | 44.30                   | 47.09                  | 75.48                   |    |      |
|                     |  | 160 MHz           | 40.41                  | 35.78                   | 42.74                  | 66.58                   |    |      |
|                     |  | 144 MHz           | 33.93                  | 33.65                   | 35.84                  | 63.83                   |    |      |
|                     |  | 120 MHz           | 28.53                  | 27.99                   | 30.41                  | 57.68                   |    |      |
|                     |  | 12 MHz            | 4.63                   | 4.14                    | 6.13                   | 32.02                   |    |      |
|                     |  | 32.768 kHz        | 1.85                   | 1.30                    | 3.5                    | 28.82                   |    |      |
|                     |  | 10 kHz            | 1.39                   | 0.73                    | 3.01                   | 28.11                   |    |      |

**Note:**

1. When analog peripheral blocks such as ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 9.3-1 Current Consumption in Normal Run Mode

| Symbol               | Conditions  | F <sub>HCLK</sub> | Typ <sup>[1]</sup>     | Max <sup>[1][2]</sup>   |                        |                         | Unit |
|----------------------|---|-------------------|------------------------|-------------------------|------------------------|-------------------------|------|
|                      |   |                   | T <sub>A</sub> = 25 °C | T <sub>A</sub> = -40 °C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 105 °C |      |
| I <sub>DD_IDLE</sub> | Idle mode, all peripherals disable<br>HIRC, PLL, HXT, LIRC or LXT clock | 192 MHz           | 8.92                   | 7.95                    | 10.40                  | 36.28                   | mA   |
|                      |   | 160 MHz           | 7.82                   | 6.92                    | 9.27                   | 35.06                   |      |
|                      |   | 144 MHz           | 7.29                   | 6.41                    | 8.78                   | 34.46                   |      |
|                      |   | 120 MHz           | 6.47                   | 5.63                    | 7.95                   | 33.56                   |      |
|                      |   | 12 MHz            | 2.15                   | 1.5                     | 3.61                   | 28.9                    |      |
|                      |   | 32.768 kHz        | 1.54                   | 0.99                    | 3.11                   | 28.18                   |      |
|                      |   | 10 kHz            | 1.07                   | 0.68                    | 2.63                   | 27.58                   |      |
|                      | Idle mode, all peripherals enable<br>HIRC, PLL, HXT, LIRC or LXT clock  | 192 MHz           | 30.59                  | 29.51                   | 32.44                  | 59.22                   |      |
|                      |   | 160 MHz           | 25.95                  | 24.95                   | 27.72                  | 54.28                   |      |
|                      |   | 144 MHz           | 23.63                  | 22.67                   | 25.37                  | 51.83                   |      |
|                      |   | 120 MHz           | 20.13                  | 19.25                   | 21.82                  | 48.15                   |      |
|                      |   | 12 MHz            | 3.80                   | 3.1                     | 5.36                   | 30.80                   |      |
|                      |   | 32.768 kHz        | 1.88                   | 1.31                    | 3.49                   | 28.74                   |      |
|                      |   | 10 kHz            | 1.39                   | 1.01                    | 3.01                   | 28.12                   |      |

**Note:**

1. When analog peripheral blocks such as ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 9.3-2 Current Consumption in Idle Mode

| Symbol               | Test Conditions   | LXT <sup>[1]</sup><br>32.768<br>kHz | LIRC<br>10<br>kHz | Typ <sup>[2]</sup><br>T <sub>A</sub> = 25<br>°C | Max <sup>[3][4]</sup>      |                        |                         | Unit |
|----------------------|---|-------------------------------------|-------------------|---|----------------------------|------------------------|-------------------------|------|
|                      |   |                                     |                   |   | T <sub>A</sub> = -40<br>°C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 105 °C |      |
| I <sub>DD_DPD</sub>  | Deep Power-down mode, all peripherals disable                                   | -                                   | -                 | 0.35  | 0.15                       | 1.1                    | 18.5                    | μA   |
|                      | Deep Power-down mode, RTC enable  | V                                   | -                 | 0.81  | 0.62                       | 1.59                   | 19                      |      |
| I <sub>DD_SPD</sub>  | Standby Power-down mode, all peripherals disabled                               | -                                   | -                 | 1.48  | 0.98                       | 3.45                   | 404                     | μA   |
|                      | Standby Power-down mode, RTC enable   | V                                   | -                 | 1.95  | 1.46                       | 3.95                   | 405                     |      |
|                      | Standby Power-down mode, RTC enable<br>RTC with LIRC10k                         | -                                   | V                 | 1.93  | 1.3                        | 4.17                   | 406                     |      |
|                      | Standby Power-down mode with 16 KB RAM retention:                               | -                                   | -                 | 5.89  | 1.6                        | 14.15                  | 524                     |      |
|                      | Standby Power-down mode with 32 KB RAM retention:                               | -                                   | -                 | 10.19   | 2.11                       | 25.46                  | 814                     |      |
|                      | Standby Power-down mode with 64 KB RAM retention:                               | -                                   | -                 | 18.35   | 3.19                       | 46.86                  | 1374                    |      |
|                      | Standby Power-down mode with 128 KB RAM retention:                              | -                                   | -                 | 34.42   | 5.31                       | 120.4                  | 2804                    |      |
| I <sub>DD_LLPD</sub> | Low leakage Power-down mode, all peripherals disabled                           | -                                   | -                 | 230   | 52.65                      | 682                    | 19161                   | μA   |
|                      | Low leakage Power-down mode, RTC/WDT/Timer/UART enable                          | V                                   | -                 | 231   | 54.23                      | 683                    | 19270                   |      |
|                      | Low leakage Power-down mode, RTC/WDT/Timer enable<br>RTC/WDT/Timer with LIRC10k | -                                   | V                 | 230   | 54.16                      | 681                    | 19301                   |      |
|                      | Low leakage Power-down mode, WDT/Timer use LIRC, RTC/UART use LXT               | V                                   | V                 | 232   | 54.32                      | 685                    | 19334                   |      |
| I <sub>DD_NPD</sub>  | Normal-Power-down mode, all peripherals disable                                 | -                                   | -                 | 672   | 185                        | 2062                   | 32045                   | μA   |
|                      | Normal-Power-down mode, WDT/Timer/UART/RTC enable                               | V                                   | -                 | 677   | 187                        | 2090                   | 32167                   |      |
|                      | Normal-Power-down mode, WDT/Timer/UART enable<br>RTC/WDT/Timer with LIRC10k     | -                                   | V                 | 677   | 186                        | 2091                   | 32121                   |      |
|                      | Normal-Power-down mode, WDT use LIRC, UART/Timer/RTC use LXT                    | V                                   | V                 | 678   | 187                        | 2092                   | 32165                   |      |

| Symbol   | Test Conditions   | LXT <sup>[1]</sup><br>32.768<br>kHz | LIRC<br>10<br>kHz | Typ <sup>[2]</sup><br>T <sub>A</sub> = 25<br>°C | Max <sup>[3][4]</sup>      |                        |                         | Unit |
|--|---|-------------------------------------|-------------------|---|----------------------------|------------------------|-------------------------|------|
|  |   |                                     |                   |   | T <sub>A</sub> = -40<br>°C | T <sub>A</sub> = 25 °C | T <sub>A</sub> = 105 °C |      |
| I <sub>DD_FWPD</sub>   | Fast wake up Power-down mode, all peripherals disable                             | -                                   | -                 | 793   | 291                        | 2204                   | 32308                   | μA   |
|  | Fast wake up Power-down mode, WDT/Timer/UART/RTC enable                           | V                                   | -                 | 797   | 293                        | 2216                   | 32403                   |      |
|  | Fast wake up Power-down mode, WDT/Timer/UART enable<br>RTC/WDT/Timer with LIRC10k | -                                   | V                 | 796   | 293                        | 2212                   | 32357                   |      |
|  | Fast wake up Power-down mode, WDT use LIRC, UART/Timer/RTC use LXT                | V                                   | V                 | 796   | 293                        | 2213                   | 32383                   |      |
| <b>Note:</b> <ol style="list-style-type: none"> <li>Crystal used: AURUM XF66RU000032C0 with a C<sub>L</sub> of 20 pF for L3 gain level</li> <li>V<sub>DD</sub> = AV<sub>DD</sub> = 3.3V.</li> <li>Based on characterization, not tested in production unless otherwise specified.</li> <li>When analog peripheral blocks such as ADC and ACMP are ON, an additional power consumption should be considered.</li> <li>Based on characterization, tested in production.</li> </ol> |   |                                     |                   |   |                            |                        |                         |      |

Table 9.3-3 Chip Current Consumption in Power-down Mode

**9.3.2 On-Chip Peripheral Current Consumption**

- The typical values for  $T_A = 25\text{ }^\circ\text{C}$  and  $V_{DD} = AV_{DD} = 3.3\text{ V}$  unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock,  $f_{HCLK} = 192\text{ MHz}$ ,  $f_{PCLK0, 1} = f_{HCLK}/2$ .
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

| Peripheral        | $I_{DD}^{[*1]}$ | Unit |
|-------------------|-----------------|------|
| PDMA              | 1166.72         | μA   |
| EBI               | 231.78          |      |
| SDH0              | 1233.37         |      |
| CRC               | 63.38           |      |
| CCAP              | 1199.17         |      |
| USBH              | 858.77          |      |
| SDH1              | 59.21           |      |
| WDT               | 45.9            |      |
| RTC               | 127.59          |      |
| TMR0              | 361.64          |      |
| TMR1              | 352.25          |      |
| TMR2              | 314.95          |      |
| TMR3              | 295.1           |      |
| CLKO              | 84.24           |      |
| ACMP01            | 60.76           |      |
| I <sup>2</sup> C0 | 28.94           |      |
| I <sup>2</sup> C1 | 17.5            |      |
| I <sup>2</sup> C2 | 48.25           |      |
| QSPI0             | 575.19          |      |
| QSPI1             | 418.16          |      |
| SPI0              | 560.07          |      |
| SPI1              | 595.36          |      |
| SPI2              | 619             |      |
| UART0             | 272.94          |      |
| UART1             | 208.76          |      |
| UART2             | 263.46          |      |
| UART3             | 170.93          |      |
| UART4             | 211.44          |      |
| UART5             | 169.76          |      |

| Peripheral        | I <sub>DD</sub> <sup>[1]</sup> | Unit |
|-------------------|--------------------------------|------|
| UART6             | 168.87                         |      |
| UART7             | 192.85                         |      |
| CAN0              | 236.13                         |      |
| CAN1              | 216.79                         |      |
| CAN2              | 211.6                          |      |
| USB FS OTG        | 333.04                         |      |
| EADC0             | 391.46                         |      |
| EADC1             | 308.99                         |      |
| I <sup>2</sup> S0 | 307.91                         |      |
| SC0               | 212.34                         |      |
| DAC               | 35.64                          |      |
| EPWM0             | 364.43                         |      |
| EPWM1             | 333.4                          |      |
| BPWM0             | 363.07                         |      |
| BPWM1             | 278.82                         |      |
| QEI0              | 51.81                          |      |
| QEI1              | 34.86                          |      |
| TRNG              | 311.47                         |      |
| ECAP0             | 66.53                          |      |
| ECAP1             | 35.24                          |      |

**Note:**

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.

Table 9.3-4 Peripheral Current Consumption

**9.3.3 Wakeup Time from Low-Power Modes**

The wakeup times given in Table 9.3-5 is measured on a wakeup phase with a 12 MHz HIRC oscillator.

| Symbol   | Parameter                               | Typ | Unit   |
|--|---|-----|--------|
| t <sub>WU_IDLE</sub>   | Wakeup from IDLE mode                   | 5   | cycles |
| t <sub>WU_FWPD</sub>   | Wakeup from Fast-wakeup power down mode | 10  | μs     |
| t <sub>WU_PD</sub>   | Wakeup from normal power down mode      | 15  |        |
| t <sub>WU_LLDP</sub>   | Wakeup from low leakage power down mode | 58  |        |
| t <sub>WU_SPD</sub>  | Wakeup from Standby Power-down mode     | 200 |        |
| t <sub>WU_DPD</sub>  | Deep Power-down mode (DPD)              | 200 |        |
| <b>Note:</b><br>1. Based on test during characterization, not tested in production.<br>2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first |   |     |        |

Table 9.3-5 Low-power Mode Wake-up Timings



### 9.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below  $V_{SS}$  or above  $V_{DD}$  should be avoided during normal product operation. However, the analog component of the MCU is most likely to be affected by the injection current, but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to  $V_{DD}$ ) to pins that include analog function which may potentially injection currents.

| Symbol         | Parameter                     | Negative Injection | Positive Injection | Unit | Test Condition   |
|----------------|-------------------------------|--------------------|--------------------|------|--|
| $I_{INJ(PIN)}$ | Injected current by a I/O Pin | -0                 | 0                  | mA   | Injected current on nReset pins  |
|                |                               | -0                 | 0                  |      | Injected current on PF2~PF5, PA10, PA11 and PB0~PB15 for analog input function |
|                |                               | -5                 | +5                 |      | Injected current on any other I/O except analog input pin                      |

Table 9.3-6 I/O Current Injection Characteristics

### 9.3.5 I/O DC Characteristics

#### 9.3.5.1 PIN Input Characteristics

| Symbol  | Parameter                            | Min                | Typ                | Max                | Unit          | Test Conditions   |
|---|--------------------------------------|--------------------|--------------------|--------------------|---------------|---|
| $V_{IL}$  | Input low voltage (Schmitt trigger)  | 0                  | -                  | $0.3 \cdot V_{DD}$ | V             |   |
|   | Input low voltage (TTL trigger)      | 0                  | -                  | 0.7                |               | $V_{DD} = 2.7\text{ V}$   |
|   |                                      | 0                  | -                  | 0.5                |               | $V_{DD} = 1.8\text{ V}$   |
| $V_{IH}$  | Input high voltage (Schmitt trigger) | $0.7 \cdot V_{DD}$ | -                  | $V_{DD}$           | V             |   |
|   | Input high voltage (TTL trigger)     | 1.5                | -                  | $V_{DD}$           |               | $V_{DD} = 3.3\text{ V}$   |
|   |                                      | 0.8                | -                  | $V_{DD}$           |               | $V_{DD} = 1.8\text{ V}$   |
| $V_{HY}^{[1]}$  | Hysteresis voltage of schmitt input  | -                  | $0.2 \cdot V_{DD}$ | -                  | V             |   |
| $I_{LK}^{[2]}$  | Input leakage current                | -1                 |                    | 1                  | $\mu\text{A}$ | $V_{SS} < V_{IN} < V_{DD}$ ,<br>Open-drain or input only mode                                 |
|   |                                      | -1                 |                    | 1                  |               | $V_{DD} < V_{IN} < 5\text{ V}$ , Open-drain or input only mode on any other 5v tolerance pins |
| $R_{PU}^{[1]}$  | Pull up resistor                     | 45                 | 52                 | 57                 | k $\Omega$    |   |
| $R_{PD}^{[1]}$  | Pull down resistor                   | 45                 | 52                 | 57                 | k $\Omega$    |   |
| <b>Note:</b>  |                                      |                    |                    |                    |               |   |
| 1. Guaranteed by characterization result, not tested in production.               |                                      |                    |                    |                    |               |   |
| 2. Leakage could be higher than the maximum value, if abnormal injection happens. |                                      |                    |                    |                    |               |   |

Table 9.3-7 I/O Input Characteristics

9.3.5.2 I/O Output Characteristics

| Symbol            | Parameter  | Min   | Typ | Max   | Unit    | Test Conditions                                 |
|-------------------|--|-------|-----|-------|---------|---|
| $I_{SR}^{[1][2]}$ | Source current for quasi-bidirectional mode and high level | 6.91  |     | 7.76  | $\mu A$ | $V_{DD} = 3.3 V$<br>$V_{IN} = (V_{DD} - 0.4) V$ |
|                   |  | 6.79  |     | 7.59  | $\mu A$ | $V_{DD} = 1.8 V$<br>$V_{IN} = (V_{DD} - 0.4) V$ |
|                   | Source current for push-pull mode and high level           | 16.98 |     | 17.40 | mA      | $V_{DD} = 3.3 V$<br>$V_{IN} = (V_{DD} - 0.4) V$ |
|                   |  | 9.85  |     | 10.19 | mA      | $V_{DD} = 1.8 V$<br>$V_{IN} = (V_{DD} - 0.4) V$ |
| $I_{SK}^{[1][2]}$ | Sink current for push-pull mode and low level              | 16.21 |     | 16.63 | mA      | $V_{DD} = 3.3 V$<br>$V_{IN} = 0.4 V$            |
|                   |  | 9.59  |     | 10.41 | mA      | $V_{DD} = 1.8 V$<br>$V_{IN} = 0.4 V$            |
| $C_{IO}^{[1]}$    | I/O pin capacitance  | -     | 5   | -     | pF      |   |

**Note:**

- Guaranteed by characterization result, not tested in production.
- The  $I_{SR}$  and  $I_{SK}$  must always respect the absolute maximum current and the sum of I/O, CPU and peripheral must not exceed  $\Sigma I_{DD}$  and  $\Sigma I_{SS}$ .

Table 9.3-8 I/O Output Characteristics

9.3.5.3 nRESET Input Characteristics

| Symbol          | Parameter                        | Min                | Typ | Max                | Unit       | Test Conditions              |
|-----------------|----------------------------------|--------------------|-----|--------------------|------------|------------------------------|
| $V_{ILR}$       | Negative going threshold, nRESET | -                  | -   | $0.3 \cdot V_{DD}$ | V          |                              |
| $V_{IHR}$       | Positive going threshold, nRESET | $0.7 \cdot V_{DD}$ | -   | -                  | V          |                              |
| $R_{RST}^{[1]}$ | Internal nRESET pull up resistor | 45                 | 52  | 47                 | k $\Omega$ |                              |
| $t_{FR}^{[1]}$  | nRESET input filtered pulse time | -                  | 24  | -                  | $\mu s$    | Normal run and Idle mode     |
|                 |                                  | -                  | 24  | -                  |            | Fast wake up Power-down mode |
|                 |                                  | 75                 | -   | 155                |            | Power-down mode              |

**Note:**

- Guaranteed by characterization result, not tested in production.
- It is recommended to add a 10 k $\Omega$  and 10 $\mu F$  capacitor at nRESET pin to keep reset signal stable.

Table 9.3-9 nRESET Input Characteristics

9.4 AC Electrical Characteristics

9.4.1 48 MHz Internal High Speed RC Oscillator (HIRC48M)

The 48 MHz RC oscillator is calibrated in production.

| Symbol.  | Parameter                                    | Min               | Typ | Max              | Unit          | Test Conditions  |
|--|--|-------------------|-----|------------------|---------------|--|
| $V_{DD}$   | Operating voltage                            | 1.75              | -   | 3.6              | V             |  |
| $f_{HIRC}$   | Oscillator frequency                         | 47.52             | 48  | 48.48            | MHz           | $T_A = 25\text{ }^\circ\text{C}$ ,<br>$V_{DD} = 1.8 \sim 3.6\text{V}$                                  |
|  | Frequency drift over temperature and voltage | -1                | -   | 1                | %             | $T_A = 25\text{ }^\circ\text{C}$ ,<br>$V_{DD} = 1.8 \sim 3.6\text{V}$                                  |
|  |  | -4 <sup>[1]</sup> | -   | 4 <sup>[1]</sup> | %             | $T_A = -40\text{ }^\circ\text{C} \sim +105\text{ }^\circ\text{C}$ ,<br>$V_{DD} = 1.8 \sim 3.6\text{V}$ |
| $I_{HIRC}^{[1]}$   | Operating current                            | -                 | -   | 230              | $\mu\text{A}$ |  |
| $T_S^{[2]}$  | Stable time                                  | -                 | -   | 20               | $\mu\text{s}$ | $T_A = -40\text{ }^\circ\text{C} \sim +105\text{ }^\circ\text{C}$ ,<br>$V_{DD} = 1.8 \sim 3.6\text{V}$ |
| <b>Note:</b> <ol style="list-style-type: none"> <li>Guaranteed by characterization result, not tested in production.</li> <li>Guaranteed by design.</li> </ol> |  |                   |     |                  |               |  |

Table 9.4-148 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

9.4.2 12 MHz Internal High Speed RC Oscillator (HIRC)

The 12 MHz RC oscillator is calibrated in production.

| Symbol.   | Parameter                                    | Min               | Typ | Max              | Unit | Test Conditions   |
|---|--|-------------------|-----|------------------|------|---|
| V <sub>DD</sub>   | Operating voltage                            | 1.75              | -   | 3.6              | V    |   |
| F <sub>MRC</sub>  | Oscillator frequency                         | 11.76             | 12  | 12.24            | MHz  | T <sub>A</sub> = 25 °C,<br>V <sub>DD</sub> = 1.8 ~ 3.6V           |
|   | Frequency drift over temperature and voltage | -1                | -   | 1                | %    | T <sub>A</sub> = 25 °C,<br>V <sub>DD</sub> = 1.8 ~ 3.6V           |
|   |  | -3 <sup>[1]</sup> | -   | 3 <sup>[1]</sup> | %    | T <sub>A</sub> = -40°C ~ +105 °C,<br>V <sub>DD</sub> = 1.8 ~ 3.6V |
| I <sub>MRC</sub> <sup>[1]</sup>                                     | Operating current                            | -                 | -   | 215              | μA   |   |
| T <sub>S</sub> <sup>[2]</sup>                                       | Stable time                                  | -                 | -   | 20               | μs   | T <sub>A</sub> = -40°C ~ +105 °C,<br>V <sub>DD</sub> = 1.8 ~ 3.6V |
| <b>Note:</b>  |  |                   |     |                  |      |   |
| 1. Guaranteed by characterization result, not tested in production. |  |                   |     |                  |      |   |
| 2. Guaranteed by design.  |  |                   |     |                  |      |   |

Table 9.4-2 12 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

9.4.3 10 kHz Internal Low Speed RC Oscillator (LIRC)

| Symbol   | Parameter                                    | Min <sup>[*1]</sup> | Typ  | Max <sup>[*1]</sup> | Unit | Test Conditions   |
|--|--|---------------------|------|---------------------|------|---|
| V <sub>DD</sub>  | Operating voltage                            | 1.75                | -    | 3.6                 | V    |   |
| F <sub>LRC</sub> <sup>[*2]</sup>   | Oscillator frequency                         | -                   | 10   | -                   | kHz  | T <sub>A</sub> = 25 °C,<br>V <sub>DD</sub> = 1.8 ~ 3.6V                                   |
|  | Frequency drift over temperature and voltage | -1                  | -    | 1                   | %    | T <sub>A</sub> = 25 °C,<br>V <sub>DD</sub> = 1.8 ~ 3.6V                                   |
|  |  | -10                 | -    | 10                  | %    | T <sub>A</sub> = -40~105°C<br>V <sub>DD</sub> = 1.8V~3.6V<br>Without software calibration |
| I <sub>LRC</sub>   | Operating current                            | -                   | 0.85 | 1                   | μA   | V <sub>DD</sub> = 3.3V  |
| T <sub>S</sub>   | Stable time                                  | -                   | 500  | -                   | μs   | T <sub>A</sub> = -40~105°C<br>V <sub>DD</sub> = 1.8V~3.6V                                 |
| <p><b>Note:</b></p> <ol style="list-style-type: none"> <li>1. Guaranteed by characterization, not tested in production.</li> <li>2. The 10 kHz low speed RC oscillator can be calibrated by user.</li> <li>3. Guaranteed by design.</li> <li>4. The LIRC duty cycle is 16/84, if need 50/50 duty clock output, user should divided by 2 at least.</li> </ol> |  |                     |      |                     |      |   |

Table 9.4-3 10 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

**9.4.4 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) Characteristics**

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this section are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1\_IN and XT1\_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

| Symbol   | Parameter                  | Min <sup>[1]</sup> | Typ  | Max <sup>[1]</sup> | Unit | Test Conditions                                    |
|--|----------------------------|--------------------|------|--------------------|------|--|
| V <sub>DD</sub>  | Operating voltage          | 1.8                | -    | 3.6                | V    |  |
| R <sub>f</sub>   | Internal feedback resistor | -                  | 1000 | -                  | kΩ   |  |
| f <sub>HXT</sub>   | Oscillator frequency       | 4                  | -    | 24                 | MHz  |  |
| I <sub>HXT</sub>   | Current consumption        | -                  | 160  | 281                | μA   | 4 MHz, Gain = L0                                   |
|  |                            |                    | 280  | 417                |      | 12 MHz, Gain = L1                                  |
|  |                            | -                  | 400  | 540                |      | 16 MHz, Gain = L2                                  |
|  |                            | -                  | 600  | 690                |      | 24 MHz, Gain = L3                                  |
| T <sub>S</sub>   | Stable time                | -                  | 1300 | 1974               | μs   | 4 MHz, Gain = L0                                   |
|  |                            |                    | 458  | 605                |      | 12 MHz, Gain = L1                                  |
|  |                            | -                  | 326  | 439                |      | 16 MHz, Gain = L2                                  |
|  |                            | -                  | 268  | 414                |      | 24 MHz, Gain = L3                                  |
| D <sub>uHXT</sub>  | Duty cycle                 | 40                 | -    | 60                 | %    |  |
| V <sub>pp</sub>  | Peak-to-peak amplitude     | -                  | 1.47 | -                  | V    | V <sub>DD</sub> = 3.3V @ f <sub>HXT</sub> = 12 MHz |
| <b>Note:</b> <ol style="list-style-type: none"> <li>Guaranteed by characterization, not tested in production.</li> <li>Recommended crystal resonators for the HXT oscillator in M480 Series MCUs               <ol style="list-style-type: none"> <li>EPSON FA-238A 12MHz (C<sub>L</sub>=12pF, ESR= 120 Ω), X1E000341000400</li> <li>EPSON FA-238A 16MHz (C<sub>L</sub>=12pF, ESR= 80 Ω), X1E000341003900</li> <li>EPSON FA-238A 24MHz (C<sub>L</sub>=12pF, ESR= 60 Ω), X1E000341014800</li> </ol> </li> </ol> |                            |                    |      |                    |      |  |

Table 9.4-4 External 4~24 MHz High Speed Crystal (HXT) Oscillator

| Symbol   | Parameter                       | Min <sup>[*1]</sup> | Typ | Max <sup>[*1]</sup> | Unit | Test Conditions |
|--|---------------------------------|---------------------|-----|---------------------|------|-----------------|
| Rs   | Equivalent series resisotr(ESR) | -                   | -   | 150                 | Ω    | Crystal @4 MHz  |
|  |                                 |                     |     | 50                  |      | Crystal @12 MHz |
|  |                                 | -                   | -   | 40                  |      | Crystal @16 MHz |
|  |                                 | -                   | -   | 40                  |      | Crystal @24 MHz |
| <b>Note:</b>   |                                 |                     |     |                     |      |                 |
| 1. Guaranteed by characterization, not tested in production. |                                 |                     |     |                     |      |                 |

Table 9.4-5 External 4~24 MHz High Speed Crystal Characteristics

9.4.4.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 25 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

| CRYSTAL        | C1    | C2    | R1      |
|----------------|-------|-------|---------|
| 4 MHz ~ 24 MHz | 20 pF | 20 pF | without |

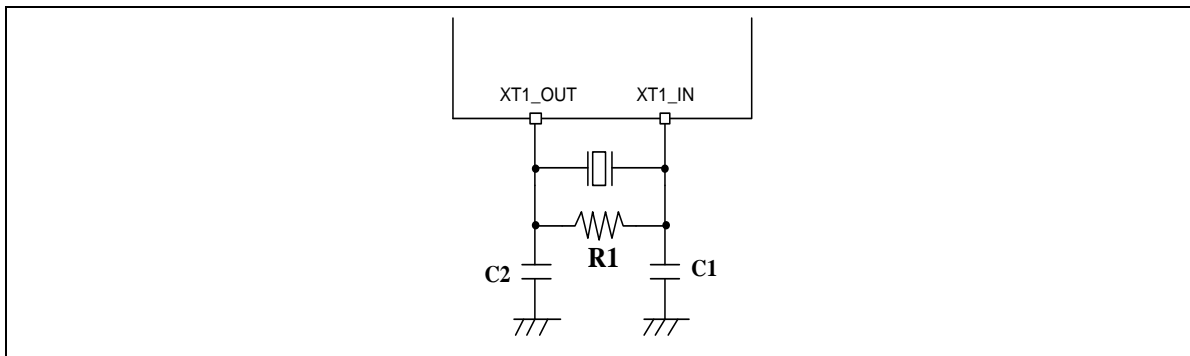


Figure 9-2 Typical Crystal Application Circuit

9.4.5 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1\_IN is a standard input pin to receive external clock. The external clock signal has to respect the Table 9.4-6. The characteristics result from tests performed using a waveform generator.

| Symbol         | Parameter                            | Min <sup>[*1]</sup> | Typ | Max <sup>[*1]</sup> | Unit | Test Conditions                         |
|----------------|--------------------------------------|---------------------|-----|---------------------|------|---|
| $f_{HXT\_ext}$ | External user clock source frequency | 4                   | -   | 24                  | MHz  |   |
| $t_{CHCX}$     | Clock high time                      | 8                   | -   | -                   | ns   |   |
| $t_{CLCX}$     | Clock low time                       | 8                   | -   | -                   | ns   |   |
| $t_{CLCH}$     | Clock rise time                      | -                   | -   | 10                  | ns   | Low (10%) to high level (90%) rise time |
| $t_{CHCL}$     | Clock fall time                      | -                   | -   | 10                  | ns   | High (90%) to low level (10%) fall time |
| $Du_{E\_HXT}$  | Duty cycle                           | 40                  | -   | 60                  | %    |   |
| $V_{IH}$       | Input high voltage                   | $0.7 \cdot V_{DD}$  | -   | $V_{DD}$            | V    |   |
| $V_{IL}$       | Input low voltage                    | $V_{SS}$            | -   | $0.3 \cdot V_{DD}$  | V    |   |

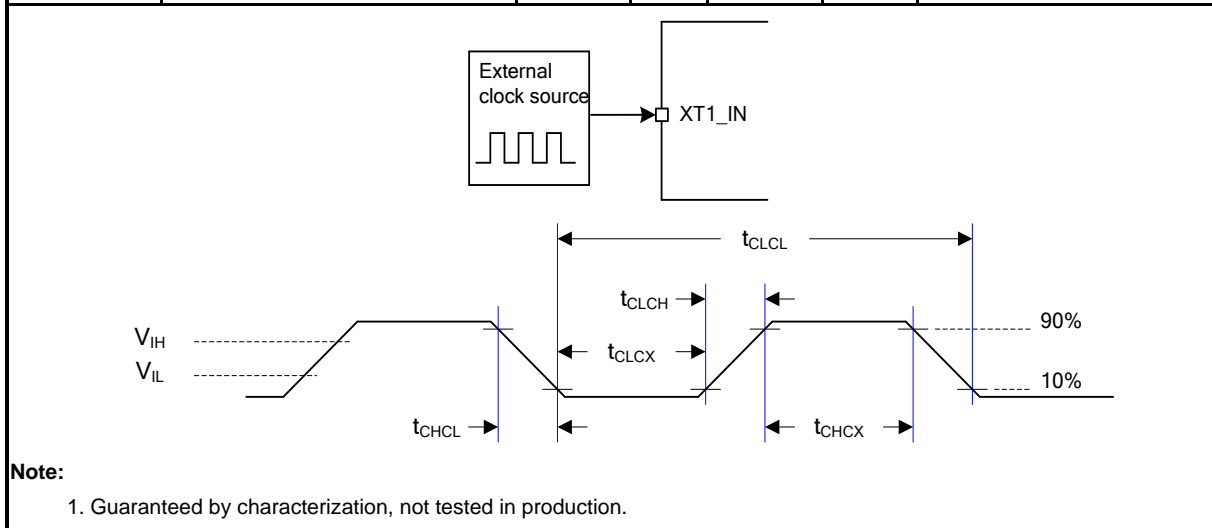


Table 9.4-6 External 4~24 MHz High Speed Clock Input Signal



9.4.6 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) Characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this section are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32\_OUT and X32\_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

| Symbol            | Parameter                  | Min <sup>[1]</sup> | Typ  | Max <sup>[1]</sup> | Unit | Test Conditions      |
|-------------------|----------------------------|--------------------|------|--------------------|------|----------------------|
| V <sub>DD</sub>   | Operation voltage          | 1.8                | -    | 3.6                | V    |                      |
| T <sub>LXT</sub>  | Temperature range          | -40                | -    | 105                | °C   |                      |
| R <sub>f</sub>    | Internal feedback resistor | -                  | 15   | -                  | MΩ   |                      |
| F <sub>LXT</sub>  | Oscillator frequency       | 32.768             |      |                    | kHz  |                      |
| I <sub>LXT</sub>  | Current consumption        | -                  | 0.25 | 0.49               | μA   | ESR=35 kΩ, Gain = L1 |
|                   |                            |                    | 0.42 | 0.8                |      | ESR=35 kΩ, Gain = L4 |
|                   |                            | -                  | 0.85 | 1.66               |      | ESR=70 kΩ, Gain = L7 |
| T <sub>SLXT</sub> | Stable time                | -                  | 1.5  | 2                  | s    |                      |
| D <sub>ULXT</sub> | Duty cycle                 | 30                 | -    | 70                 | %    |                      |

**Note:**

- Guaranteed by characterization, not tested in production.
- Recommended crystal resonators for the LXT oscillator in M480 Series MCUs
  - 2.1 EPSON FC-13A 32.768 kHz (C<sub>L</sub>= 12.5pF, ESR=70 kΩ), X1A000091000100

Table 9.4-7 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

| Symbol         | Parameter                       | Min | Typ | Max | Unit | Test Conditions     |
|----------------|---------------------------------|-----|-----|-----|------|---------------------|
| R <sub>s</sub> | Equivalent Series Resistor(ESR) | -   | 35  | 70  | kΩ   | Crystal @32.768 kHz |

Table 9.4-8 External 32.768 kHz Low Speed Crystal Characteristics

9.4.6.1 Typical Crystal Application Circuits

| CRYSTAL                 | C1    | C2    | R1      |
|-------------------------|-------|-------|---------|
| 32.768 kHz, ESR < 70 KΩ | 20 pF | 20 pF | without |

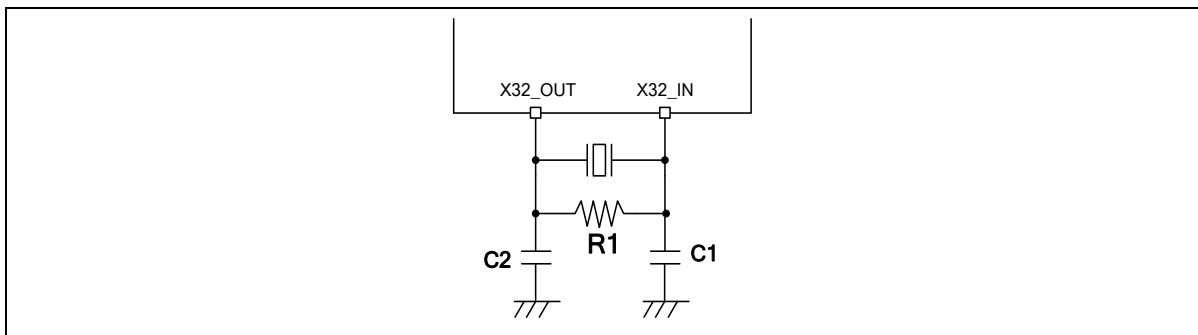


Figure 9-3 Typical 32.768 kHz Crystal Application Circuit

9.4.7 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32\_IN is a standard input pin to receive external clock. The external clock signal has to respect the Table 9.4-9. The characteristics result from tests performed using a waveform generator.

| Symbol               | Parameter                        | Min <sup>(1)</sup>  | Typ    | Max <sup>(1)</sup>  | Unit | Test Conditions                         |
|----------------------|----------------------------------|---------------------|--------|---------------------|------|---|
| f <sub>LSE_ext</sub> | External clock source frequency  | -                   | 32.768 | -                   | kHz  |   |
| t <sub>CHCX</sub>    | Clock high time                  | 450                 | -      | -                   | ns   |   |
| t <sub>CLCX</sub>    | Clock low time                   | 450                 | -      | -                   | ns   |   |
| t <sub>CLCH</sub>    | Clock rise time                  | -                   | -      | 50                  | ns   | Low (10%) to high level (90%) rise time |
| t <sub>CHCL</sub>    | Clock fall time                  | -                   | -      | 50                  | ns   | High (90%) to low level (10%) fall time |
| Du <sub>E_LXT</sub>  | Duty cycle                       | 30                  | -      | 70                  | %    |   |
| Xin_VIH              | LXT input pin input high voltage | 0.7*V <sub>DD</sub> | -      | V <sub>DD</sub>     | V    |   |
| Xin_VIL              | LXT input pin input low voltage  | V <sub>SS</sub>     | -      | 0.3*V <sub>DD</sub> | V    |   |

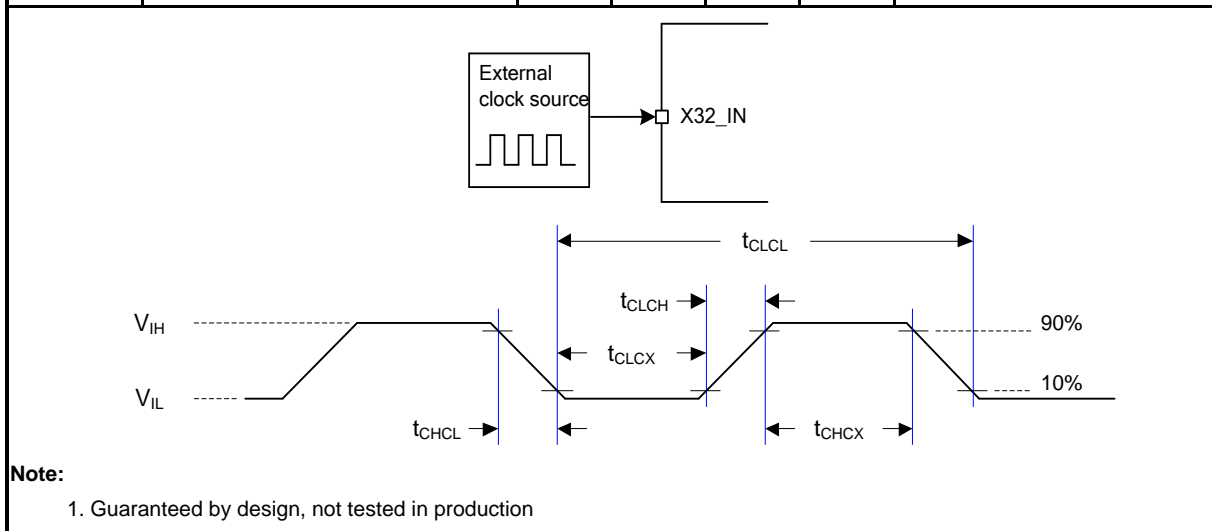


Table 9.4-9 External 32.768 kHz Low Speed Clock Input Signal

9.4.8 PLL Characteristics

| Symbol                | Parameter                         | Min <sup>[1]</sup> | Typ  | Max <sup>[1]</sup> | Unit    | Test Conditions                           |
|-----------------------|-----------------------------------|--------------------|------|--------------------|---------|---|
| $f_{PLL\_in}$         | PLL input clock                   | 4                  | -    | 24                 | MHz     |   |
| $f_{PLL\_OUT}$        | PLL multiplier output clock       | 50                 | -    | 480                | MHz     |   |
| $f_{PLL\_REF}$        | PLL reference clock               | 4                  | -    | 8                  | MHz     |   |
| $f_{PLL\_VCO}$        | PLL voltage controlled oscillator | 200                | -    | 480                | MHz     |   |
| $T_L$                 | PLL locking time                  | -                  | -    | 100                | $\mu$ s |   |
| Jitter <sup>[2]</sup> | Cycle-to-cycle Jitter             | -                  | -    | 500                | ps      |   |
| $I_{DD}$              | Power consumption                 | -                  | 3.56 | 4.4                | mA      | $V_{DD}=3.3V @ f_{PLL\_VCO} = 500$<br>MHz |

**Note:**

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production

Table 9.4-10 PLL Characteristics

9.4.9 I/O AC Characteristics

| Symbol          | Parameter  | Typ. | Max <sup>[1]</sup> | Unit | Test Conditions <sup>[2]</sup>                 |  |
|-----------------|--|------|--------------------|------|--|--|
| $t_{f(I/O)out}$ | Output high (90%) to low level (10%) fall time<br>(Normal Slew Rate) | -    | 3.5                | ns   | $C_L = 30\text{ pF}, V_{DD} \geq 3.6\text{ V}$ |  |
|                 |  | -    | 2                  |      | $C_L = 10\text{ pF}, V_{DD} \geq 3.6\text{ V}$ |  |
|                 |  | -    | 4.5                |      | $C_L = 30\text{ pF}, V_{DD} \geq 2.7\text{ V}$ |  |
|                 |  | -    | 3                  |      | $C_L = 10\text{ pF}, V_{DD} \geq 2.7\text{ V}$ |  |
|                 |  | -    | 8                  |      | $C_L = 30\text{ pF}, V_{DD} \geq 1.8\text{ V}$ |  |
|                 |  | -    | 5.5                |      | $C_L = 10\text{ pF}, V_{DD} \geq 1.8\text{ V}$ |  |
|                 | Output high (90%) to low level (10%) fall time<br>(High Slew Rate)   | -    | 3                  |      | $C_L = 30\text{ pF}, V_{DD} \geq 3.6\text{ V}$ |  |
|                 |  | -    | 1.5                |      | $C_L = 10\text{ pF}, V_{DD} \geq 3.6\text{ V}$ |  |
|                 |  | -    | 3.5                |      | $C_L = 30\text{ pF}, V_{DD} \geq 2.7\text{ V}$ |  |
|                 |  | -    | 2                  |      | $C_L = 10\text{ pF}, V_{DD} \geq 2.7\text{ V}$ |  |
|                 |  | -    | 6.5                |      | $C_L = 30\text{ pF}, V_{DD} \geq 1.8\text{ V}$ |  |
|                 |  | -    | 3.5                |      | $C_L = 10\text{ pF}, V_{DD} \geq 1.8\text{ V}$ |  |
|                 | Output high (90%) to low level (10%) fall time<br>(Fast Slew Rate)   | -    | 2.5                |      | $C_L = 30\text{ pF}, V_{DD} \geq 3.6\text{ V}$ |  |
|                 |  | -    | 1.5                |      | $C_L = 10\text{ pF}, V_{DD} \geq 3.6\text{ V}$ |  |
|                 |  | -    | 3                  |      | $C_L = 30\text{ pF}, V_{DD} \geq 2.7\text{ V}$ |  |
|                 |  | -    | 2                  |      | $C_L = 10\text{ pF}, V_{DD} \geq 2.7\text{ V}$ |  |
|                 |  | -    | 5.5                |      | $C_L = 30\text{ pF}, V_{DD} \geq 1.8\text{ V}$ |  |
|                 |  | -    | 3.5                |      | $C_L = 10\text{ pF}, V_{DD} \geq 1.8\text{ V}$ |  |
| $t_{r(I/O)out}$ | Output low (10%) to high level (90%) rise time<br>(Normal Slew Rate) | -    | 4                  | ns   | $C_L = 30\text{ pF}, V_{DD} \geq 3.6\text{ V}$ |  |
|                 |  | -    | 2.5                |      | $C_L = 10\text{ pF}, V_{DD} \geq 3.6\text{ V}$ |  |
|                 |  | -    | 4.5                |      | $C_L = 30\text{ pF}, V_{DD} \geq 2.7\text{ V}$ |  |
|                 |  | -    | 3                  |      | $C_L = 10\text{ pF}, V_{DD} \geq 2.7\text{ V}$ |  |
|                 |  | -    | 8                  |      | $C_L = 30\text{ pF}, V_{DD} \geq 1.8\text{ V}$ |  |
|                 |  | -    | 5.5                |      | $C_L = 10\text{ pF}, V_{DD} \geq 1.8\text{ V}$ |  |
|                 | Output low (10%) to high level (90%) rise time<br>(High Slew Rate)   | -    | 2.5                |      | ns   | $C_L = 30\text{ pF}, V_{DD} \geq 3.6\text{ V}$ |
|                 |  | -    | 1.5                |      |  | $C_L = 10\text{ pF}, V_{DD} \geq 3.6\text{ V}$ |
|                 |  | -    | 3                  |      |  | $C_L = 30\text{ pF}, V_{DD} \geq 2.7\text{ V}$ |
|                 |  | -    | 2                  |      |  | $C_L = 10\text{ pF}, V_{DD} \geq 2.7\text{ V}$ |
|                 |  | -    | 5                  |      |  | $C_L = 30\text{ pF}, V_{DD} \geq 1.8\text{ V}$ |
|                 |  | -    | 3                  |      |  | $C_L = 10\text{ pF}, V_{DD} \geq 1.8\text{ V}$ |

| Symbol                                  | Parameter   | Typ. | Max <sup>[1]</sup> | Unit | Test Conditions <sup>[2]</sup>  |
|---|---|------|--------------------|------|---|
|   | Output low (10%) to high level (90%) rise time (Fast Slew Rate) | -    | 2.5                | ns   | C <sub>L</sub> = 30 pF, V <sub>DD</sub> >= 3.6 V                                |
|   |   | -    | 1.5                |      | C <sub>L</sub> = 10 pF, V <sub>DD</sub> >= 3.6 V                                |
|   |   | -    | 3                  |      | C <sub>L</sub> = 30 pF, V <sub>DD</sub> >= 2.7 V                                |
|   |   | -    | 2                  |      | C <sub>L</sub> = 10 pF, V <sub>DD</sub> >= 2.7 V                                |
|   |   | -    | 5                  |      | C <sub>L</sub> = 30 pF, V <sub>DD</sub> >= 1.8 V                                |
|   |   | -    | 3                  |      | C <sub>L</sub> = 10 pF, V <sub>DD</sub> >= 1.8 V                                |
| f <sub>max(I/O)out</sub> <sup>[3]</sup> | I/O maximum frequency (Normal Slew Rate)                        | -    | 88.9               | MHz  | C <sub>L</sub> = 30 pF, V <sub>DD</sub> >= 3.6 V                                |
|   |   | -    | 148.1              |      | C <sub>L</sub> = 10 pF, V <sub>DD</sub> >= 3.6 V                                |
|   |   | -    | 74.1               |      | C <sub>L</sub> = 30 pF, V <sub>DD</sub> >= 2.7 V                                |
|   |   | -    | 111.1              |      | C <sub>L</sub> = 10 pF, V <sub>DD</sub> >= 2.7 V                                |
|   |   | -    | 41.7               |      | C <sub>L</sub> = 30 pF, V <sub>DD</sub> >= 1.8 V                                |
|   |   | -    | 60.6               |      | C <sub>L</sub> = 10 pF, V <sub>DD</sub> >= 1.8 V                                |
|   | I/O maximum frequency (High Slew Rate)                          | -    | 121.2              | MHz  | C <sub>L</sub> = 30 pF, V <sub>DD</sub> >= 3.6 V                                |
|   |   | -    | 222.2              |      | C <sub>L</sub> = 10 pF, V <sub>DD</sub> >= 3.6 V                                |
|   |   | -    | 102.6              |      | C <sub>L</sub> = 30 pF, V <sub>DD</sub> >= 2.7 V                                |
|   |   | -    | 166.7              |      | C <sub>L</sub> = 10 pF, V <sub>DD</sub> >= 2.7 V                                |
|   |   | -    | 58.0               |      | C <sub>L</sub> = 30 pF, V <sub>DD</sub> >= 1.8 V                                |
|   |   | -    | 102.6              |      | C <sub>L</sub> = 10 pF, V <sub>DD</sub> >= 1.8 V                                |
|   | I/O maximum frequency (Fastigh Slew Rate)                       | -    | 133.3              | MHz  | C <sub>L</sub> = 30 pF, V <sub>DD</sub> >= 3.6 V                                |
|   |   | -    | 222.2              |      | C <sub>L</sub> = 10 pF, V <sub>DD</sub> >= 3.6 V                                |
|   |   | -    | 111.1              |      | C <sub>L</sub> = 30 pF, V <sub>DD</sub> >= 2.7 V                                |
|   |   | -    | 166.7              |      | C <sub>L</sub> = 10 pF, V <sub>DD</sub> >= 2.7 V                                |
|   |   | -    | 63.5               |      | C <sub>L</sub> = 30 pF, V <sub>DD</sub> >= 1.8 V                                |
|   |   | -    | 102.6              |      | C <sub>L</sub> = 10 pF, V <sub>DD</sub> >= 1.8 V                                |
| I <sub>DIO</sub> <sup>[4]</sup>         | I/O dynamic current consumption                                 | 2.77 | -                  | mA   | C <sub>L</sub> = 30 pF, V <sub>DD</sub> = 3.3 V, f <sub>(I/O)out</sub> = 24 MHz |
|   |   | 1.19 | -                  |      | C <sub>L</sub> = 10 pF, V <sub>DD</sub> = 3.3 V, f <sub>(I/O)out</sub> = 24 MHz |
|   |   | 0.69 | -                  |      | C <sub>L</sub> = 30 pF, V <sub>DD</sub> = 3.3 V, f <sub>(I/O)out</sub> = 6 MHz  |
|   |   | 0.3  | -                  |      | C <sub>L</sub> = 10 pF, V <sub>DD</sub> = 3.3 V, f <sub>(I/O)out</sub> = 6 MHz  |

| Symbol   | Parameter | Typ. | Max <sup>[1]</sup> | Unit | Test Conditions <sup>[2]</sup> |
|--|-----------|------|--------------------|------|--------------------------------|
| <p><b>Note:</b></p> <ol style="list-style-type: none"> <li>1. Guaranteed by characterization result, not tested in production.</li> <li>2. C<sub>L</sub> is a external capacitive load to simulate PCB and device loading.</li> <li>3. The maximum frequency is defined by <math>f_{max} = \frac{2}{3 \times (t_f + t_r)}</math>.</li> <li>4. The I/O dynamic current consumption is defined by <math>I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)</math></li> </ol> |           |      |                    |      |                                |

Table 9.4-11 I/O AC Characteristics

## 9.5 Analog Characteristics

### 9.5.1 LDO

| Symbol           | Parameter      | Min | Typ  | Max | Unit | Test Condition |
|------------------|----------------|-----|------|-----|------|----------------|
| V <sub>DD</sub>  | Power supply   | 1.8 | -    | 3.6 | V    |                |
| V <sub>LDO</sub> | Output voltage | -   | 1.26 | -   | V    |                |
| T <sub>A</sub>   | Temperature    | -40 | -    | 105 | °C   |                |

**Note:**

1. It is recommended a 0.1μF bypass capacitor is connected between V<sub>DD</sub> and the closest V<sub>SS</sub> pin of the device.
2. For ensuring power stability, a 1μF capacitor must be connected between LDO\_CAP pin and the closest V<sub>SS</sub> pin of the device.

9.5.2 Reset and Power Control Block Characteristics

The parameters in Table 9.5-1 are derived from tests performed under ambient temperature.

| Symbol              | Parameter                                   | Min  | Typ  | Max   | Unit           | Test Conditions                   |
|---------------------|---|------|------|-------|----------------|-----------------------------------|
| $I_{POR}^{[1]}$     | POR operating current                       | -    | 35   | 45    | $\mu A$        | $AV_{DD} = 3.6V$                  |
| $I_{LVR}^{[1]}$     | LVR operating current                       | -    | 0.3  | 0.6   |                | $AV_{DD} = 3.6V$ , Normal mode    |
| $I_{BOD}^{[1]}$     | BOD operating current                       | -    | 30   | 40    |                | $AV_{DD} = 3.6V$ , Normal mode    |
|                     |   | -    | 1    | -     |                | $AV_{DD} = 3.6V$ , Low Power mode |
| $V_{POR}$           | POR reset voltage                           | 1.38 | 1.46 | 1.54  | V              | -                                 |
| $V_{LVR}$           | LVR reset voltage                           | 1.45 | 1.50 | 1.55  |                | -                                 |
| $V_{BOD}$           | BOD brown-out detect voltage (Falling edge) | 1.50 | 1.60 | 1.70  |                | BODVL = 0                         |
|                     |   | 1.70 | 1.80 | 1.90  |                | BODVL = 1                         |
|                     |   | 1.90 | 2.00 | 2.10  |                | BODVL = 2                         |
|                     |   | 2.10 | 2.20 | 2.30  |                | BODVL = 3                         |
|                     |   | 2.30 | 2.40 | 2.50  |                | BODVL = 4                         |
|                     |   | 2.50 | 2.60 | 2.70  |                | BODVL = 5                         |
|                     |   | 2.70 | 2.80 | 2.90  |                | BODVL = 6                         |
|                     |   | 2.90 | 3.00 | 3.10  |                | BODVL = 7                         |
|                     | BOD brown-out detect voltage (Rising edge)  | 1.58 | 1.68 | 1.78  |                | BODVL = 0                         |
|                     |   | 1.78 | 1.88 | 1.98  |                | BODVL = 1                         |
|                     |   | 1.98 | 2.08 | 2.18  |                | BODVL = 2                         |
|                     |   | 2.18 | 2.28 | 2.38  |                | BODVL = 3                         |
|                     |   | 2.38 | 2.48 | 2.58  |                | BODVL = 4                         |
|                     |   | 2.58 | 2.68 | 2.78  |                | BODVL = 5                         |
|                     |   | 2.78 | 2.88 | 2.98  |                | BODVL = 6                         |
|                     |   | 2.98 | 3.08 | 3.18  |                | BODVL = 7                         |
| $T_{LVR\_SU}^{[1]}$ | LVR startup time                            | -    | 200  | 256   | $\mu s$        | -                                 |
| $T_{LVR\_RE}^{[1]}$ | LVR respond time                            | -    | 1    | 2     |                | Normal mode                       |
| $T_{BOD\_SU}^{[1]}$ | BOD startup time                            | -    | 1000 | -     |                | -                                 |
| $T_{BOD\_RE}^{[1]}$ | BOD respond time                            | -    | -    | 100   |                | Normal mode                       |
|                     |   | -    | -    | 12000 | Low Power mode |                                   |
| $R_{VDDR}^{[1]}$    | $V_{DD}$ rise time rate                     | 10   | -    | -     | $\mu s/V$      | POR Enabled                       |
| $R_{VDDF}^{[1]}$    | $V_{DD}$ fall time rate                     | 10   | -    | -     |                | POR Enabled                       |
|                     |   | 300  | -    | -     |                | LVR Enabled                       |
|                     |   | 666  | -    | -     |                | BOD 1.6V Enabled, Normal mode     |



| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions               |
|--------|-----------|-----|-----|-----|------|-------------------------------|
|        |           | 285 | -   | -   |      | BOD 1.8V Enabled, Normal mode |
|        |           | 180 | -   | -   |      | BOD 2.0V Enabled, Normal mode |
|        |           | 133 | -   | -   |      | BOD 2.2V Enabled, Normal mode |
|        |           | 105 | -   | -   |      | BOD 2.4V Enabled, Normal mode |
|        |           | 85  | -   | -   |      | BOD 2.6V Enabled, Normal mode |
|        |           | 75  | -   | -   |      | BOD 2.8V Enabled, Normal mode |
|        |           | 65  |     |     |      | BOD 3.0V Enabled, Normal mode |

**Note:**

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 9.5-1 Reset and Power Control Unit

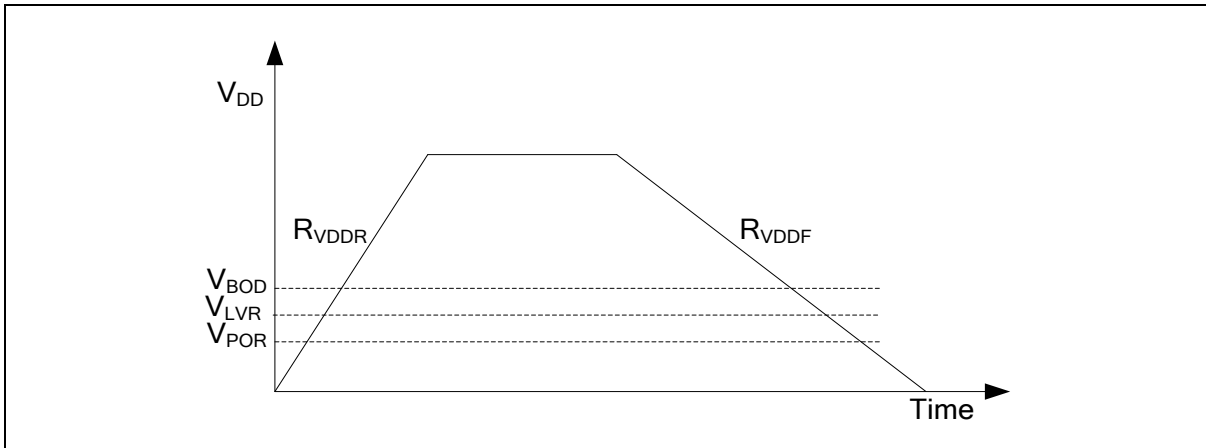


Figure 9-4 Power Ramp Up/Down Condition

9.5.3 12-bit SAR ADC

9.5.3.1 ADC0 Characteristics

***Fast Speed Channel***

| Symbol                | Parameter   | Min   | Typ | Max              | Unit               | Test Conditions   |
|-----------------------|---|-------|-----|------------------|--------------------|---|
| T <sub>A</sub>        | Temperature   | -40   | -   | 105              | °C                 |   |
| AV <sub>DD</sub>      | Analog operating voltage  | 1.8   | -   | 3.6              | V                  | AV <sub>DD</sub> = V <sub>DD</sub>  |
| V <sub>REF</sub>      | Reference voltage   | 1.6   | -   | AV <sub>DD</sub> | V                  |   |
| V <sub>IN</sub>       | ADC channel input voltage   | 0     | -   | V <sub>REF</sub> | V                  |   |
| I <sub>ADC</sub> [*1] | Operating current (AV <sub>DD</sub> current)<br>(Enable ADC and disable all other analog modules) | 599   | -   | 629              | µA                 | AV <sub>DD</sub> = V <sub>DD</sub> = V <sub>REF</sub> = 3.3V<br>ADC Clock Rate = 80 MHz<br>High speed channel |
| N <sub>R</sub>        | Resolution  | 12    |     |                  | Bit                |   |
| F <sub>ADC</sub>      | ADC Clock frequency   | TBD   | -   | 80               | MHz                | F <sub>ADC</sub> = 1/T <sub>ADC</sub>   |
| T <sub>SMP</sub>      | Sampling Time   |       | 2   |                  | 1/F <sub>ADC</sub> |   |
| T <sub>CONV</sub>     | Conversion time   |       | 14  |                  | 1/F <sub>ADC</sub> | T <sub>CONV</sub> = T <sub>SMP</sub> + 12   |
| F <sub>SPS</sub>      | Sampling Rate   | TBD   | -   | 5                | MSPS               | High speed channel  |
| T <sub>EN</sub>       | Enable to ready time  | TBD   | -   | -                | µs                 |   |
| INL                   | Integral Non-Linearity Error  | -4.42 | -   | 2.4              | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 3.3V<br>package with V <sub>REF</sub> pin                               |
| DNL                   | Differential Non-Linearity Error  | -1    | -   | 4.62             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 3.3V<br>package with V <sub>REF</sub> pin                               |
| E <sub>G</sub>        | Gain error  | 0.5   | -   | 2.06             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 3.3V<br>package with V <sub>REF</sub> pin                               |
| E <sub>O</sub>        | Offset error  | 0     | -   | 1.81             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 3.3V<br>package with V <sub>REF</sub> pin                               |
| E <sub>A</sub>        | Absolute Error  | 3.69  | -   | 6.37             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 3.3V<br>package with V <sub>REF</sub> pin                               |
| C <sub>IN</sub> [*1]  | Internal Capacitance  | -     | 5   | -                | pF                 |   |

**Note:**

1. Guaranteed by characterization result, not tested in production.
2. R<sub>EX</sub> max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resolution) and k is the number of sampling clocks (T<sub>SMP</sub>). C<sub>EX</sub> represents the capacitance of PCB and pad and is combined with R<sub>EX</sub> into a low-pass filter. Once the R<sub>EX</sub> and C<sub>EX</sub> values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$$

**Low Speed Channel**

| Symbol                           | Parameter   | Min   | Typ | Max              | Unit               | Test Conditions   |
|----------------------------------|---|-------|-----|------------------|--------------------|---|
| T <sub>A</sub>                   | Temperature   | -40   | -   | 105              | °C                 |   |
| AV <sub>DD</sub>                 | Analog operating voltage  | 1.8   | -   | 3.6              | V                  | AV <sub>DD</sub> = V <sub>DD</sub>  |
| V <sub>REF</sub>                 | Reference voltage   | 1.6   | -   | AV <sub>DD</sub> | V                  |   |
| V <sub>IN</sub>                  | ADC channel input voltage   | 0     | -   | V <sub>REF</sub> | V                  |   |
| I <sub>ADC</sub> <sup>[*1]</sup> | Operating current (AV <sub>DD</sub> current)<br>(Enable ADC and disable all other analog modules) | 163   | -   | 270              | µA                 | AV <sub>DD</sub> = V <sub>DD</sub> = V <sub>REF</sub> = 1.62V ~ 3.3V<br>ADC Clock Rate = 32 MHz<br>High speed channel |
| N <sub>R</sub>                   | Resolution  | 12    |     |                  | Bit                |   |
| F <sub>ADC</sub>                 | ADC Clock frequency   | TBD   | -   | 80               | MHz                | F <sub>ADC</sub> = 1/T <sub>ADC</sub>   |
| T <sub>SMP</sub>                 | Sampling Time   |       | 2   |                  | 1/F <sub>ADC</sub> |   |
| T <sub>CONV</sub>                | Conversion time   |       | 14  |                  | 1/F <sub>ADC</sub> | T <sub>CONV</sub> = T <sub>SMP</sub> + 12   |
| F <sub>SPS</sub>                 | Sampling Rate   | 0.1   | -   | 2                | MSPS               | Low speed channel<br><b>Note:</b> it needs more extend sampling time to slow down the sampling rate.                  |
| T <sub>EN</sub>                  | Enable to ready time  | TBD   | -   | -                | µs                 |   |
| INL                              | Integral Non-Linearity Error  | -2.17 | -   | 1.89             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 1.62V ~ 3.3V<br>package with V <sub>REF</sub> pin                               |
| DNL                              | Differential Non-Linearity Error  | -1    | -   | 1.87             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 1.62V ~ 3.3V<br>package with V <sub>REF</sub> pin                               |
| E <sub>G</sub>                   | Gain error  | 0.31  | -   | 2.56             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 1.62V ~ 3.3V<br>package with V <sub>REF</sub> pin                               |
| E <sub>O</sub>                   | Offset error  | -0.31 | -   | 2.19             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 1.62V ~ 3.3V<br>package with V <sub>REF</sub> pin                               |
| E <sub>A</sub>                   | Absolute Error  | -3.5  | -   | 5.87             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 1.62V ~ 3.3V<br>package with V <sub>REF</sub> pin                               |
| C <sub>IN</sub> <sup>[*1]</sup>  | Internal Capacitance  | -     | 5   | -                | pF                 |   |

**Note:**

- Guaranteed by characterization result, not tested in production.
- R<sub>EX</sub> max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resolution) and k is the number of sampling clocks (T<sub>SMP</sub>). C<sub>EX</sub> represents the capacitance of PCB and pad and is combined with R<sub>EX</sub> into a low-pass filter. Once the R<sub>EX</sub> and C<sub>EX</sub> values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$$

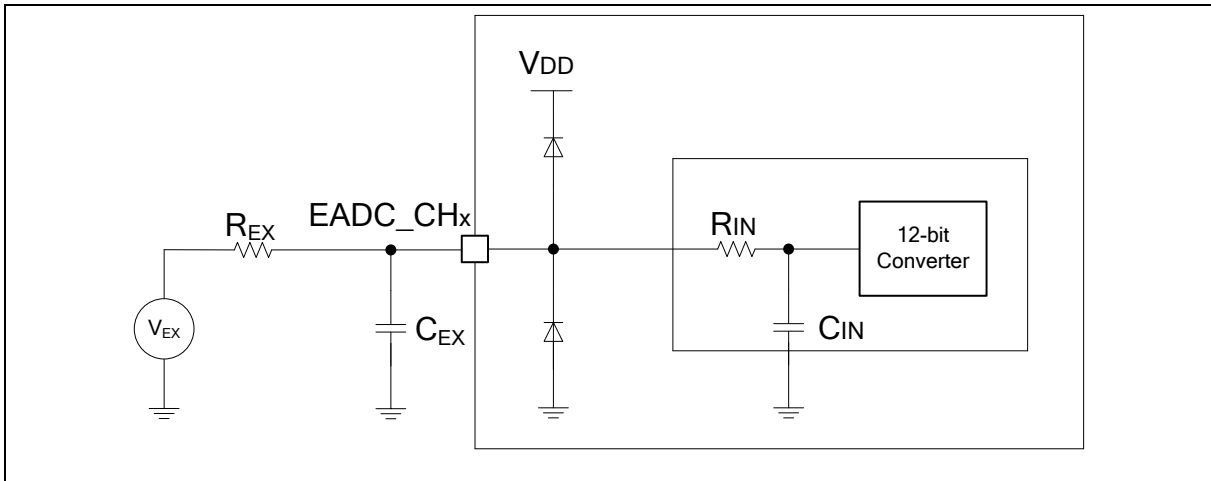
9.5.3.2 ADC1 Characteristics

**Fast Speed Channel**

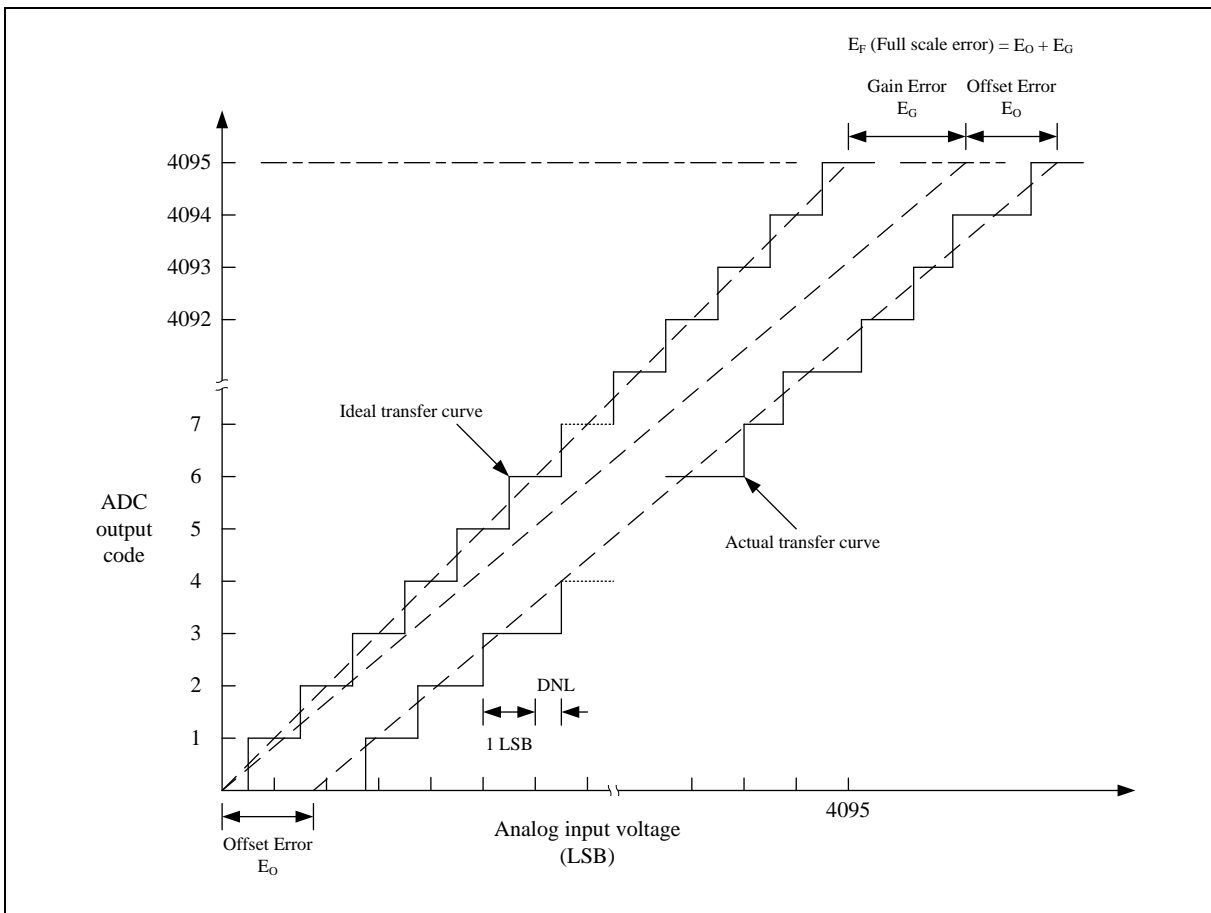
| Symbol  | Parameter   | Min   | Typ | Max              | Unit               | Test Conditions   |
|---|---|-------|-----|------------------|--------------------|---|
| T <sub>A</sub>  | Temperature   | -40   | -   | 105              | °C                 |   |
| AV <sub>DD</sub>  | Analog operating voltage  | 1.8   | -   | 3.6              | V                  | AV <sub>DD</sub> = V <sub>DD</sub>  |
| V <sub>REF</sub>  | Reference voltage   | 1.6   | -   | AV <sub>DD</sub> | V                  |   |
| V <sub>IN</sub>   | ADC channel input voltage   | 0     | -   | V <sub>REF</sub> | V                  |   |
| I <sub>ADC</sub> [*1]   | Operating current (AV <sub>DD</sub> current)<br>(Enable ADC and disable all other analog modules) | 596   | -   | 627              | μA                 | AV <sub>DD</sub> = V <sub>DD</sub> = V <sub>REF</sub> = 3.3V<br>ADC Clock Rate = 80 MHz<br>High speed channel |
| N <sub>R</sub>  | Resolution  | 12    |     |                  | Bit                |   |
| F <sub>ADC</sub>  | ADC Clock frequency   | TBD   | -   | 80               | MHz                | F <sub>ADC</sub> = 1/T <sub>ADC</sub>   |
| T <sub>SMP</sub>  | Sampling Time   |       | 2   |                  | 1/F <sub>ADC</sub> |   |
| T <sub>CONV</sub>   | Conversion time   |       | 14  |                  | 1/F <sub>ADC</sub> | T <sub>CONV</sub> = T <sub>SMP</sub> + 12   |
| F <sub>SPS</sub>  | Sampling Rate   | TBD   | -   | 5                | MSPS               | High speed channel  |
| T <sub>EN</sub>   | Enable to ready time  | TBD   | -   | -                | μs                 |   |
| INL   | Integral Non-Linearity Error  | -6.22 | -   | 2.17             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 3.3V<br>package with V <sub>REF</sub> pin                               |
| DNL   | Differential Non-Linearity Error  | -1    | -   | 6.62             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 3.3V<br>package with V <sub>REF</sub> pin                               |
| E <sub>G</sub>  | Gain error  | 1.06  | -   | 2.94             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 3.3V<br>package with V <sub>REF</sub> pin                               |
| E <sub>O</sub>  | Offset error  | 0     | -   | 1.75             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 3.3V<br>package with V <sub>REF</sub> pin                               |
| E <sub>A</sub>  | Absolute Error  | 3     | -   | 5.69             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 3.3V<br>package with V <sub>REF</sub> pin                               |
| C <sub>IN</sub> [*1]  | Internal Capacitance  | -     | 5   | -                | pF                 |   |
| <b>Note:</b>  |   |       |     |                  |                    |   |
| <ol style="list-style-type: none"> <li>Guaranteed by characterization result, not tested in production.</li> <li>R<sub>EX</sub> max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resolution) and k is the number of sampling clocks (T<sub>SMP</sub>). C<sub>EX</sub> represents the capacitance of PCB and pad and is combined with R<sub>EX</sub> into a low-pass filter. Once the R<sub>EX</sub> and C<sub>EX</sub> values are too large, it is possible to filter the real signal and reduce the ADC accuracy.</li> </ol> |   |       |     |                  |                    |   |
| $R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$   |   |       |     |                  |                    |   |

**Low Speed Channel**

| Symbol  | Parameter   | Min   | Typ | Max              | Unit               | Test Conditions   |
|---|---|-------|-----|------------------|--------------------|---|
| T <sub>A</sub>  | Temperature   | -40   | -   | 105              | °C                 |   |
| AV <sub>DD</sub>  | Analog operating voltage  | 1.8   | -   | 3.6              | V                  | AV <sub>DD</sub> = V <sub>DD</sub>  |
| V <sub>REF</sub>  | Reference voltage   | 1.6   | -   | AV <sub>DD</sub> | V                  |   |
| V <sub>IN</sub>   | ADC channel input voltage   | 0     | -   | V <sub>REF</sub> | V                  |   |
| I <sub>ADC</sub> <sup>[*1]</sup>  | Operating current (AV <sub>DD</sub> current)<br>(Enable ADC and disable all other analog modules) | 162   | -   | 269              | µA                 | AV <sub>DD</sub> = V <sub>DD</sub> = V <sub>REF</sub> = 1.62V ~ 3.3V<br>ADC Clock Rate = 32 MHz<br>High speed channel |
| N <sub>R</sub>  | Resolution  | 12    |     |                  | Bit                |   |
| F <sub>ADC</sub>  | ADC Clock frequency   | 1.5   | -   | 32               | MHz                | F <sub>ADC</sub> = 1/T <sub>ADC</sub>   |
| T <sub>SMP</sub>  | Sampling Time   |       | 2   |                  | 1/F <sub>ADC</sub> |   |
| T <sub>CONV</sub>   | Conversion time   |       | 14  |                  | 1/F <sub>ADC</sub> | T <sub>CONV</sub> = T <sub>SMP</sub> + 12   |
| F <sub>SPS</sub>  | Sampling Rate   | 0.1   | -   | 2                | MSPS               | Low speed channel   |
| T <sub>EN</sub>   | Enable to ready time  | TBD   | -   | -                | µs                 |   |
| INL   | Integral Non-Linearity Error  | -1.96 | -   | 1.22             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 1.62V ~ 3.3V<br>package with V <sub>REF</sub> pin                               |
| DNL   | Differential Non-Linearity Error  | -1    | -   | 1.94             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 1.62V ~ 3.3V<br>package with V <sub>REF</sub> pin                               |
| E <sub>G</sub>  | Gain error  | 0.62  | -   | 3.19             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 1.62V ~ 3.3V<br>package with V <sub>REF</sub> pin                               |
| E <sub>O</sub>  | Offset error  | -0.44 | -   | 2.62             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 1.62V ~ 3.3V<br>package with V <sub>REF</sub> pin                               |
| E <sub>A</sub>  | Absolute Error  | 2.81  | -   | 6.19             | LSB                | V <sub>REF</sub> = AV <sub>DD</sub> = 1.62V ~ 3.3V<br>package with V <sub>REF</sub> pin                               |
| C <sub>IN</sub> <sup>[*1]</sup>   | Internal Capacitance  | -     | 5   | -                | pF                 |   |
| <b>Note:</b>  |   |       |     |                  |                    |   |
| <ol style="list-style-type: none"> <li>Guaranteed by characterization result, not tested in production.</li> <li>R<sub>EX</sub> max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resolution) and k is the number of sampling clocks (T<sub>SMP</sub>). C<sub>EX</sub> represents the capacitance of PCB and pad and is combined with R<sub>EX</sub> into a low-pass filter. Once the R<sub>EX</sub> and C<sub>EX</sub> values are too large, it is possible to filter the real signal and reduce the ADC accuracy.</li> </ol> |   |       |     |                  |                    |   |
| $R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$   |   |       |     |                  |                    |   |



**Note:** Injection current is an important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



**Note:** The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

9.5.4 Temperature Sensor

| Symbol  | Parameter  | Min   | Typ   | Max   | Unit  |
|---|--|-------|-------|-------|-------|
| V <sub>DD</sub>   | Operating Voltage  | 1.8   |       | 3.6   | V     |
| T <sub>A</sub>  | Temperature Range  | -40   |       | 105   | °C    |
| I <sub>TEMP</sub>   | Current Consumption [*3]   |       | 16    |       | μA    |
| T <sub>c</sub>  | Temperature Coefficient [*3]                                       | -1.77 | -1.82 | -1.84 | mV/°C |
| V <sub>os</sub>   | Offset Voltage when T <sub>A</sub> = 0°C [*3]                      | 710.2 |       | 716.8 | mV    |
| t <sub>S</sub>  | Stable time[*2]  |       | 1     |       | μs    |
| T <sub>S_temp</sub>   | ADC sampling time when reading the temperature (5pF cap load) [*1] |       | 3     |       | μs    |
| <p><b>Note:</b></p> <ol style="list-style-type: none"> <li>1. <math>V_{TEMP} (mV) = T_c (mV/°C) \times \text{Temperature } (°C) + V_{os} (mV)</math></li> <li>2. Guaranteed by design, not tested in production</li> <li>3. Guaranteed by characteristic, not tested in production</li> </ol> |  |       |       |       |       |

9.5.5 Analog Comparator Controller (ACMP)

The maximum values are obtained for  $V_{DD} = 3.6\text{ V}$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25\text{ }^\circ\text{C}$  and  $V_{DD} = 3.3\text{ V}$  unless otherwise specified.

| Symbol  | Parameter                              | Min | Typ                   | Max             | Unit             | Test Conditions                        |
|---|--|-----|-----------------------|-----------------|------------------|--|
| $AV_{DD}$   | Analog supply voltage                  | 1.8 | -                     | 3.6             | V                | $V_{DD} = AV_{DD}$                     |
| $T_A$   | Temperature                            | -40 | -                     | 105             | $^\circ\text{C}$ |  |
| $I_{ACMP}^{[2]}$  | ACMP operating current                 | -   | 75                    | 90              | $\mu\text{A}$    | MODESEL = 11                           |
|   |  | -   | 10                    | 30              |                  | MODESEL = 10                           |
|   |  | -   | 3                     | 10              |                  | MODESEL = 01                           |
|   |  | -   | 1.2                   | 6               |                  | MODESEL = 00                           |
| $V_{CM}^{[2]}$  | Input common mode voltage range        | 0.1 | $\frac{1}{2} AV_{DD}$ | $AV_{DD} - 0.1$ |                  |  |
| $V_{DI}^{[2]}$  | Differential input voltage sensitivity | -   | 10                    | -               | mV               | Hysteresis disable (HYSSEL = 00)       |
| $V_{offset}^{[2]}$  | Input offset voltage                   | -   | 5                     | 10              | mV               | Hysteresis disable (HYSSEL = 00)       |
| $V_{hys}^{[2]}$   | Hysteresis window                      | -   | 10                    | 20              | mV               | HYSSEL = 01                            |
|   |  |     | 20                    | 40              |                  | HYSSEL = 10                            |
|   |  |     | 30                    | 60              |                  | HYSSEL = 11                            |
| $A_V^{[1]}$   | DC voltage Gain                        | 43  | 70                    | -               | dB               |  |
| $T_d^{[2]}$   | Propagation delay                      | -   | 180                   | 250             | ns               | MODESEL = 11                           |
|   |  | -   | 350                   | 600             |                  | MODESEL = 10                           |
|   |  | -   | 750                   | 2000            |                  | MODESEL = 01                           |
|   |  | -   | 1600                  | 4500            |                  | MODESEL = 00                           |
| $T_{Setup}^{[2]}$   | Setup time                             | -   | $250 + T_d$           | $450 + T_d$     | ns               |  |
| $A_{CRV}^{[2]}$   | CRV output voltage                     | -5  | -                     | 5               | %                | $AV_{DD} \times (1/6 + CRVCTL/24)$     |
| $R_{CRV}^{[2]}$   | Unit resistor value                    | -   | 4.2                   | -               | k $\Omega$       |  |
| $T_{SETUP\_CRV}^{[2]}$  | Setup time                             | -   | -                     | TBD             | $\mu\text{s}$    | CRV output voltage settle to $\pm 5\%$ |
| $I_{DD\_CRV}^{[2]}$   | Operating current                      | -   | 32.7                  | -               | $\mu\text{A}$    |  |
| <b>Note:</b> <ol style="list-style-type: none"> <li>1. Guaranteed by design, not tested in production</li> <li>2. Guaranteed by characteristic, not tested in production</li> </ol> |  |     |                       |                 |                  |  |

Table 9.5-2 ACMP Characteristics



9.5.6 Digital to Analog Converter (DAC)

The maximum values are obtained for  $V_{DD} = 3.6\text{ V}$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25\text{ }^\circ\text{C}$  and  $V_{DD} = 3.3\text{ V}$  unless otherwise specified.

| Symbol              | Parameter                        | Min               | Typ | Max               | Unit       | Test Condition                   |
|---------------------|----------------------------------|-------------------|-----|-------------------|------------|----------------------------------|
| $V_{DD}$            | Analog supply voltage            | 1.8               | -   | 3.6               | V          | -                                |
| $N_R$               | Resolution                       | 12                |     |                   | bit        | -                                |
| $V_{REF}$           | Reference supply voltage         | 1.5               | -   | $V_{DD}$          | V          | $V_{REF} \leq V_{DD}$            |
| $DNL^{[2]}$         | Differential non-linearity error | -                 | -   | $\pm 2$           | LSB        | 12-bit mode                      |
|                     |                                  | -                 | -   | $\pm 0.5$         | LSB        | 8-bit mode                       |
| $INL^{[2]}$         | Integral non-linearity error     | -                 | -   | $\pm 4$           | LSB        | 12-bit mode                      |
|                     |                                  | -                 | -   | $\pm 1$           | LSB        | 8-bit mode                       |
| $OE^{[2]}$          | Offset Error                     | -                 | -   | $\pm 30$          | LSB        | 12-bit mode<br>DACOUT buffer ON  |
|                     |                                  | -                 | -   | $\pm 4$           | LSB        | 12-bit mode<br>DACOUT buffer OFF |
|                     |                                  | -                 | -   | $\pm 2$           | LSB        | 8-bit mode                       |
| $GE^{[2]}$          | Gain Error                       | -                 | -   | $\pm 8$           | LSB        | 12-bit mode<br>DACOUT buffer ON  |
|                     |                                  | -                 | -   | $\pm 4$           | LSB        | 12-bit mode<br>DACOUT buffer OFF |
|                     |                                  | -                 | -   | $\pm 2$           | LSB        | 8-bit mode                       |
| $AE^{[2]}$          | Absolute Error                   | -                 | -   | $\pm 10$          | LSB        | 12-bit mode<br>DACOUT buffer ON  |
|                     |                                  | -                 | -   | $\pm 4$           | LSB        | 12-bit mode<br>DACOUT buffer OFF |
|                     |                                  | -                 | -   | $\pm 2$           | LSB        | 8-bit mode                       |
| -                   | Monotonic                        | 10-bit guaranteed |     |                   | -          | -                                |
| $V_O^{[1]}$         | Output Voltage                   | 0.2               |     | $V_{DD} - 0.2$    | V          | DACOUT buffer ON                 |
|                     |                                  | 1*LSB             |     | $V_{REF} - 1*LSB$ |            | DACOUT buffer OFF                |
| $R_{LOAD}^{[2][3]}$ | Resistive load                   | 7.5               | -   | -                 | k $\Omega$ | DACOUT buffer ON                 |
| $R_O^{[2]}$         | Output impedance                 | -                 | 10  | 12                | k $\Omega$ | DACOUT buffer OFF                |
| $C_{LOAD}^{[2][4]}$ | Capacitive load                  | -                 | -   | 50                | pF         | DACOUT buffer ON                 |
|                     |                                  | -                 | -   | 20                | pF         | DACOUT buffer OFF                |

| Symbol   | Parameter  | Min | Typ | Max | Unit | Test Condition   |
|--|--|-----|-----|-----|------|--|
| I <sub>DAC_AVDD</sub> [*2]   | DAC operating current on AV <sub>DD</sub> supply | -   | 340 | 550 | μA   | AV <sub>DD</sub> = 3.6V, no load, lowest code (0x000)  |
|  |  |     |     |     |      | AV <sub>DD</sub> = 3.6V, no load, middle code (0x800)  |
| I <sub>DAC_VREF</sub> [*2]   | DAC operating current on V <sub>REF</sub> supply | -   | -   | 160 | μA   | V <sub>REF</sub> = 3.6V, no load, middle code (0x800)  |
| T <sub>B</sub> [*2]  | Settling Time                                    | -   | 5   | 6   | μs   | Full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1 LSB, C <sub>LOAD</sub> ≤ 50pF, R <sub>LOAD</sub> ≥ 5kΩ |
| F <sub>S</sub>   | Update Rate                                      | -   | -   | 1   | MSPS | Max. frequency for a correct DAC_OUT change from code i to i+1LSB, C <sub>LOAD</sub> ≤ 50pF, R <sub>LOAD</sub> ≥ 5kΩ   |
| T <sub>WAKEUP</sub>  | Wake-up Time                                     | -   | 9   | 15  | μs   | Wakeup time from OFF state. Input code between lowest and highest possible codes.<br>DAC clock source = 1 MHz  |
| PSRR[*1]   | Power Supply Rejection Ratio                     | -   | -60 | -40 | dB   | No R <sub>LOAD</sub> , C <sub>LOAD</sub> = 50pF  |
| <b>Note:</b> <ol style="list-style-type: none"> <li>Guaranteed by design, not tested in production</li> <li>Guaranteed by characteristic, not tested in production.</li> <li>Resistive load between DACOUT and AV<sub>SS</sub>.</li> <li>Capacitive load at DACOUT pin.</li> </ol> |  |     |     |     |      |  |

9.5.7 Internal Voltage Reference

The maximum values are obtained for  $V_{DD} = 3.6\text{ V}$  and maximum ambient temperature ( $T_A$ ), and the typical values for  $T_A = 25\text{ }^\circ\text{C}$  and  $V_{DD} = 3.3\text{ V}$  unless otherwise specified.

| Symbol  | Parameter                  | Min  | Typ | Max  | Unit | Comments   |
|---|----------------------------|------|-----|------|------|--|
| $V_{REF\_INT}$  | Internal reference voltage | 1.55 | 1.6 | 1.65 | V    | $AV_{DD} \geq 2.0\text{ V}$                            |
|   |                            | 1.95 | 2.0 | 2.05 |      | $AV_{DD} \geq 2.2\text{ V}$                            |
|   |                            | 2.45 | 2.5 | 2.55 |      | $AV_{DD} \geq 2.7\text{ V}$                            |
|   |                            | 2.95 | 3.0 | 3.05 |      | $AV_{DD} \geq 3.2\text{ V}$                            |
| $T_s^{[1]}$   | Stable time                | -    | 0.5 | 0.8  | ms   | $C_L = 4.7\text{ }\mu\text{F}$ , $V_{REF}$ initial=0   |
|   |                            | -    | 9.3 | 13   | ms   | $C_L = 4.7\text{ }\mu\text{F}$ , $V_{REF}$ initial=3.6 |
|   |                            | -    | 24  | 180  | us   | $C_L = 1\text{ }\mu\text{F}$ , $V_{REF}$ initial=0     |
|   |                            | -    | 2   | 2.6  | ms   | $C_L = 1\text{ }\mu\text{F}$ , $V_{REF}$ initial=3.6   |
| <b>Note:</b>  |                            |      |     |      |      |  |
| 1. Guaranteed by characterization, not tested in production |                            |      |     |      |      |  |

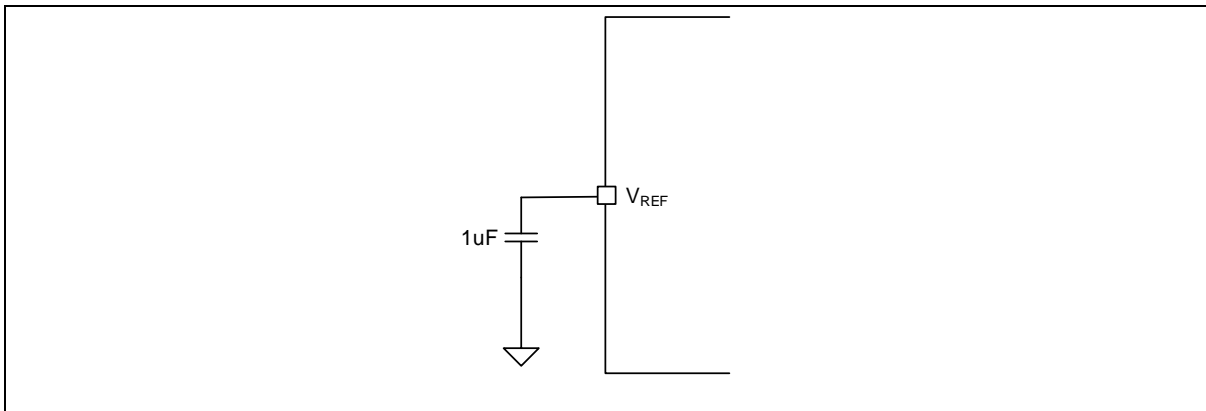


Figure 9-5 Typical Connection with Internal Voltage Reference

### 9.6 Communications Characteristics

#### 9.6.1 SPI Dynamic Characteristics

| Symbol                          | Parameter              | Specificaitons <sup>[1]</sup> |     |     |      | Test Conditions  |
|---------------------------------|------------------------|-------------------------------|-----|-----|------|--|
|                                 |                        | Min                           | Typ | Max | Unit |  |
| $F_{SPICLK}$<br>1/ $T_{SPICLK}$ | SPI clock frequency    | -                             | -   | 96  | MHz  | $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}, C_L = 30\text{ pF}$ |
|                                 |                        |                               |     | 96  |      | $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}, C_L = 30\text{ pF}$ |
|                                 |                        | -                             | -   | 96  |      | $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}, C_L = 30\text{ pF}$ |
| $t_{CLKH}$                      | Clock output High time | $T_{SPICLK} / 2$              |     |     | ns   |  |
| $t_{CLKL}$                      | Clock output Low time  | $T_{SPICLK} / 2$              |     |     | ns   |  |
| $t_{DS}$                        | Data input setup time  | 0                             | -   | -   | ns   |  |
| $t_{DH}$                        | Data input hold time   | 2                             | -   | -   | ns   |  |
| $t_V$                           | Data output valid time | -                             | -   | 2   | ns   | $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}, C_L = 30\text{ pF}$ |
|                                 |                        |                               |     | 2   | ns   | $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}, C_L = 30\text{ pF}$ |
|                                 |                        | -                             | -   | 2.2 | ns   | $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}, C_L = 30\text{ pF}$ |

**Note:**  
1. Guaranteed by design.

Table 9.6-1 SPI Master Mode Characteristics

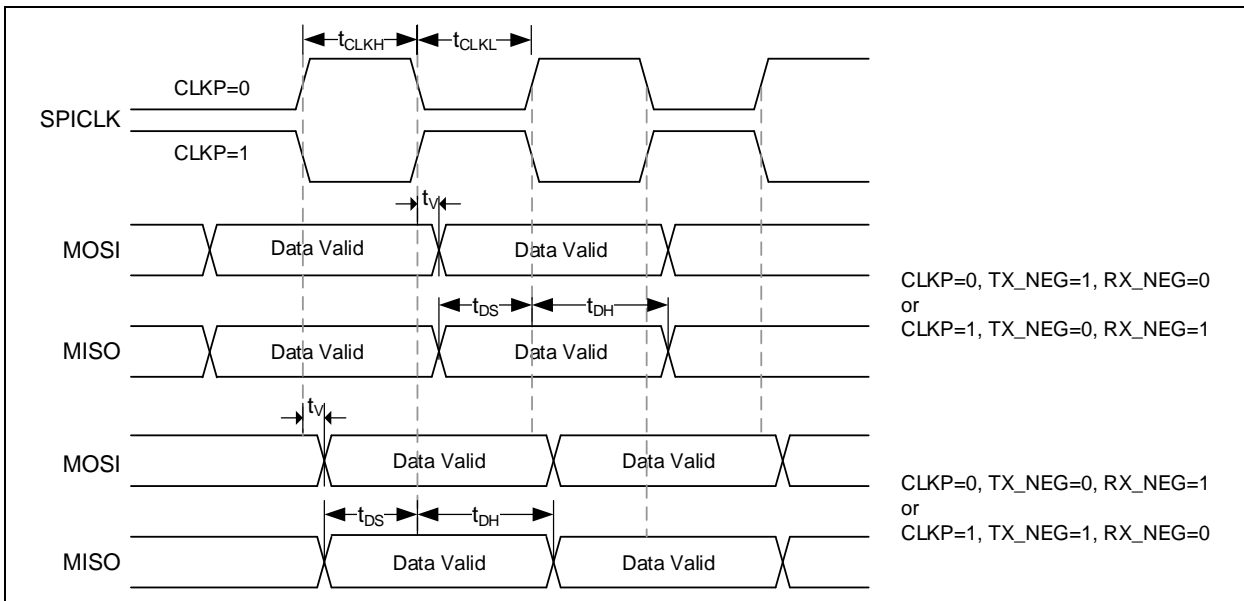


Figure 9-6 SPI Master Mode Timing Diagram

| Symbol  | Parameter               | Specifications <sup>[1]</sup>     |     |     |      | Test Conditions   |
|---|-------------------------|-----------------------------------|-----|-----|------|---|
|   |                         | Min                               | Typ | Max | Unit |   |
| F <sub>SPICLK</sub><br>1/ T <sub>SPICLK</sub> | SPI clock frequency     | -                                 | -   | 45  | MHz  | 3.0 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 30 pF |
|   |                         |                                   |     | 45  |      | 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 30 pF |
|   |                         | -                                 | -   | 33  |      | 1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 30 pF |
| t <sub>CLKH</sub>                             | Clock output High time  | T <sub>SPICLK</sub> / 2           |     |     | ns   |   |
| t <sub>CLKL</sub>                             | Clock output Low time   | T <sub>SPICLK</sub> / 2           |     |     | ns   |   |
| t <sub>SS</sub>                               | Slave select setup time | 1<br>T <sub>SPICLK</sub><br>+ 2ns | -   | -   | ns   | 3.0 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 30 pF |
|   |                         | 1<br>T <sub>SPICLK</sub><br>+ 2ns |     |     |      | 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 30 pF |
|   |                         | 1<br>T <sub>SPICLK</sub><br>+ 3ns | -   | -   |      | 1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 30 pF |
| t <sub>SH</sub>                               | Slave select hold time  | 1<br>T <sub>SPICLK</sub>          | -   | -   | ns   |   |
| t <sub>DS</sub>                               | Data input setup time   | 0                                 | -   | -   | ns   |   |
| t <sub>DH</sub>                               | Data input hold time    | 2                                 | -   | -   | ns   |   |
| t <sub>V</sub>                                | Data output valid time  | -                                 | -   | 11  | ns   | 3.0 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 30 pF |
|   |                         |                                   |     | 11  |      | 2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 30 pF |
|   |                         | -                                 | -   | 15  |      | 1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>L</sub> = 30 pF |
| <b>Note:</b>                                  |                         |                                   |     |     |      |   |
| 1. Guaranteed by design.                      |                         |                                   |     |     |      |   |

Table 9.6-2 SPI Slave Mode Characteristics

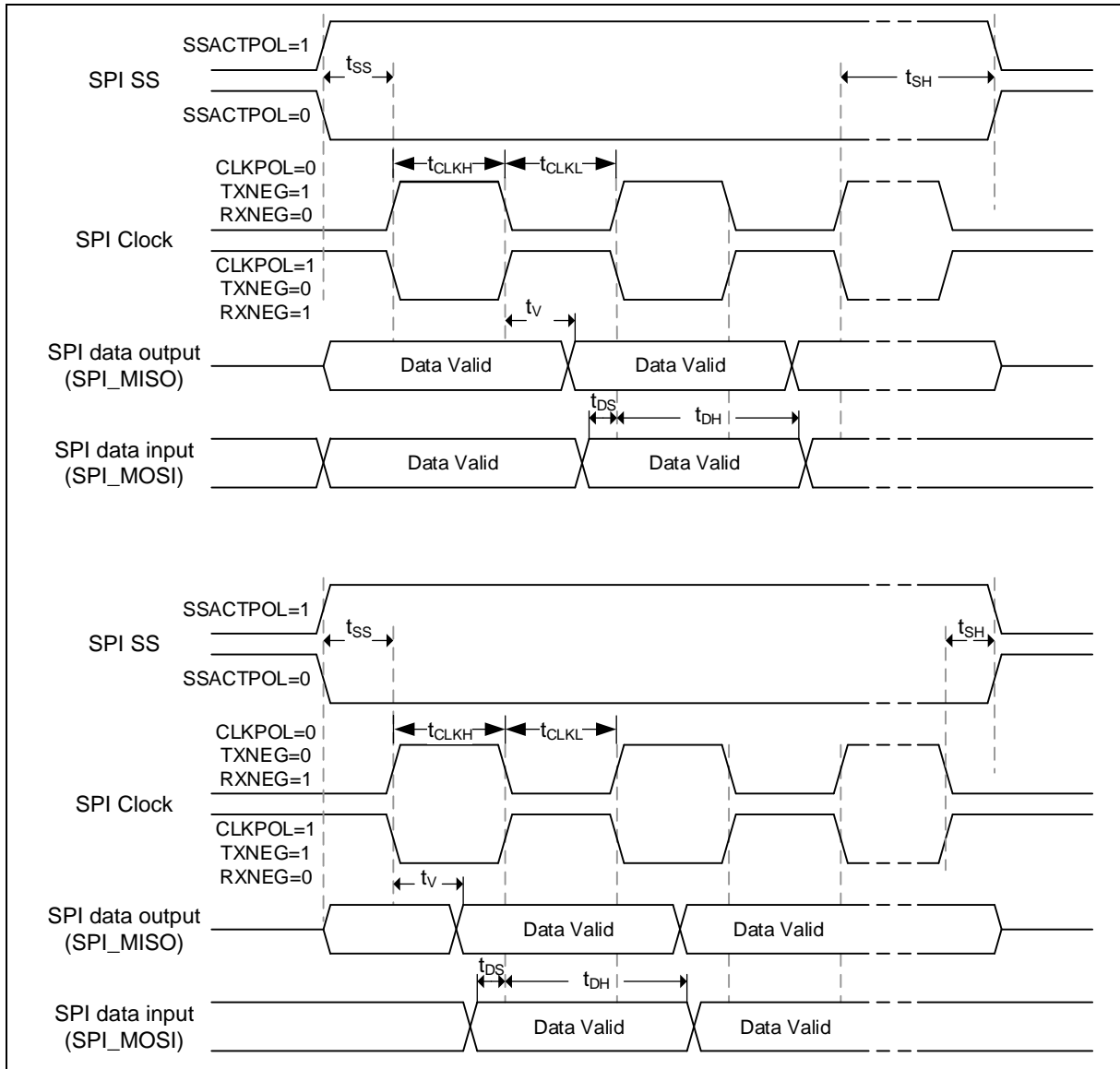


Figure 9-7 SPI Slave Mode Timing Diagram

9.6.2 SPI - I<sup>2</sup>S Dynamic Characteristics

| Symbol                         | Parameter                                     | Min <sup>[1]</sup> | Max <sup>[1]</sup> | Unit | Test Conditions  |
|--------------------------------|---|--------------------|--------------------|------|--|
| $t_w(\text{CKH})$              | I <sup>2</sup> S clock high time              | 80                 | -                  | ns   | Master $f_{\text{PCLK}} = 48 \text{ MHz}$ , data: 24 bits, audio frequency = 128 kHz |
| $t_w(\text{CKL})$              | I <sup>2</sup> S clock low time               | 80                 | -                  |      |  |
| $t_v(\text{WS})$               | WS valid time                                 | 2                  | 6                  |      |  |
| $t_h(\text{WS})$               | WS hold time                                  | 2                  | -                  |      |  |
| $t_{\text{su}}(\text{WS})$     | WS setup time                                 | 24                 | -                  |      |  |
| $t_h(\text{WS})$               | WS hold time                                  | 0                  | -                  |      |  |
| $\text{DuCy}(\text{SCK})$      | I <sup>2</sup> S slave input clock duty cycle | 30                 | 70                 | %    | Slave mode   |
| $t_{\text{su}}(\text{SD\_MR})$ | Data input setup time                         | 10                 | -                  | ns   | Master receiver  |
| $t_{\text{su}}(\text{SD\_SR})$ |   | 7                  | -                  |      | Slave receiver   |
| $t_h(\text{SD\_MR})$           | Data input hold time                          | 7                  | -                  |      | Master receiver  |
| $t_h(\text{SD\_SR})$           |   | 4                  | -                  |      | Slave receiver   |
| $t_v(\text{SD\_ST})$           | Data output valid time                        | -                  | 25                 |      | Slave transmitter (after enable edge)  |
| $t_h(\text{SD\_ST})$           | Data output hold time                         | 4                  | -                  |      | Slave transmitter (after enable edge)  |
| $t_v(\text{SD\_MT})$           | Data output valid time                        | -                  | 4                  |      | Master transmitter (after enable edge)   |
| $t_h(\text{SD\_MT})$           | Data output hold time                         | 0                  | -                  |      | Master transmitter (after enable edge)   |
| <b>Note:</b>                   |   |                    |                    |      |  |
| 1. Guaranteed by design.       |   |                    |                    |      |  |

Table 9.6-3 I<sup>2</sup>S Characteristics

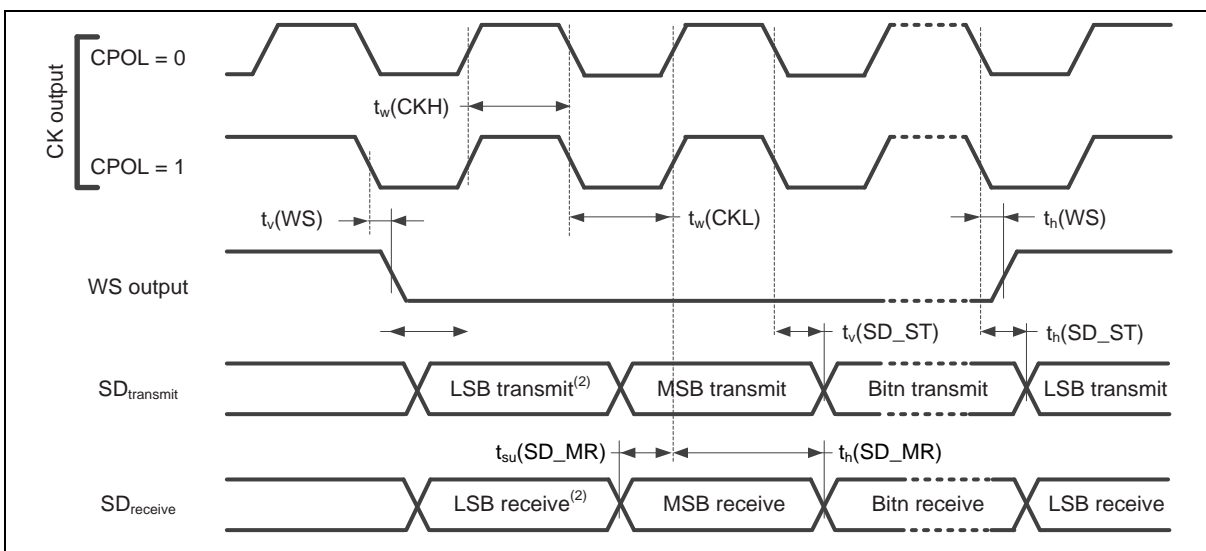


Figure 9-8 I<sup>2</sup>S Master Mode Timing Diagram

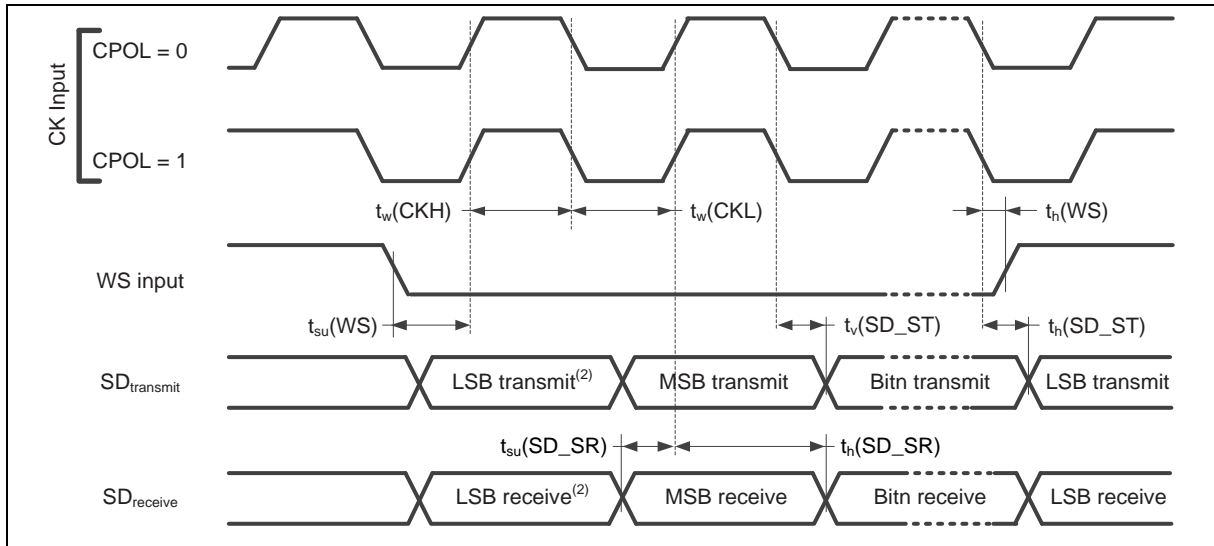


Figure 9-9 I<sup>2</sup>S Slave Mode Timing Diagram



9.6.3 I<sup>2</sup>S Dynamic Characteristics

| Symbol                         | Parameter                                     | Min | Max | Unit | Test Conditions  |
|--------------------------------|---|-----|-----|------|--|
| $t_w(\text{CKH})$              | I <sup>2</sup> S clock high time              | 40  | -   | ns   | Master $f_{\text{PCLK}} = \text{MHz}$ , data: 24 bits, audio frequency = 256 kHz |
| $t_w(\text{CKL})$              | I <sup>2</sup> S clock low time               | 40  | -   |      |  |
| $t_v(\text{WS})$               | WS valid time                                 | 4   | 16  |      |  |
| $t_h(\text{WS})$               | WS hold time                                  | 1   | -   |      |  |
| $t_{\text{su}}(\text{WS})$     | WS setup time                                 | 24  | -   |      |  |
| $t_h(\text{WS})$               | WS hold time                                  | 0   | -   |      |  |
| $\text{DuCy}(\text{SCK})$      | I <sup>2</sup> S slave input clock duty cycle | 30  | 70  |      |  |
| $t_{\text{su}}(\text{SD\_MR})$ | Data input setup time                         | 10  | -   | ns   | Master receiver  |
| $t_{\text{su}}(\text{SD\_SR})$ |   | 7   | -   |      | Slave receiver   |
| $t_h(\text{SD\_MR})$           | Data input hold time                          | 7   | -   |      | Master receiver  |
| $t_h(\text{SD\_SR})$           |   | 4   | -   |      | Slave receiver   |
| $t_v(\text{SD\_ST})$           | Data output valid time                        | -   | 10  |      | Slave transmitter (after enable edge)  |
| $t_h(\text{SD\_ST})$           | Data output hold time                         | 4   | -   |      | Slave transmitter (after enable edge)  |
| $t_v(\text{SD\_MT})$           | Data output valid time                        | -   | 4   |      | Master transmitter (after enable edge)   |
| $t_h(\text{SD\_MT})$           | Data output hold time                         | 0   | -   |      | Master transmitter (after enable edge)   |
| <b>Note:</b>                   |   |     |     |      |  |
| 1. Guaranteed by design.       |   |     |     |      |  |

Table 9.6-4 I<sup>2</sup>S Characteristics

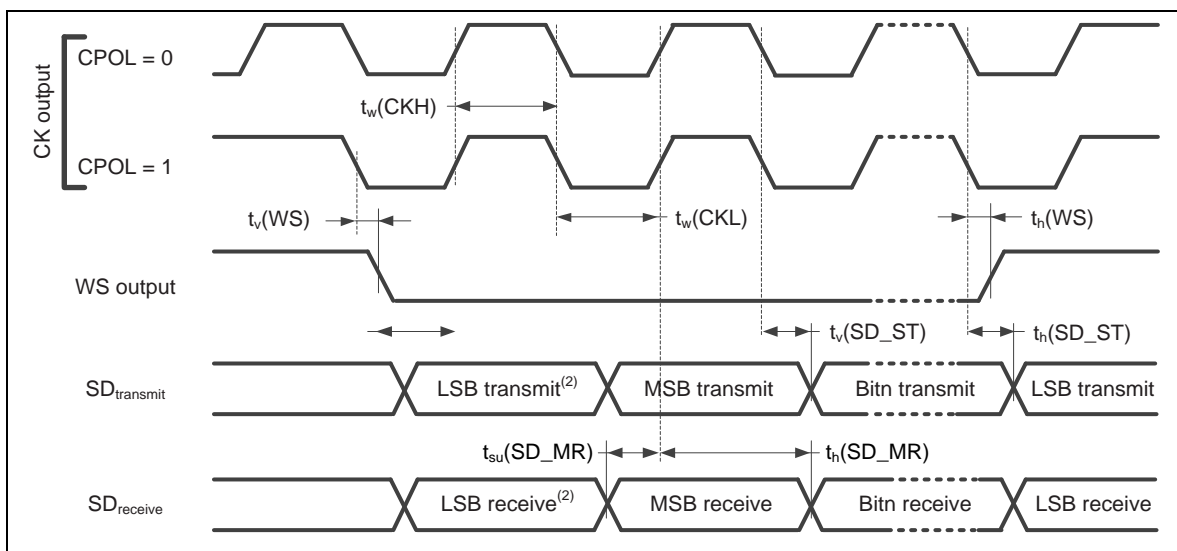


Figure 9-10 I<sup>2</sup>S Master Mode Timing Diagram

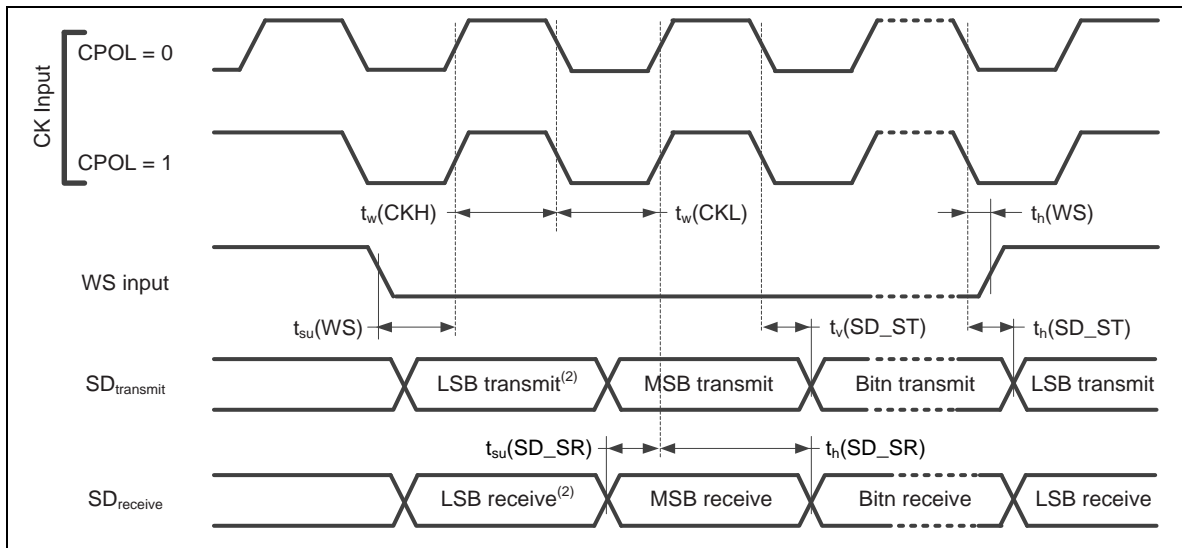


Figure 9-11 I<sup>2</sup>S Slave Mode Timing Diagram

9.6.4 I<sup>2</sup>C Dynamic Characteristics

| Symbol              | Parameter                           | Standard Mode <sup>[1][2]</sup> |                     | Fast Mode <sup>[1][2]</sup> |                    | Unit |
|---------------------|-------------------------------------|---------------------------------|---------------------|-----------------------------|--------------------|------|
|                     |                                     | Min                             | Max                 | Min                         | Max                |      |
| t <sub>LOW</sub>    | SCL low period                      | 4.7                             | -                   | 1.3                         | -                  | μs   |
| t <sub>HIGH</sub>   | SCL high period                     | 4                               | -                   | 0.6                         | -                  | μs   |
| t <sub>SU;STA</sub> | Repeated START condition setup time | 4.7                             | -                   | 0.6                         | -                  | μs   |
| t <sub>HD;STA</sub> | START condition hold time           | 4                               | -                   | 0.6                         | -                  | μs   |
| t <sub>SU;STO</sub> | STOP condition setup time           | 4                               | -                   | 0.6                         | -                  | μs   |
| t <sub>BUF</sub>    | Bus free time                       | 4.7 <sup>[3]</sup>              | -                   | 1.2 <sup>[3]</sup>          | -                  | μs   |
| t <sub>SU;DAT</sub> | Data setup time                     | 250                             | -                   | 100                         | -                  | ns   |
| t <sub>HD;DAT</sub> | Data hold time                      | 0 <sup>[4]</sup>                | 3.45 <sup>[5]</sup> | 0 <sup>[4]</sup>            | 0.8 <sup>[5]</sup> | μs   |
| t <sub>r</sub>      | SCL/SDA rise time                   | -                               | 1000                | 20+0.1C <sub>b</sub>        | 300                | ns   |
| t <sub>f</sub>      | SCL/SDA fall time                   | -                               | 300                 | -                           | 300                | ns   |
| C <sub>b</sub>      | Capacitive load for each bus line   | -                               | 400                 | -                           | 400                | pF   |

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I<sup>2</sup>C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I<sup>2</sup>C frequency.
3. I<sup>2</sup>C controller must be retrigged immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 9.6-5 I<sup>2</sup>C Characteristics

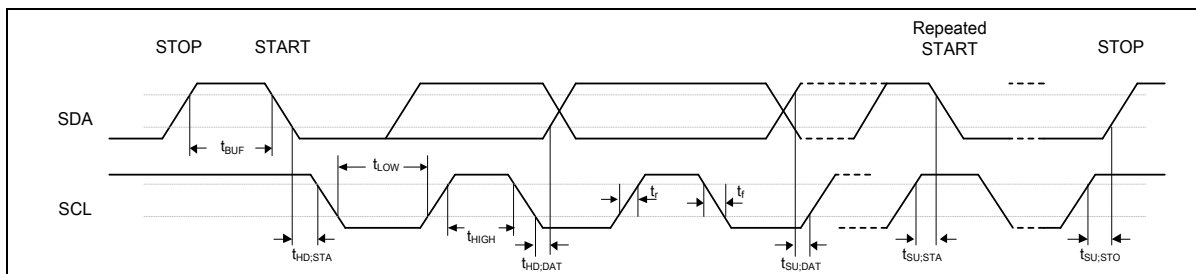


Figure 9-12 I<sup>2</sup>C Timing Diagram

9.6.5 USB Characteristics

9.6.5.1 USB Full-Speed Characteristics

| Symbol           | Parameter   | Min.  | Typ. | Max.  | Unit | Test Conditions |
|------------------|---|-------|------|-------|------|-----------------|
| V <sub>DD</sub>  | Operation Voltage                                   | 3.0   |      | 3.6   | V    |                 |
| V <sub>IH</sub>  | Input High (driven)                                 | 2.0   | -    | -     | V    | -               |
| V <sub>IL</sub>  | Input Low   | -     | -    | 0.8   | V    | -               |
| V <sub>DI</sub>  | Differential Input Sensitivity                      | -     | 0.2  | -     | V    | PADP-PADM       |
| V <sub>CM</sub>  | Differential Common-mode Range                      | 0.8   | -    | 2.5   | V    | -               |
| V <sub>SE</sub>  | Single-ended Receiver Threshold                     | 0.8   | -    | 2.0   | V    | -               |
|                  | Receiver Hysteresis                                 | -     | 200  | -     | mV   | Single End RX   |
| V <sub>OL</sub>  | Output Low (driven)                                 | 0     | -    | 0.3   | V    | -               |
| V <sub>OH</sub>  | Output High (driven)                                | 2.8   | -    | 3.6   | V    | -               |
| V <sub>CRS</sub> | Output Signal Cross Voltage                         | 1.3   | -    | 2.0   | V    | -               |
| R <sub>PU</sub>  | Pull-up Resistor                                    | 0.9   | 1.2  | 1.575 | kΩ   | DATARPU2=1      |
| R <sub>PU</sub>  | Pull-up Resistor                                    | 1.425 | 2.3  | 3.09  | kΩ   | DATARPU2=0      |
| R <sub>PD</sub>  | Pull-down Resistor                                  | 14.25 | 19.5 | 24.8  | kΩ   | -               |
| V <sub>TRM</sub> | TERMINATION Voltage for Upstream port pull up (RPU) | 3.0   | -    | 3.6   | V    | -               |
| Z <sub>DRV</sub> | Driver Output Resistance                            | -     | 10   | -     | Ω    | -               |
| C <sub>IN</sub>  | Transceiver Capacitance                             | -     | -    | 26    | pF   | -               |

Table 9.6-6 USB Full-Speed Characteristics

9.6.5.2 USB Full-Speed PHY characteristics

| Symbol  | Parameter                   | Min <sup>[*1]</sup> | Typ | Max <sup>[*1]</sup> | Unit | Test Conditions                                      |
|---|-----------------------------|---------------------|-----|---------------------|------|--|
| T <sub>FR</sub>   | rise time                   | 4                   | -   | 20                  | ns   | -  |
| T <sub>FF</sub>   | fall time                   | 4                   | -   | 20                  | ns   | -  |
| T <sub>FRFF</sub>   | rise and fall time matching | 90                  | -   | 111.11              | %    | T <sub>FRFF</sub> = T <sub>FR</sub> /T <sub>FF</sub> |
| <b>Note:</b>  |                             |                     |     |                     |      |  |
| 1. Guaranteed by characterization result, not tested in production. |                             |                     |     |                     |      |  |

Table 9.6-7 USB Full-Speed PHY Characteristics

9.6.6 SDIO Characteristics

9.6.6.1 SDIO Default Mode Timing

| Symbol               | Parameter                                | Min   | Typ | Max | Unit | Test Condition |
|----------------------|--|-------|-----|-----|------|----------------|
| $T_{P\_SD\_CLK}$     | SD_CLK Period<br>(Data Transfer Mode)    | 40    | -   | -   | ns   | -              |
| $T_{P\_SD\_CLK\_ID}$ | SD_CLK Period<br>(Identification Mode)   | 2,500 | -   | -   | ns   | -              |
| $T_{H\_SD\_CLK}$     | SD_CLK High Time                         | -     | 20  | -   | ns   | -              |
| $T_{L\_SD\_CLK}$     | SD_CLK Low Time                          | -     | 20  | -   | ns   | -              |
| $T_{SU\_SD\_IN}$     | SD_DATA Setup Time to<br>SD_CLK Rising   | 5     | -   | -   | ns   | -              |
| $T_{HD\_SD\_IN}$     | SD_DATA Hold Time from<br>SD_CLK Rising  | 5     | -   | -   | ns   | -              |
| $T_{DLY\_SD\_OUT}$   | SD_CLK Falling to<br>Valid SD_DATA Delay | -     | -   | 14  | ns   | -              |

**Note:**

- Guaranteed by characterization result, not tested in production.

Table 9.6-8 SDIO Default Mode Timing

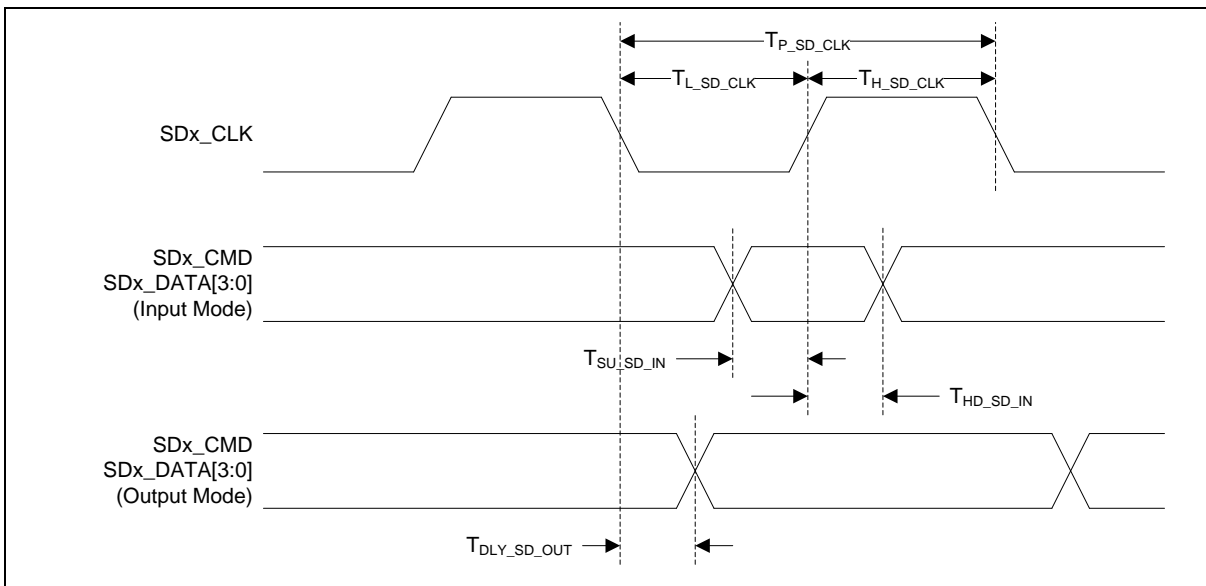


Figure 9-13 SDIO Default Mode

9.6.6.2 SDIO Dynamic characteristics

| Symbol             | Parameter                             | Min | Typ | Max | Unit | Test Condition |
|--------------------|---------------------------------------|-----|-----|-----|------|----------------|
| $T_{P\_SD\_CLK}$   | SD_CLK Period                         | 20  | -   | -   | ns   | -              |
| $T_{H\_SD\_CLK}$   | SD_CLK High Time                      | 7   | -   | -   | ns   | -              |
| $T_{L\_SD\_CLK}$   | SD_CLK Low Time                       | 7   | -   | -   | ns   | -              |
| $T_{SU\_SD\_IN}$   | SD_DATA Setup Time to SD_CLK Rising   | 6   | -   | -   | ns   | -              |
| $T_{HD\_SD\_IN}$   | SD_DATA Hold Time from SD_CLK Rising  | 2   | -   | -   | ns   | -              |
| $T_{DLY\_SD\_OUT}$ | SD_CLK Falling to Valid SD_DATA Delay | -   | -   | 14  | ns   | -              |
| $T_{HD\_SD\_OUT}$  | SD_DATA Hold Time from SD_CLK Rising  | 2.5 | -   | -   | ns   | -              |

**Note:**

- Guaranteed by characterization result, not tested in production.

Table 9.6-9 SDIO Dynamic Characteristics

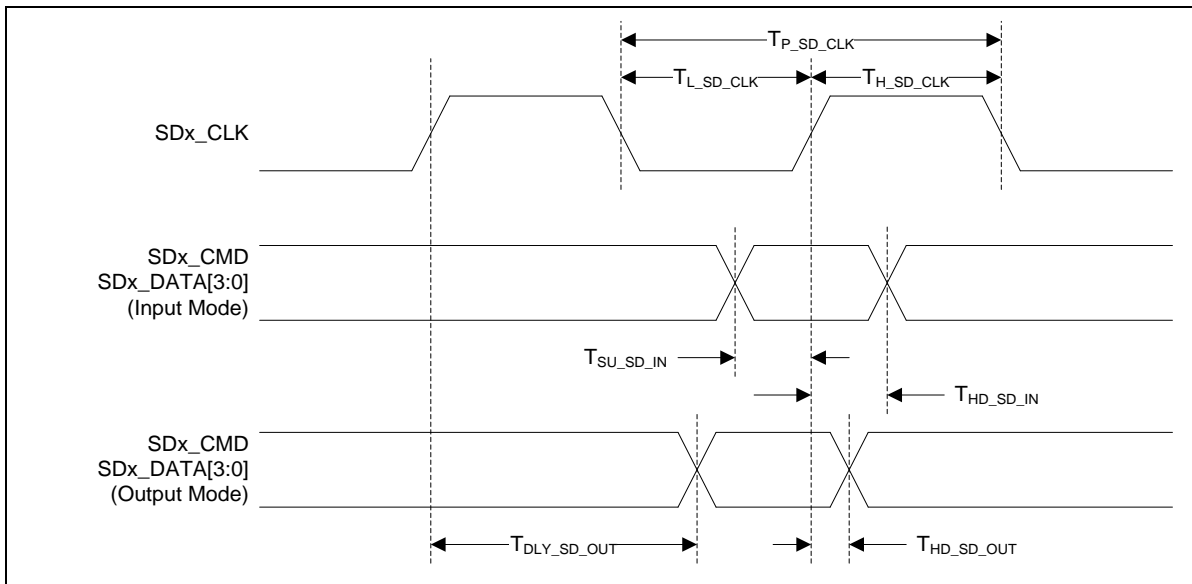


Figure 9-14 SDIO High-speed Mode

9.6.7 EBI Characteristics

| Symbol            | Parameter   | Min              | Typ | Max | Unit             | Test Condition |
|-------------------|---|------------------|-----|-----|------------------|----------------|
| $T_{IACS}$        | Address Setup Time to EBI_nCS Falling Edge            | -                | 0   | -   | $T_{HCLK}^{(1)}$ | -              |
| $T_{ICOS}$        | EBI_nCS Setup Time to EBI_nWE or EBI_nOE Falling Edge | -                | 1   | -   | $T_{HCLK}^{(1)}$ | -              |
| $T_{IACC}$        | EBI_nWE or EBI_nOE Active Low Time                    | 1 <sup>[2]</sup> | -   | 32  | $T_{HCLK}^{(1)}$ | -              |
| $T_{ICOH}$        | EBI_nCS Hold Time from EBI_nWE or EBI_nOE Rising Edge | 0                | -   | 8   | $T_{HCLK}^{(1)}$ | -              |
| $T_{SU\_EBI\_RD}$ | EBI_DATA Read Setup Time to EBI_nOE Rising Edge       | 1                | -   | -   | $T_{HCLK}^{(1)}$ | -              |

Notes:

1.  $T_{HCLK}$  is the period of EBI's operating clock.
2.  $T_{IACC}$  must be set for at least 13ns.

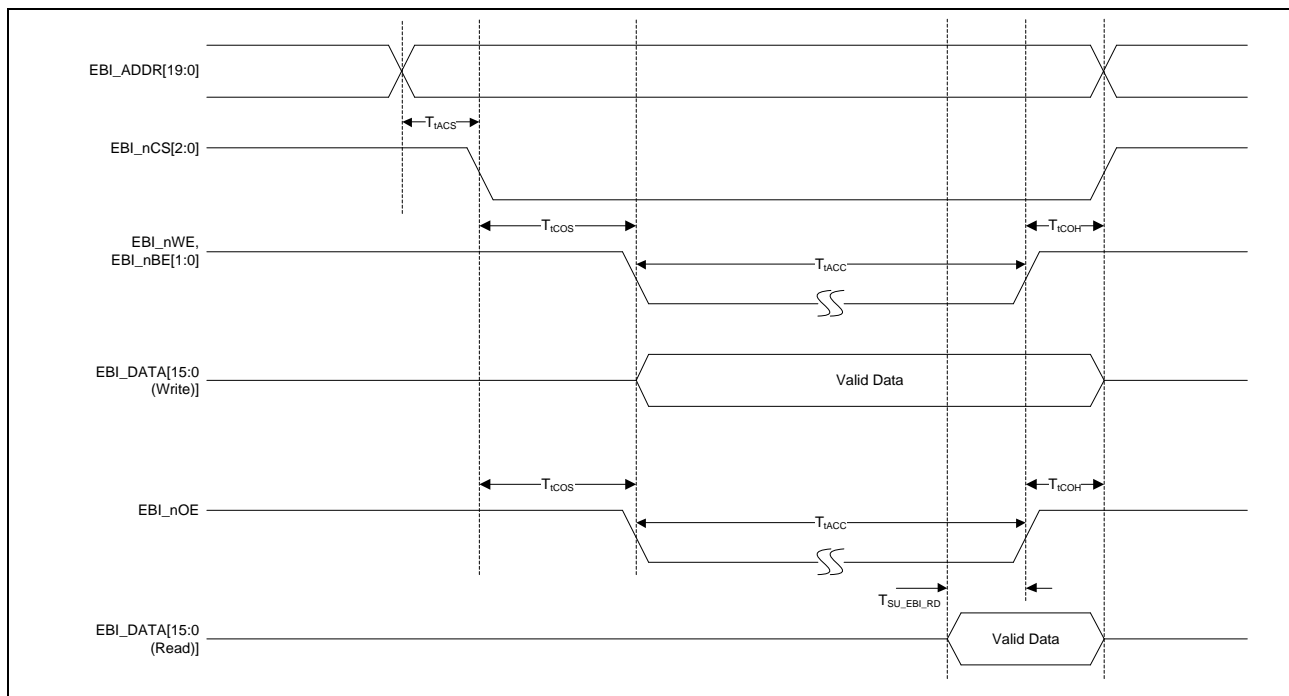


Figure 9-15 External Bus Interface Timing Diagram

9.6.8 Camera Capture Interface (CCAP) Characteristics

| Symbol              | Parameter  | Min | Typ  | Max | Unit | Test Condition |
|---------------------|--|-----|------|-----|------|----------------|
| $T_{P\_CCAP\_PCLK}$ | CCAP_PCLK Period   | 20  | -    | -   | ns   |                |
| $T_{H\_CCAP\_PCLK}$ | CCAP_PCLK High Time  | -   | 10.0 | -   | ns   |                |
| $T_{L\_CCAP\_PCLK}$ | CCAP_PCLK Low Time   | -   | 10.0 | -   | ns   |                |
| $T_{SU\_CCAP\_IN}$  | CCAP_HSYNC, CCAP_VSYNC, CCAP_FIELD and CCAP_DATA Setup Time to CCAP_PCLK Rising  | 4   | -    | -   | ns   |                |
| $T_{HD\_CCAP\_IN}$  | CCAP_HSYNC, CCAP_VSYNC, CCAP_FIELD and CCAP_DATA Hold Time from CCAP_PCLK Rising | 1   | -    | -   | ns   |                |

**Note:**

- Guaranteed by design.

Table 9.6-10 Camera Capture Interface Timing

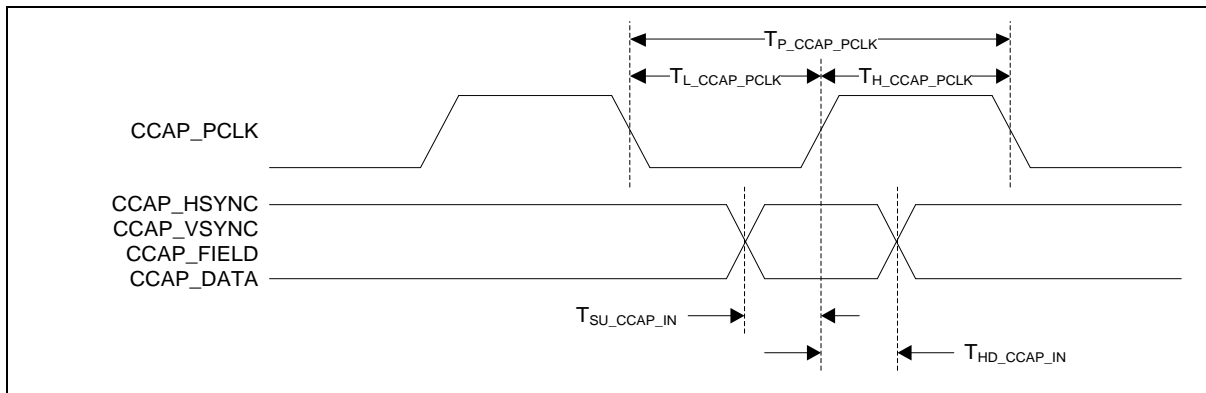


Figure 9-16 Camera Capture Interface Timing Diagram



### 9.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

| Symbol   | Parameter       | Min    | Typ  | Max  | Unit                  | Test Condition                                     |
|--|-----------------|--------|------|------|-----------------------|--|
| $V_{FLA}^{[1]}$  | Supply voltage  | 1.08   | -    | 1.32 | V                     | $T_A = 25^\circ\text{C}$                           |
| $T_{ERASE}$  | Page erase time | -      | -    | 160  | ms                    |  |
| $T_{PROG}$   | Program time    | -      | -    | 50   | $\mu\text{s}$         |  |
| $I_{DD1}$  | Read current    | -      | 4.12 | -    | mA                    |  |
| $I_{DD2}$  | Program current | -      | 5    | -    | mA                    |  |
| $I_{DD3}$  | Erase current   | -      | 5    | -    | mA                    |  |
| $N_{ENDUR}$  | Endurance       | 10,000 | -    |      | cycles <sup>[2]</sup> | $T_J = -40^\circ\text{C} \sim 125^\circ\text{C}$   |
| $T_{RET}$  | Data retention  | TBD    | -    | -    | year                  | 10 kcycle <sup>[3]</sup> $T_A = 55^\circ\text{C}$  |
|  |                 | 10     | -    | -    | year                  | 10 kcycle <sup>[3]</sup> $T_A = 85^\circ\text{C}$  |
|  |                 | TBD    | -    | -    | year                  | 10 kcycle <sup>[3]</sup> $T_A = 125^\circ\text{C}$ |
| <b>Note:</b> <ol style="list-style-type: none"> <li><math>V_{FLA}</math> is source from chip internal LDO output voltage.</li> <li>Number of program/erase cycles.</li> <li>Guaranteed by design.</li> </ol> |                 |        |      |      |                       |  |

## 10 ABBREVIATIONS

### 10.1 Abbreviations

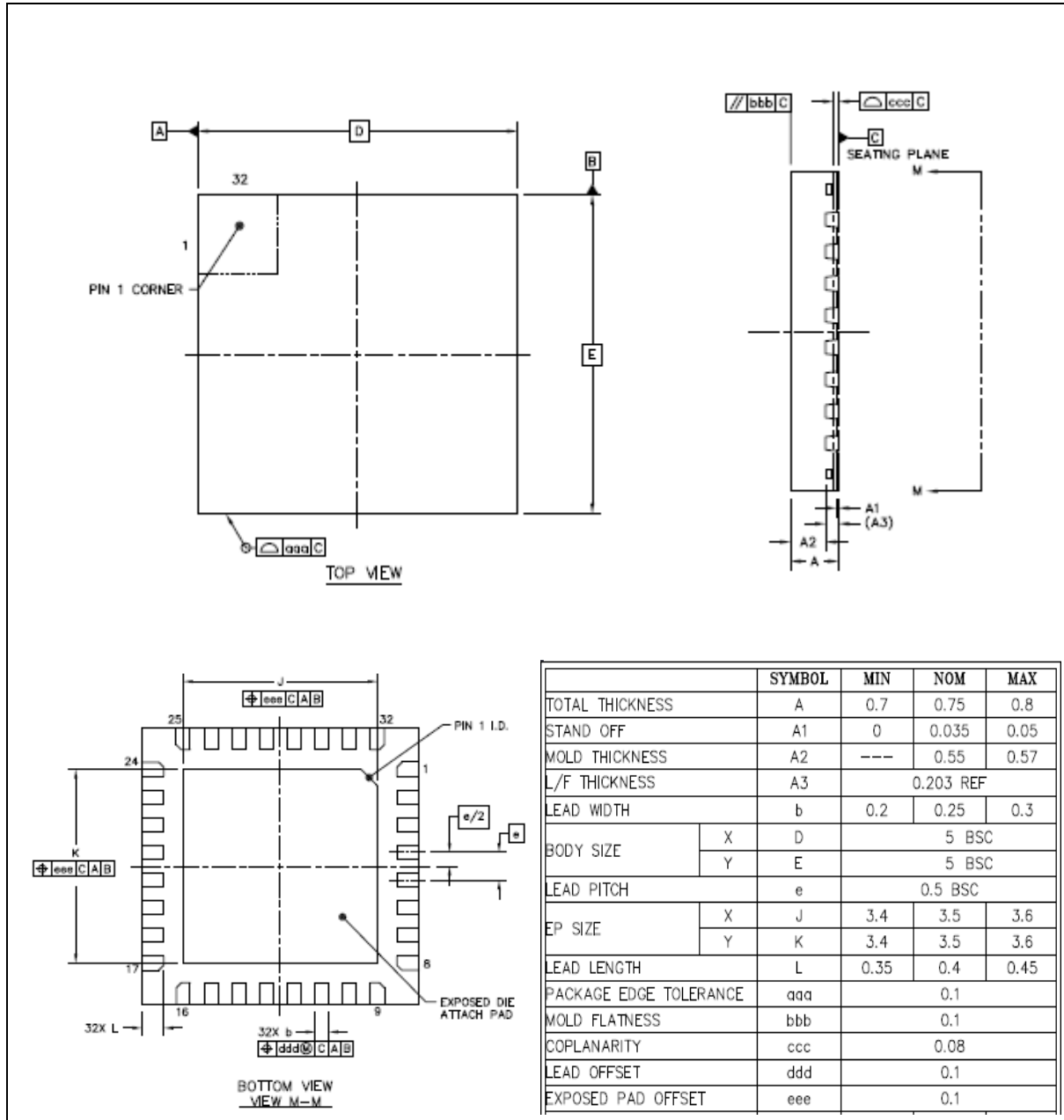
| Acronym | Description                                     |
|---------|---|
| ACMP    | Analog Comparator Controller                    |
| ADC     | Analog-to-Digital Converter                     |
| AES     | Advanced Encryption Standard                    |
| APB     | Advanced Peripheral Bus                         |
| AHB     | Advanced High-Performance Bus                   |
| BOD     | Brown-out Detection                             |
| CAN     | Controller Area Network                         |
| CCAP    | Camera Capture Interface                        |
| DAP     | Debug Access Port                               |
| DES     | Data Encryption Standard                        |
| EADC    | Enhanced Analog-to-Digital Converter            |
| EBI     | External Bus Interface                          |
| EMAC    | Ethernet MAC Controller                         |
| EPWM    | Enhanced Pulse Width Modulation                 |
| FIFO    | First In, First Out                             |
| FMC     | Flash Memory Controller                         |
| FPU     | Floating-point Unit                             |
| GPIO    | General-Purpose Input/Output                    |
| HCLK    | The Clock of Advanced High-Performance Bus      |
| HIRC    | 12 MHz Internal High Speed RC Oscillator        |
| HXT     | 4~24 MHz External High Speed Crystal Oscillator |
| IAP     | In Application Programming                      |
| ICP     | In Circuit Programming                          |
| ISP     | In System Programming                           |
| LDO     | Low Dropout Regulator                           |
| LIN     | Local Interconnect Network                      |
| LIRC    | 10 kHz internal low speed RC oscillator (LIRC)  |
| MPU     | Memory Protection Unit                          |
| NVIC    | Nested Vectored Interrupt Controller            |
| PCLK    | The Clock of Advanced Peripheral Bus            |
| PDMA    | Peripheral Direct Memory Access                 |
| PLL     | Phase-Locked Loop                               |

|      |   |
|------|---|
| PWM  | Pulse Width Modulation                      |
| QEI  | Quadrature Encoder Interface                |
| SD   | Secure Digital                              |
| SPI  | Serial Peripheral Interface                 |
| SPS  | Samples per Second                          |
| TDES | Triple Data Encryption Standard             |
| TK   | Touch Key                                   |
| TMR  | Timer Controller                            |
| UART | Universal Asynchronous Receiver/Transmitter |
| UCID | Unique Customer ID                          |
| USB  | Universal Serial Bus                        |
| WDT  | Watchdog Timer                              |
| WWDT | Window Watchdog Timer                       |

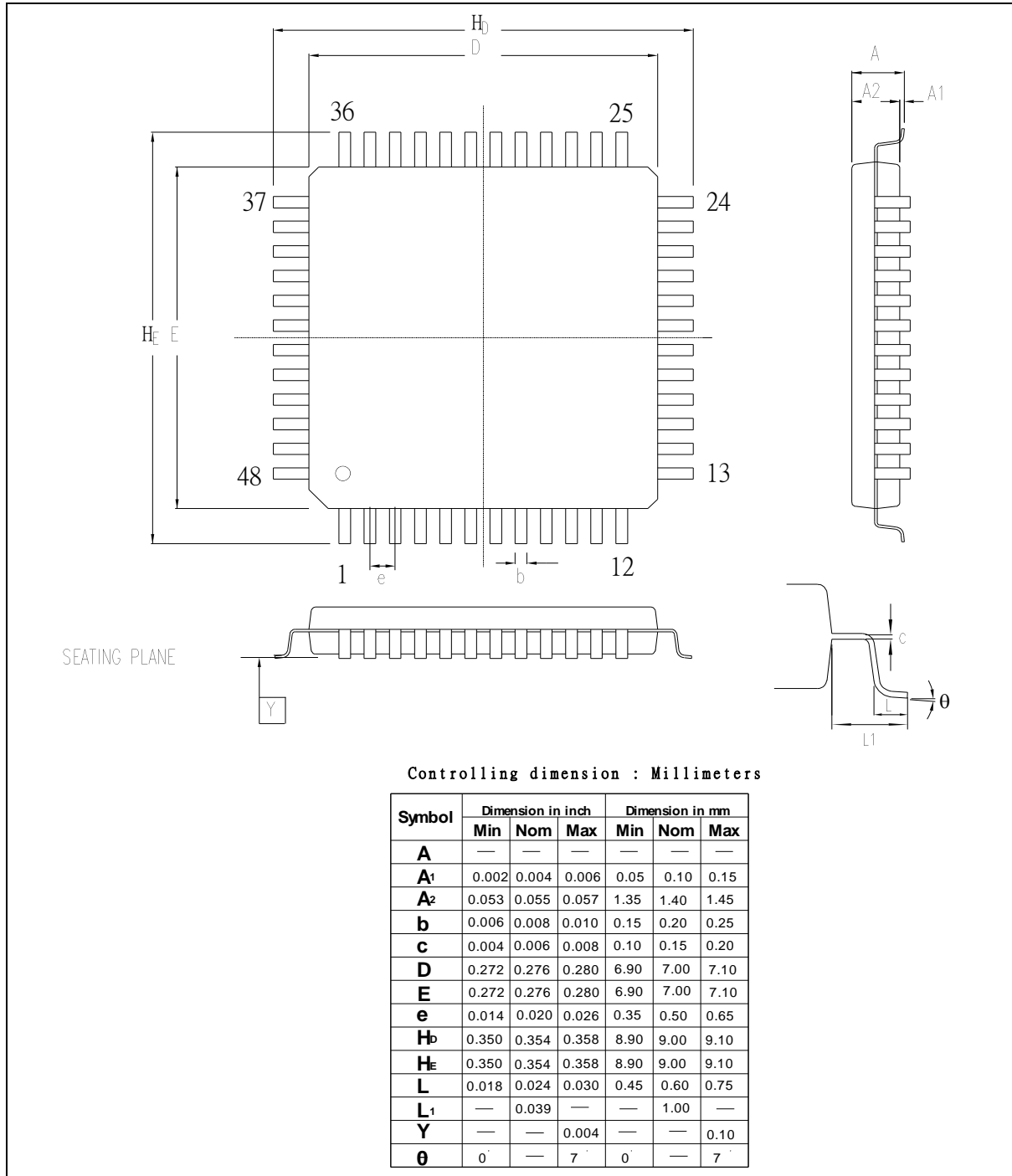
Table 10.1-1 List of Abbreviations

11 PACKAGE DIMENSIONS

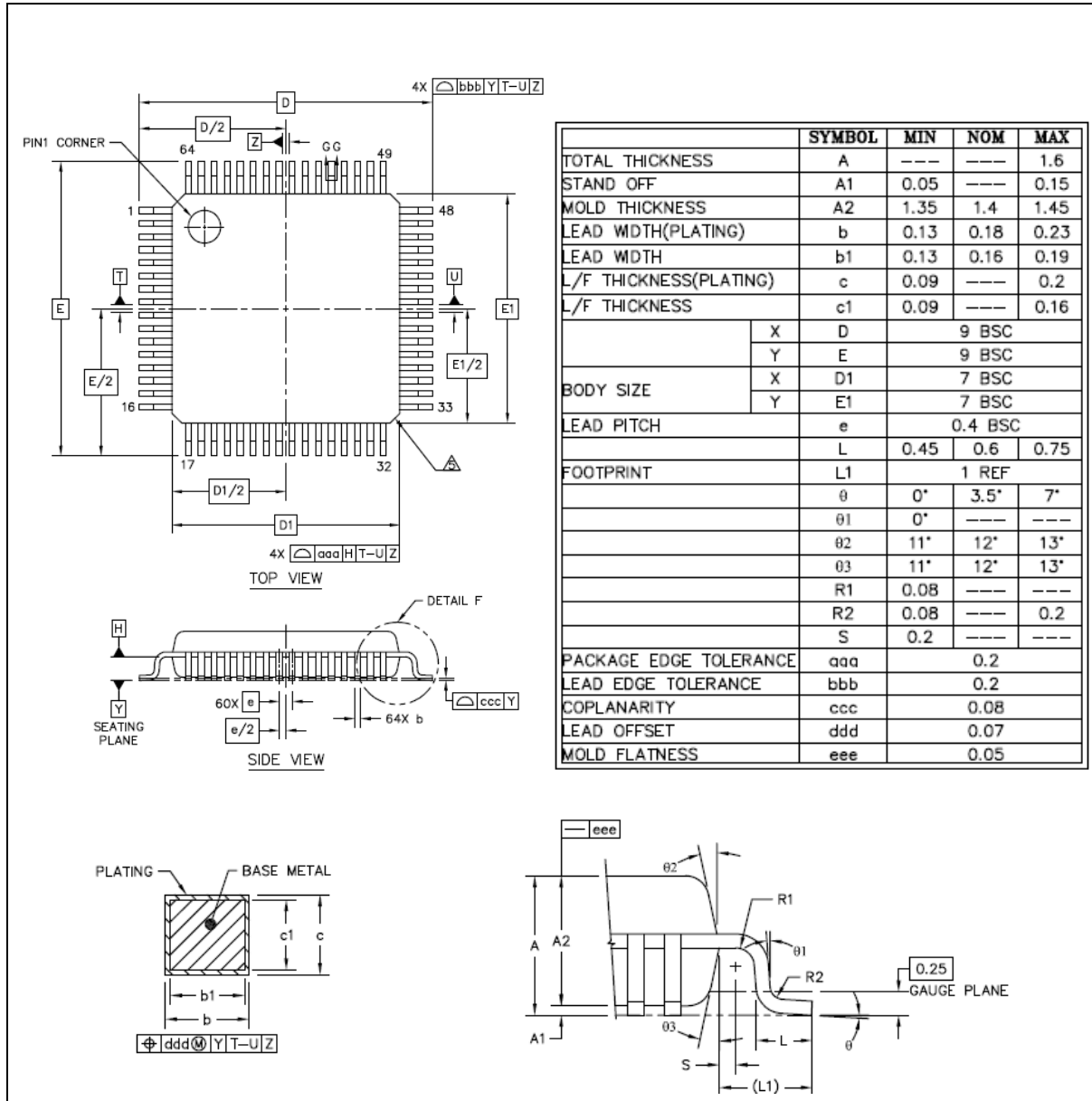
11.1 QFN 33L (5x5x0.8 mm<sup>3</sup> Pitch 0.5 mm)



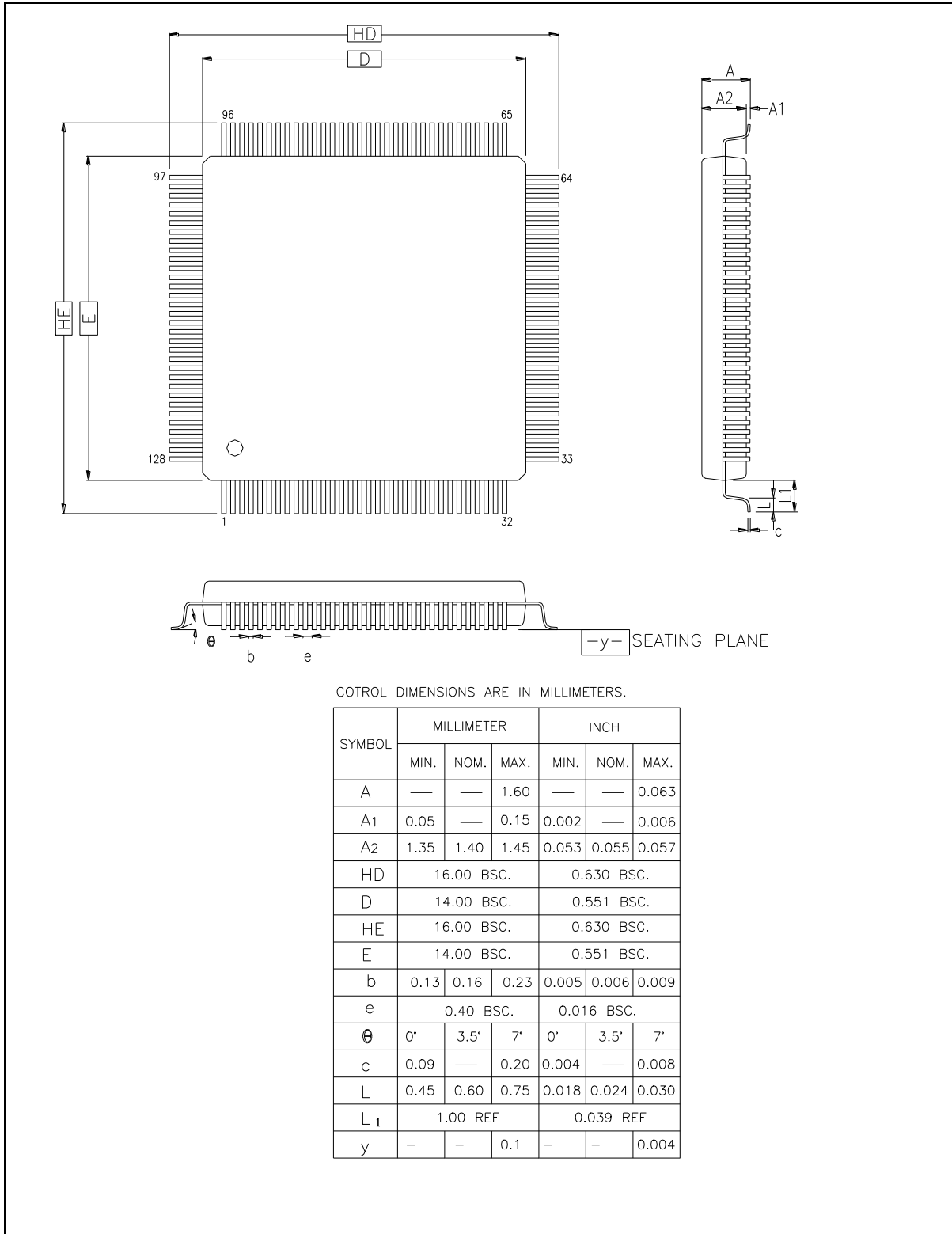
11.2 LQFP 48L (7x7x1.4 mm<sup>3</sup> Footprint 2.0mm)



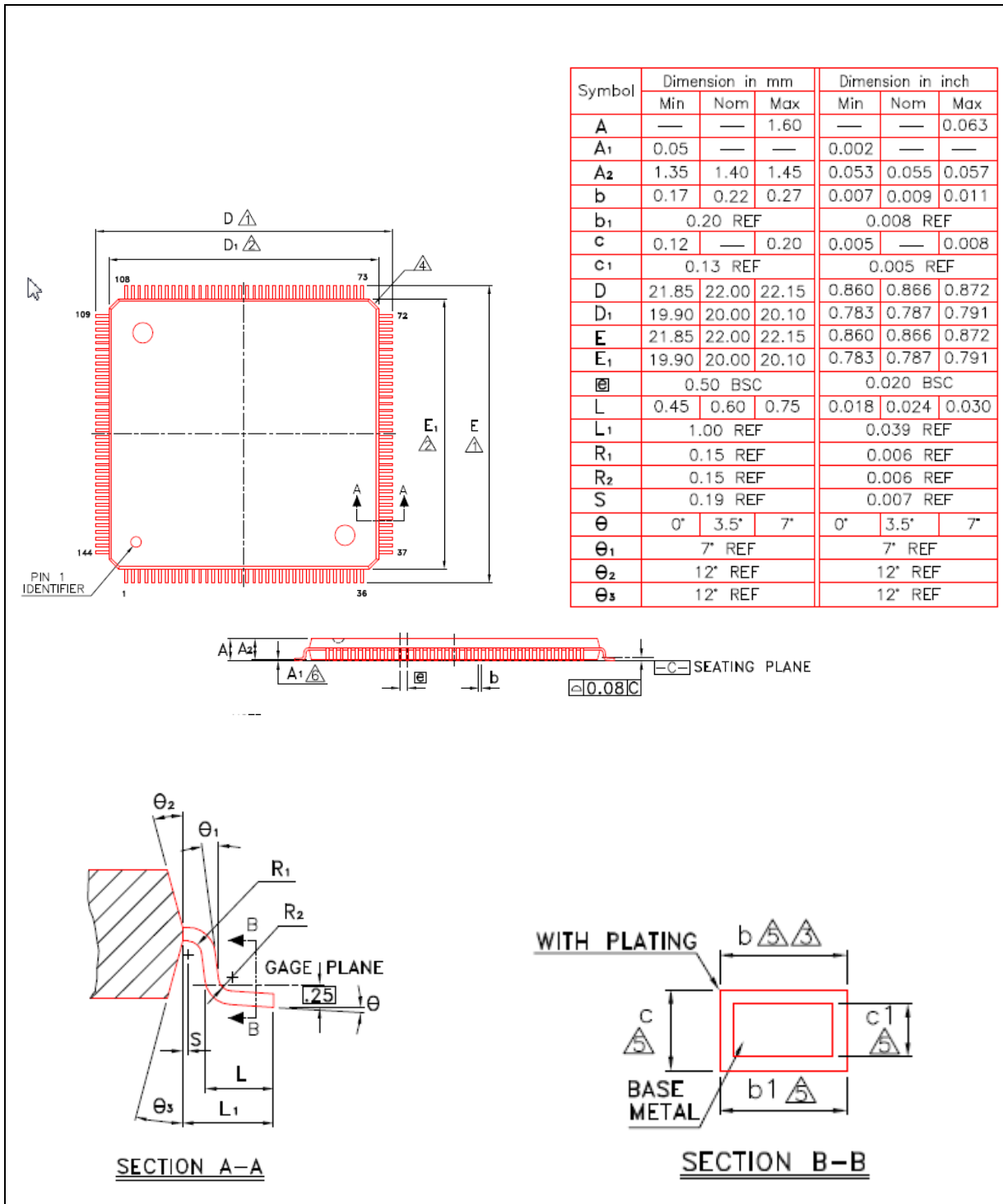
11.3 LQFP 64L (7x7x1.4 mm<sup>3</sup> footprint 2.0 mm)



11.4 LQFP 128L (14x14x1.4 mm<sup>3</sup> footprint 2.0 mm)



11.5 LQFP 144L (20x20x1.4 mm<sup>3</sup> footprint 2.0 mm)





12 REVISION HISTORY

| Date       | Revision | Description  |
|------------|----------|--|
| 2018.03.30 | 1.00     | 1. Preliminary version.  |
| 2018.07.16 | 1.01     | 1. Added the note “the SRAM bank2 has additional two wait cycles when reading data” in section 6.2.7.<br>2. Added the note that HXT should be 12 MHz for USB High-speed application in Figure 6-13.  |
| 2019.06.20 | 2.00     | 1. Added new M480 256 KB Flash product lines.<br>2. Added features comparison tables in FMC, BPWM, SDH, Crypto and EADC peripherals.<br>3. Added section 6.44 Peripherals Interconnection which allow autonomous communication or synchronous action between peripherals.  |
| 2019.08.20 | 2.01     | 1. Removed M48xGAAE parts information in Selection Guide.  |
| 2019.10.20 | 2.02     | 1. Added new M480 128 KB Flash product lines:<br>- M481 product line: M481ZE8AE, M481LE8AE and M481SE8AE<br>- M482 product line: M482ZE8AE, M482LE8AE and M482SE8AE<br>- M483 product line: M483SE8AE  |
| 2020.05.08 | 3.00     | 1. Added new part M487KMCAN.<br>2. Added notes about the hardware reference design for ICE_DAT, ICE_CLK and nRESET pins in section 4.2, 4.3 and chapter 7.<br>3. Fixed SPIx clock PCLK defined in Figure 6-13.<br>4. Added CCAP_SCLK and removed HSOTG clock in Figure 6-14.   |
| 2020.11.02 | 3.01     | 1. Added notes about the register HCLKDIV in Figure 6-14.<br>2. Added notes about external crystal HXT and LXT in Table 9.4-4 and Table 9.4-7.   |
| 2020.12.08 | 3.02     | 1. Added external crystal part number in Table 9.4-4 and Table 9.4-7 notes.  |
| 2022.02.22 | 3.03     | 1. Updated the Max. current of DPD mode in section 9.3.1.<br>2. Revised UART, TIMER and WDT clocks in Table 6.2-5.<br>3. Added Table 8.1-3 Thermal Characteristics.<br>4. Added Table 8.1-5 ESD Characteristics.<br>5. Added section 8.1.4.1 Electrostatic discharge (ESD).<br>6. Added section 8.1.4.2 Static latchup.<br>7. Added section 8.1.4.3 Electrical fast transients (EFT).<br>8. Added section 8.1.5 Package Moisture Sensitivity (MSL).<br>9. Added section 8.1.6 Soldering Profile.<br>10. Added InRush current in section 8.2. |
| 2022.05.04 | 3.04     | 1. Removed 1.62V featrue.<br>2. Added LQFP144 Thermal resistance junction-ambient in Table 8.1-3.<br>3. Added section 8.15 EBI Characteristics for M48XID/M487KMCAN.<br>4. Added section 9.6.7 EBI Characteristics for M48XGC/M48XE8.  |

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|            |      |   |
|------------|------|---|
| 2022.08.17 | 3.05 | <ol style="list-style-type: none"> <li>1. Removed SWDH pin name in section 4.2 and 4.3.</li> <li>2. Revised Standby Power-down mode current consumption in section 9.3.1.</li> <li>3. Revised PE.8, PE.9, PE.10, PE.11 and PE.12 MFP14 in section 4.2.</li> <li>4. Removed Flash access cycle auto-tuning function in section 6.5.</li> </ol> |
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### Important Notice

**Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, “Insecure Usage”.**

**Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.**

**All Insecure Usage shall be made at customer’s risk, and in the event that third parties lay claims to Nuvoton as a result of customer’s Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.**

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