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Flaircomm Technologies Inc.

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Datasheet

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1. Introduction

FLC-BTM801 is a dual-mode Bluetooth HCI module that allows OEM to add Bluetooth wireless capability to their products. The module supports BT3.0-HS and BT4.0 (Bluetooth low energy) with HCI interface that makes it simple to design into fully certified embedded Bluetooth solutions. This module is designed for automotive applications.

With FLC's Bluetooth stack running on a host, designers can easily customize their applications to support different Bluetooth profiles, such HS/HF, A2DP, AVRCP, OPP, DUN, SPP, and etc. The module supports Bluetooth® Enhanced Data Rate (EDR) and delivers up to 3 Mbps data rate.

1.1 Naming Declaration

New Naming	Old Naming
FLC-BTM801	NA

Table 1: Naming Declaration

1.2 Block Diagram

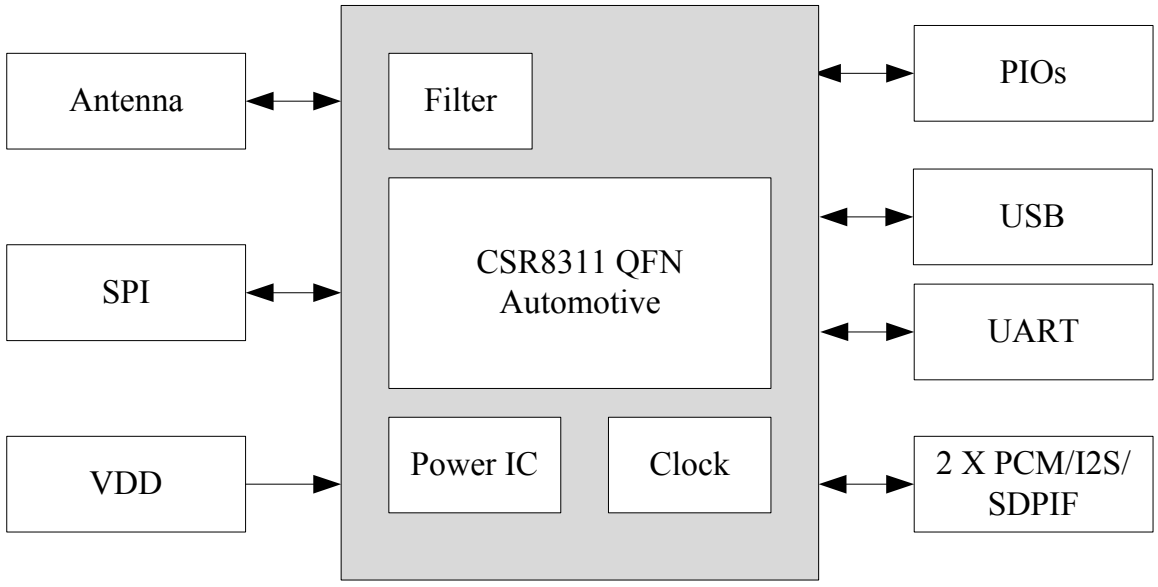


Figure 1: Block Diagram

1.3 Features

- Bluetooth v2.1+EDR, Class 1.5

- Bluetooth V3.0-HS, Class 1.5
- Bluetooth V4.0 low energy connections
- 7dBm RF transmit power with level control
- -89dBm π/4 DQPSK sensitivity
  - ✧ Integrated channel filters
  - ✧ Digital demodulator for improved sensitivity and co-channel rejection
  - ✧ Fas AGC for enhanced dynamic range
  - ✧ Channel classification for AFH
  - ✧ 2Mbps and 3Mbps EDR support
- UART or USB programming and data interface
  - ✧ Fill-speed (12Mbps) USB 2.0 interface
  - ✧ Synchronous serial interface up to 4Mbps for system debugging
  - ✧ UART interface with programmable baud rate up to 4Mbps
- Two PCM/I2S digital audio interface
- Baseband and Software
  - ✧ Internal RAM enables full speed data transfer, mixed voice and data, and full piconet operation, including all medium rate packet types
  - ✧ Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping. Includes support for eSCO and AFH
  - ✧ Transcoders for A-Law, μ-Law and linear voice from host and A-law, μ-law and CVSD voice over air.
- Module with Bluetooth Protocol Stack runs up to HCI on the on-chip CPU
- Small form factor
- SMT pads for easy and reliable PCB mounting
- BQB/FCC/CE Certified
- RoHS compliant

1.4 Applications

- Automotive

2. General Specification

Bluetooth Specification	
Standard	BT2.1+EDR, BT 3.0-HS, BT4.0 BLE, Class 1.5
Frequency Band	2.402G ~ 2.480G
Maximum Data Rate	3Mbps
RF Input Impedance	50 ohms
Baseband TCXO	26MHz
Interface	UART, USB, PIO, SPI, PCM/I2S/SPDIF
Sensitivity	-89dBm@0.1%BER
RF TX Power	7dBm
Power	
Supply Voltage	2.3 ~ 4.8V DC
Working Current	Refer to 错误！未找到引用源。
Standby Current	10uA in deep sleep mode
Operating Environment	
Temperature	-40ºC to +85ºC
Humidity	10%~90% Non-Condensing
Certifications	BQB/FCC/CE
Environmental	RoHS Compliant
Dimension and Weight	
Dimension	23.24mm x 11.94mm x 2.50mm
Weight	TBD

Table 2: General Specification

3. Pin Definition

3.1 Pin Configuration

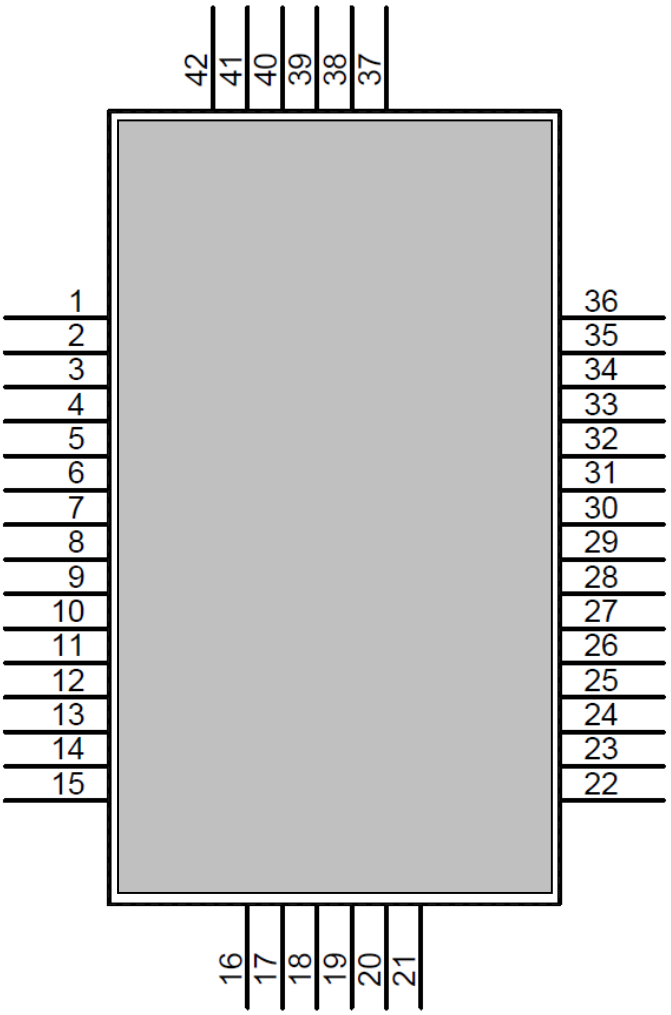


Figure 2: Pin Configuration

3.2 Pin Definition

Pin	Symbol	I/O Type	Description
1	GND	Ground	Ground
2	RESETB	CMOS input with weak internal pull-up	Active low
3	SPI_CLK / PCM1_CLK	Input with weak internal pull-down	Serial Peripheral Interface clock / Synchronous data clock

4	SPI_MISO / PCM1_OUT	Output, tri-state, with weak internal pull-down	Serial Peripheral Interface output / Synchronous data output
5	SPI_MOSI / PCM1_IN	Input with weak internal pull-down	Serial Peripheral Interface input / Synchronous data input
6	SPI_CSB / PCM1_Sync	Input with weak internal pull-up	Chip select for Synchronous Serial Interface active low / Synchronous data sync
7	NC	Not connected	Not connected
8	PIO5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
9	PIO4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
10	PIO3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
11	PIO2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
12	PIO0	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
13	PIO1	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
14	NC	Not connected	Not connected
15	GND	Ground	Ground
16	NC	Not connected	Not connected
17	RF_GND	RF Ground	RF Ground
18	RF_IN	Analogue	Radio transceiver input/output line
19	RF_GND	RF Ground	RF Ground
20	NC	Not connected.	Not connected
21	NC	Not connected.	Not connected
22	GND	Ground	Ground
23	NC	Not connected.	Not connected
24	NC	Not connected.	Not connected
25	NC	Not connected.	Not connected
26	NC	Not connected.	Not connected
27	SPI_PCM#_SEL	Input with internal pull down	SPI / PCM selection High – SPI is selected Low – PCM1 is selected
28	VBUS	Power Input	Input voltage 4.2V to 5.75V. It can be power with USB power. If this power supply is used, port VDD is for decoupling only. A low ESR MLC capacitor from 1μF to 4.7μF should be connected to pin 30 (VDD). If the high voltage is not used, leave this pin unconnected.
29	USB_UART#_SEL	Input with internal pull down	USB / UART selection High – USB is selected

			Low – UART is selected
30	VDD	Power input	If VBUS is used, this pin is for decoupling only. A low ESR MLC capacitor from 1μF to 4.7μF should be connected. If VBUS is not used, this pin is 3.3v power input.
31	DP	Bi-directional	USB data
32	DN	Bi-directional	USB data
33	PCM2_CLK	Bi-directional with weak internal pull down	Synchronous data clock
34	PCM2_OUT	Output, tri-state, with weak internal pull-down	Synchronous data output
35	PCM2_IN	Input with weak internal pull-down	Synchronous data input
36	PCM2_SYNC	Bi-directional with weak internal pull-down	Synchronous data sync
37	GND	Ground	Ground
38	UART_TX	Bi-directional with programmable strength internal pull-up/down	UART data output
39	UART_RX	Bi-directional with programmable strength internal pull-up/down	UART data input
40	UART_CTS	Bi-directional with programmable strength internal pull-up/down	UART flow control
41	NC	Not connected.	Not connected
42	UART_RTS	Bi-directional with programmable strength internal pull-up/down	UART flow control

Table 3: Pin Definition

4. Physical Interfaces

4.1 Power Supply

There are two options for the power supply.

1. USB power, from 4.2V to 5.75V, can be directly used to power this module. If this power supply is used, port VDD (pin30) is for decoupling only. A low ESR MLC capacitor from 1µF to 4.7µF should be connected to pin 30 (VDD). If the high voltage is not used, leave pin 28 unconnected.
2. If the high voltage is not used, a 3.3V voltage has to apply to pin 30. In this case, leave pin 28 unconnected.

4.2 Reset

The module may be reset from several sources: RESETB pin, power-on reset, a UART break character or via a software configured watchdog timer.

The RESETB pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active. It is recommended that RESETB be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-downs.

Pin Name / Group	I/O Type	No Core Voltage Reset	Full Chip Reset
RST#	Digital input	Strong pull-down	N/A
SPI_CLK / PCM_CLK / PIO[24]	Digital bidirectional tristated	Weak pull-down	Weak pull-down
SPI_CS# / PCM_SYNC / PIO[23]	Digital bidirectional tristated	Weak pull-up (SPI) Weak pull-down (PCM)	Weak pull-up (SPI) Weak pull-down (PCM / PIO)
SPI_MISO / PCM_OUT / PIO[22]	Digital output tristated	Weak pull-down	Weak pull-down
SPI_MOSI / PCM_IN / PIO[21]	Digital input	Weak pull-down	Weak pull-down
PIO[5:0]	Digital bidirectional tristated	Weak pull-down	Weak pull-down

Table 4: Pin Status on Reset

Note: Pull-up (PU) and pull-down (PD) default to weak values unless specified otherwise.

4.3 Audio Interfaces

4.3.1 Audio Interface Overview

BTM801 module provides 2 independent audio interfaces which can be configured independent as PCM interface or as Digital audio interface (I^2C).

PCM2 has dedicated pins, whereas PCN1 pins are multiplexed with SPI and PIO lines. The information in this section applies to both PCM interface.

Each interface has its own set of PS keys.

4.3.2 PCM Interface

The audio PCM interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth. By default the audio data are multiplexed in UART transport. Contact Flaircomm for special driver to route the audio data to PCM.

PCM is a standard method used to digitize audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, the module has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for applications. The module offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on the module allows the data to be sent to and received from a SCO connection. Up to three SCO connections can be supported by the PCM interface at any one time.

The module can operate as the PCM interface master generating an output clock of 128, 256, 512, 1536 or 2400kHz. When configured as PCM interface slave, it can operate with an input clock up to 2400kHz. The module is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8k samples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC.

The module interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channels A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- The module is also compatible with the Motorola SSI Interface

4.3.3 PCM Interface Master/Slave

When configured as the master of the PCM interface, the module generates PCM_CLK and PCM_SYNC.

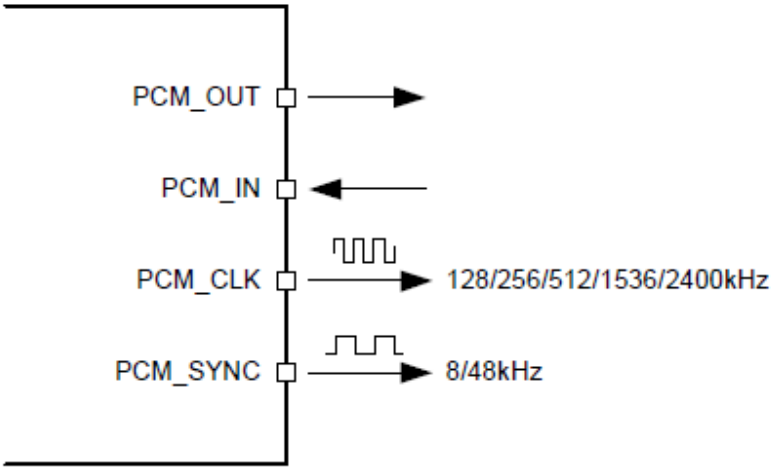


Figure 3: Configured PCM as a Master

When PCM is configured as the slave, the module accepts PCM_CLK rates up to 2400kHz.

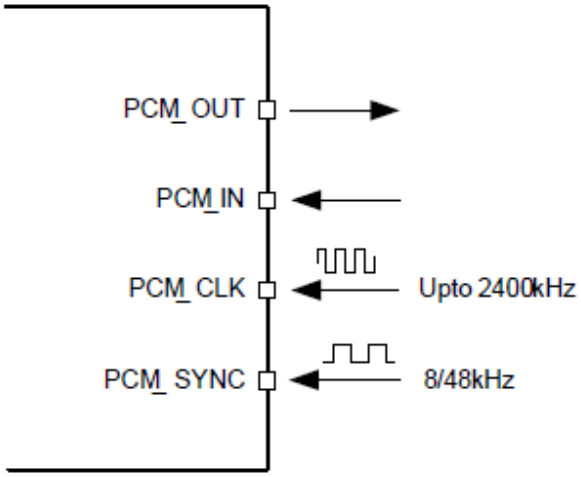


Figure 4: Configured PCM as a Slave

4.3.4 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When the module is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When the module is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e., 62.5µs long.

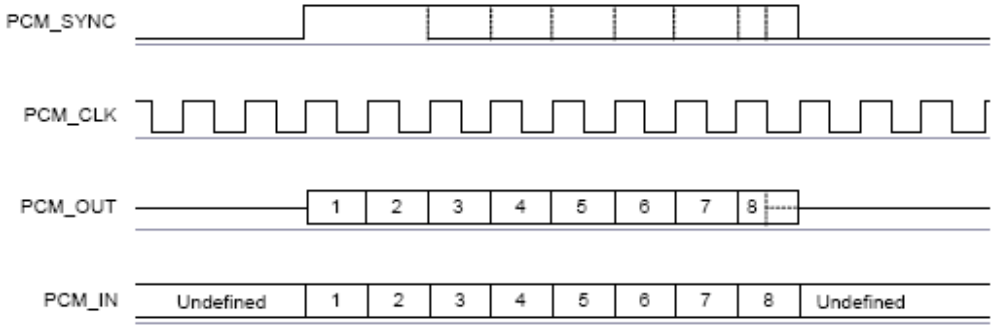


Figure 5: Long Frame Sync (Shown with 8-bit Companded Sample)

The module samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

4.3.5 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

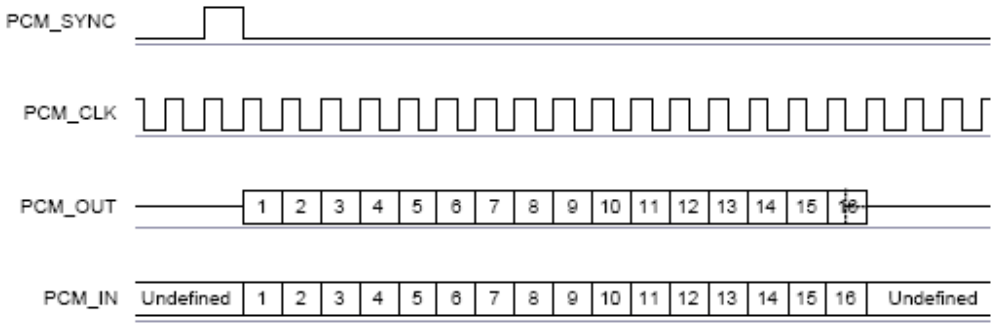


Figure 6: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, the module samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

4.3.6 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

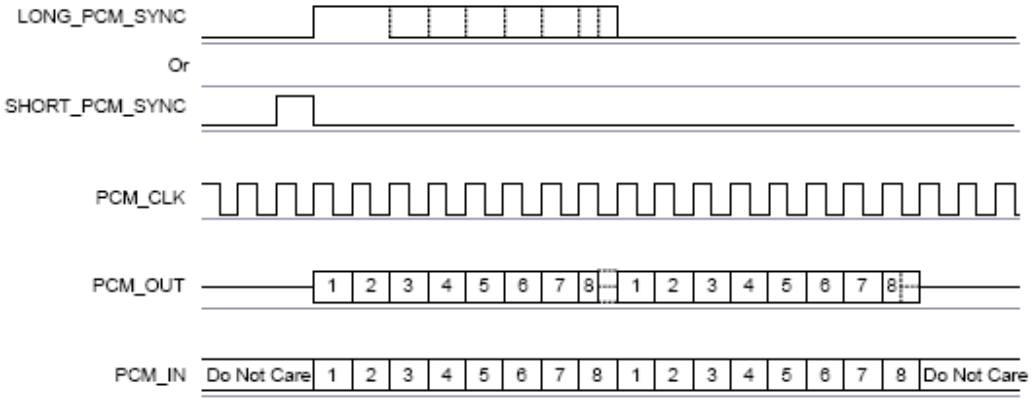


Figure 7: Multi-Slot Operation with Two Slots and 8-bit Companded Samples

4.3.7 GCI Interface

The module is compatible with the General Circuit Interface (GCI), a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

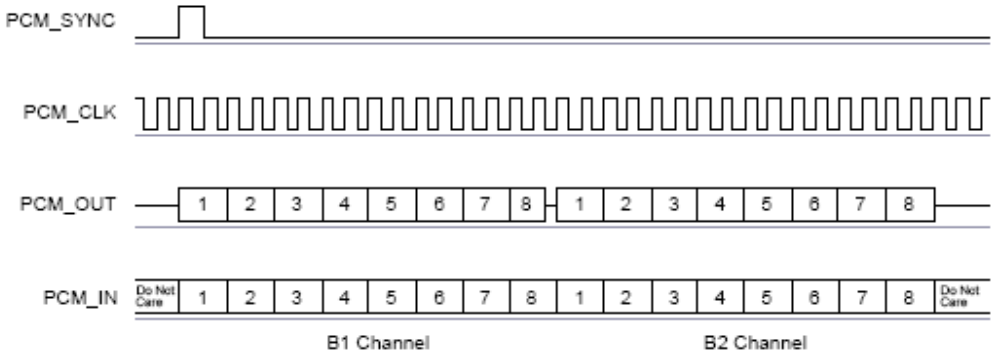


Figure 8: GCI Interface

The start of a frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With the module in slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

4.3.8 Slots and Sample Formats

The module can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats. The module supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8k samples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

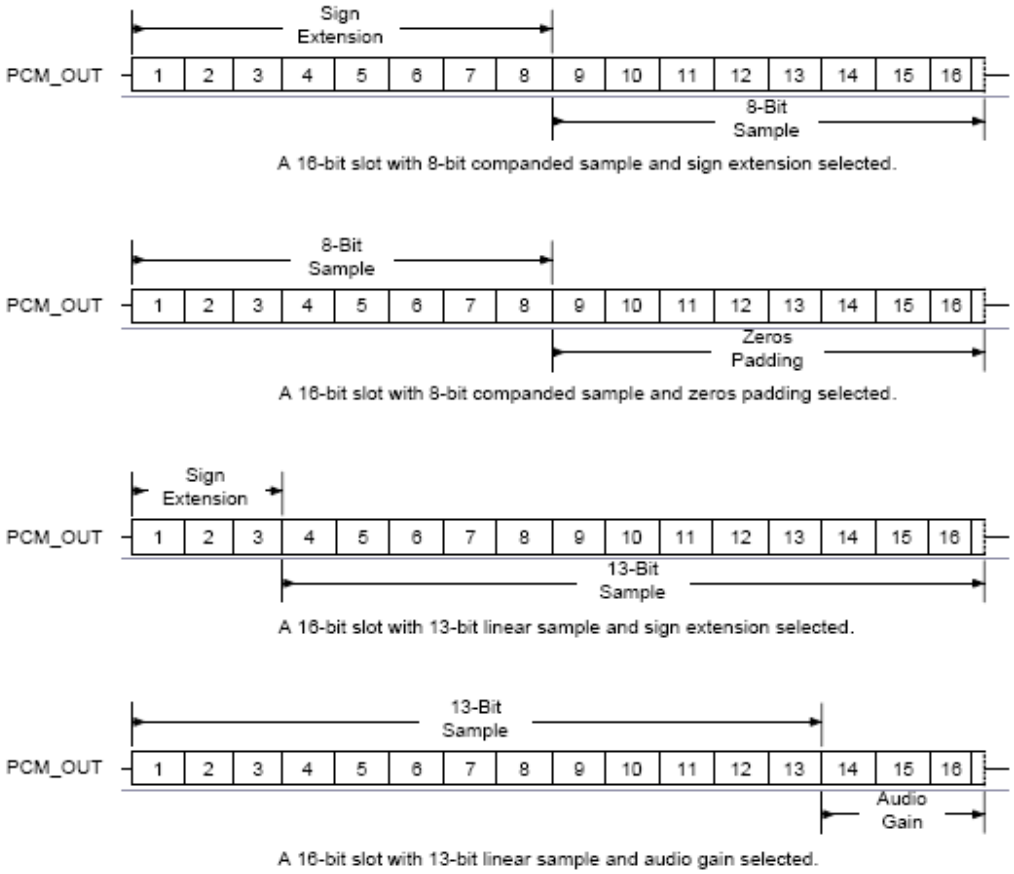


Figure 9: 16-Bit Slot Length and Sample Formats

4.3.9 Additional Features

The module has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

4.3.10 PCM Timing Information

Symbol	Parameter		Min	Typical	Max	Unit
f_{mclk}	PCL_CLK Frequency	4MHz DDS generation. Selection of frequency is programmable.	-	128	-	kHz
				256		
				512		

		48MHz DDS generation. Selection of frequency is programmable.	2.9		-	kHz
-	PCM_SYNC frequency		-	8		kHz
t_{mclkh} (a)	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} (a)	PCM_CLK low	4MHz DDS generation	730	-		ns
-	PCM_CLK jitter	48MHz DDS generation			21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 5: PCM Master Timing

(a) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

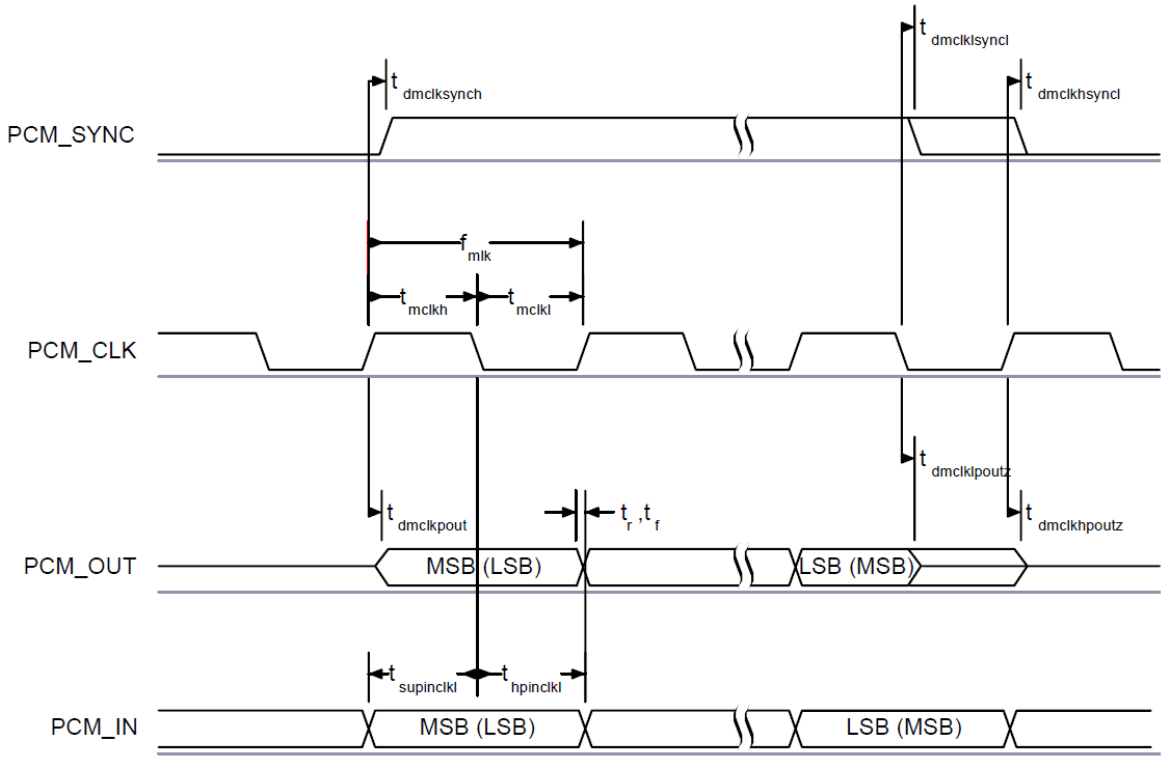


Figure 10: PCM Master Timing Long Frame Sync

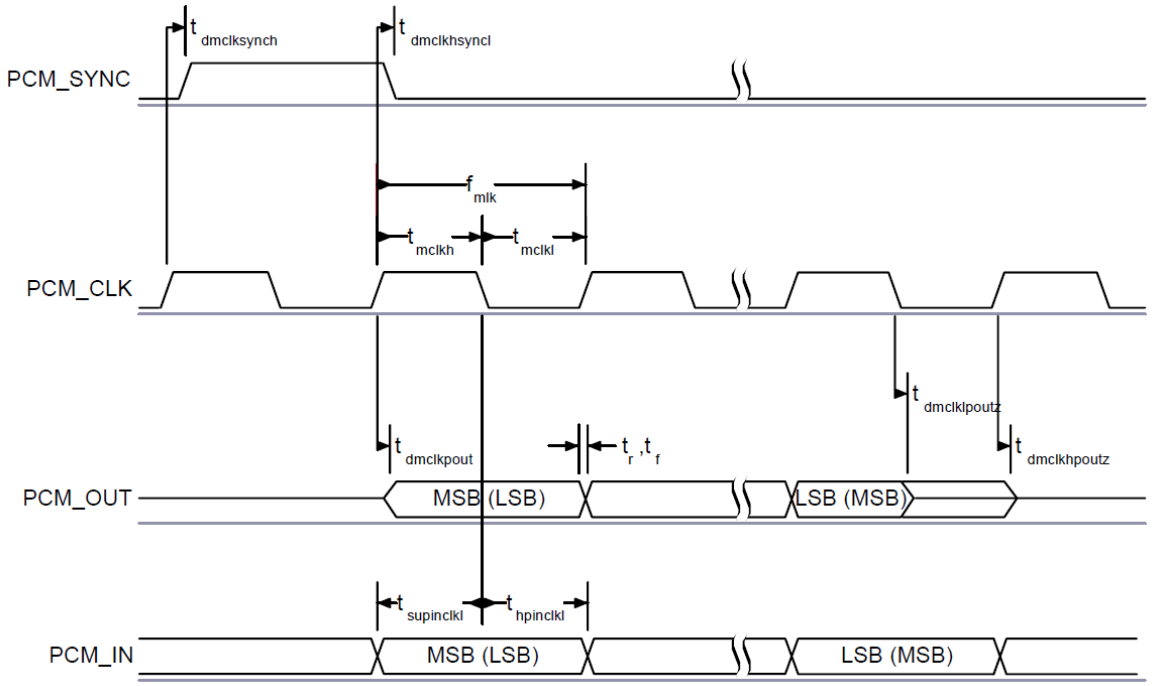


Figure 11: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typical	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns

Table 6: PCM Slave Timing

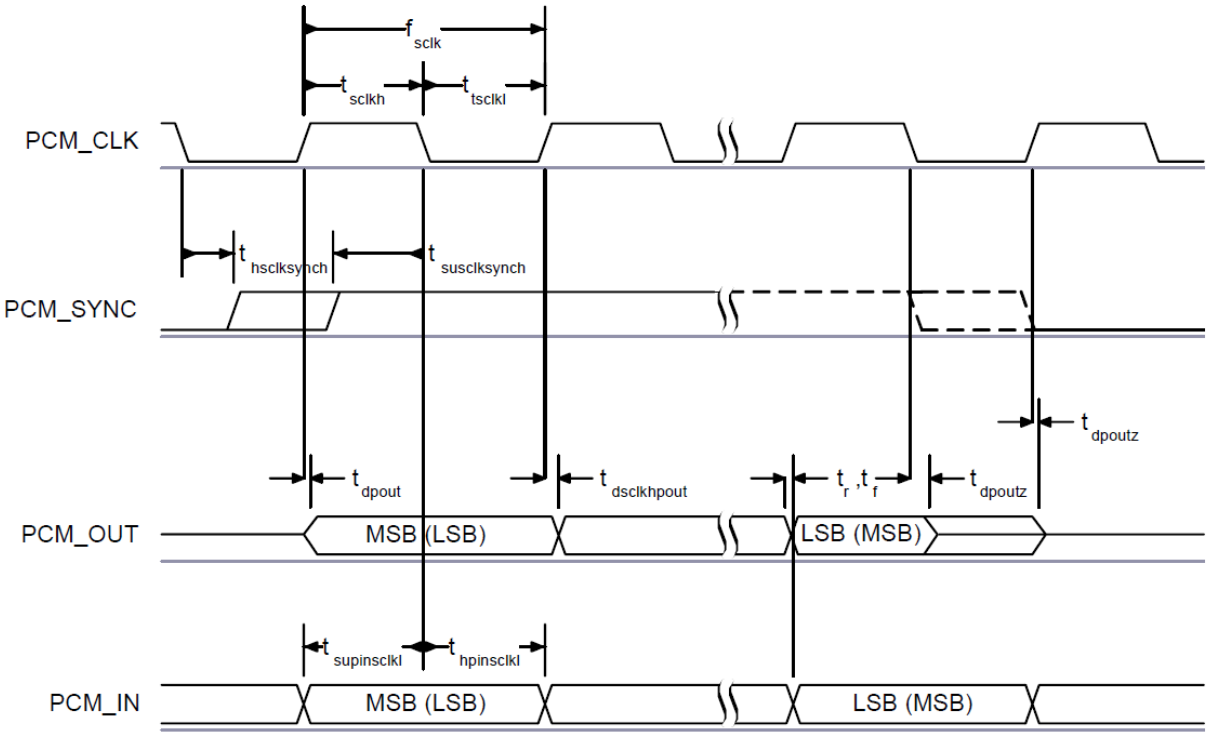


Figure 12: PCM Slave Timing Long Frame Sync

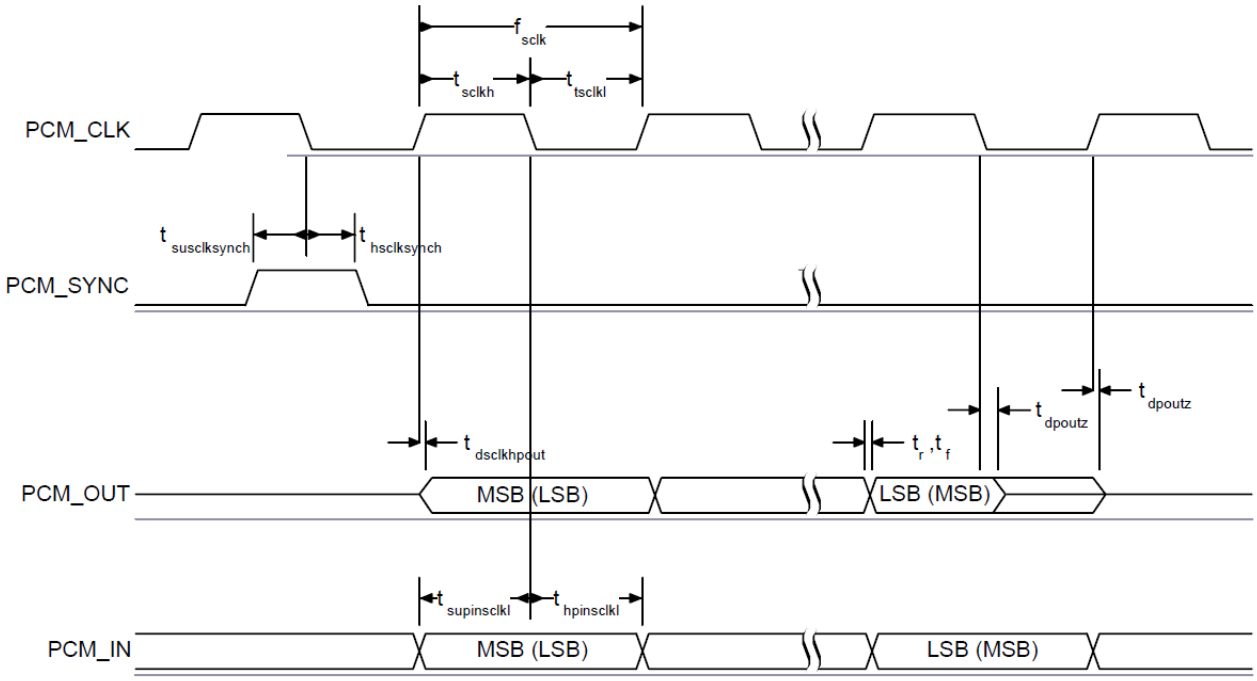


Figure 13: PCM Slave Timing Short Frame Sync

4.4 Digital Audio Interface (I^2S)

The digital audio interface supports the industry standard formats for I^2S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage.

PCM Interface	I^2S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 7: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

Special driver is needed if I^2S is designed. Contact Flaircomm for the special driver when use I^2S as the interface between the module and the host or the codec.

Figure 14 shows the timing diagram.

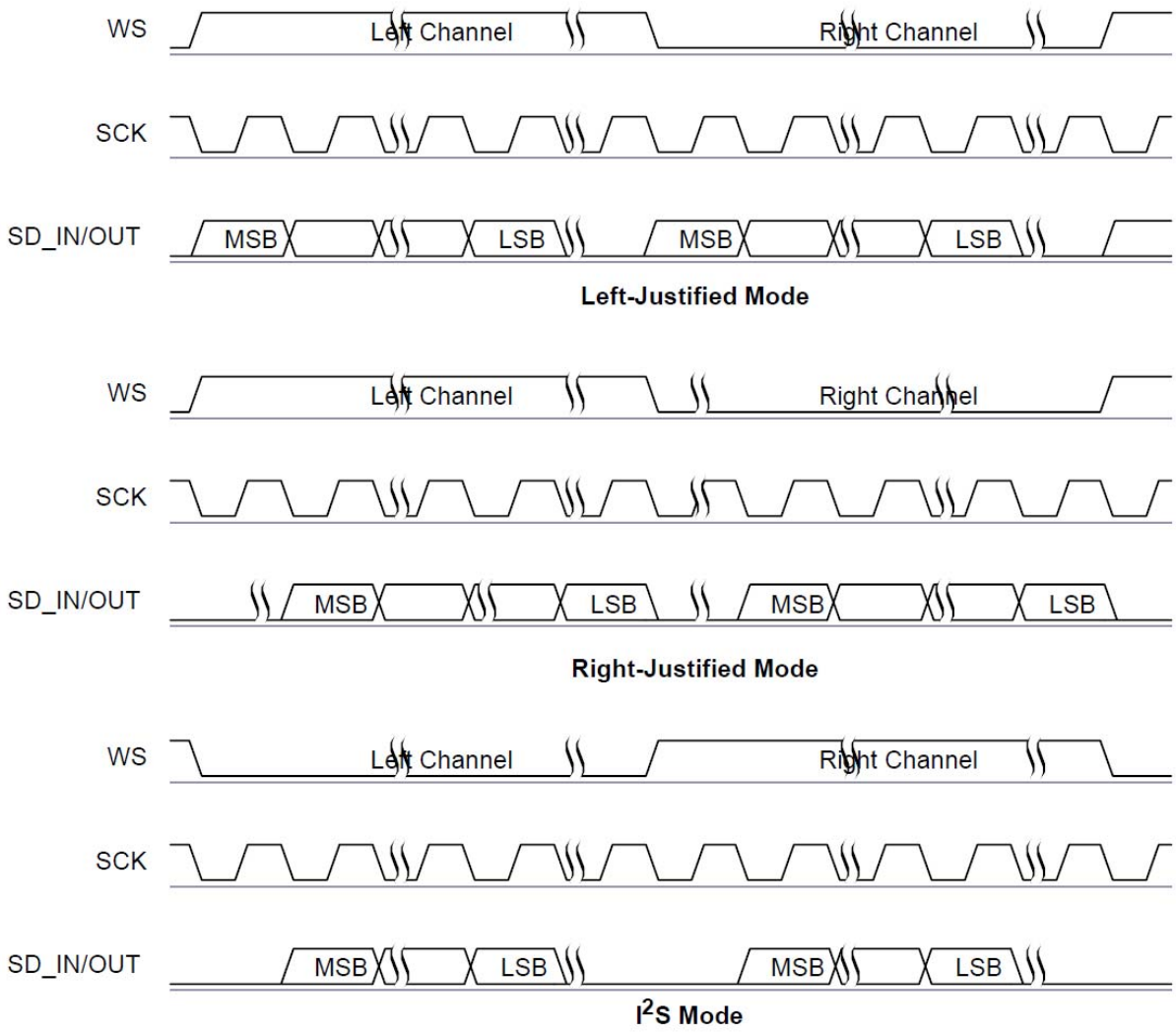


Figure 14: Digital Audio Interface Modes

The internal representation of audio samples is 16-bit and data on SD_OUT is limited to 16-bit per channel.

Symbol	Parameter	Min	Typical	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{ssu}	WS to SCK set up time	20	-	-	ns
t_{sh}	WS to SCK hold time	20	-	-	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	20	-	-	ns

Table 8: Digital Audio Interface Slave Timing

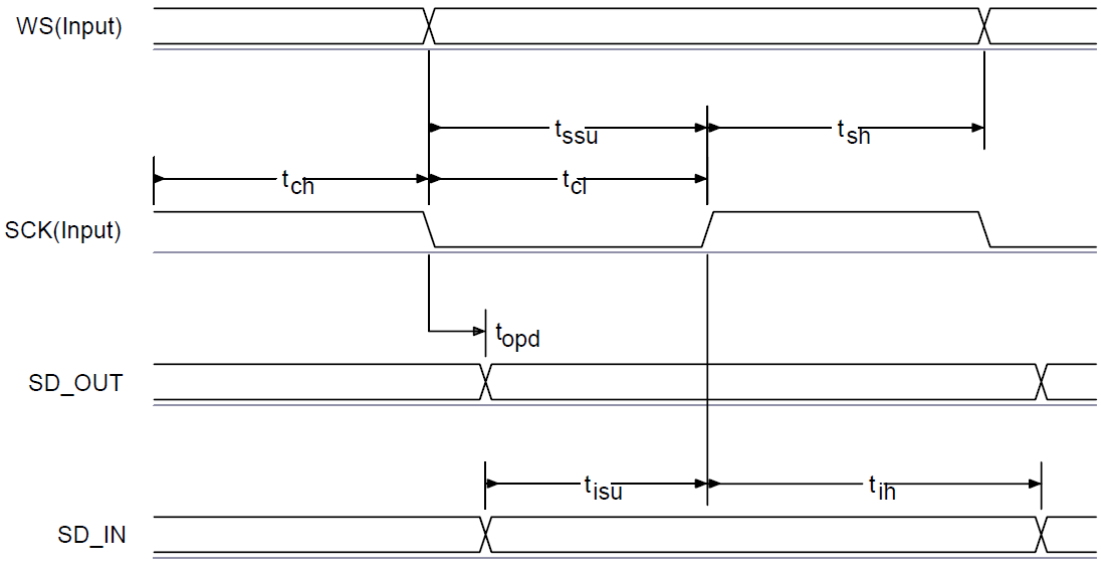


Figure 15: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typical	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{spd}	SCK to WS delay	-	-	20	ns
t_{sh}	WS to SCK hold time	20	-	-	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	10	-	-	ns

Table 9: Digital Audio Interface Master Timing

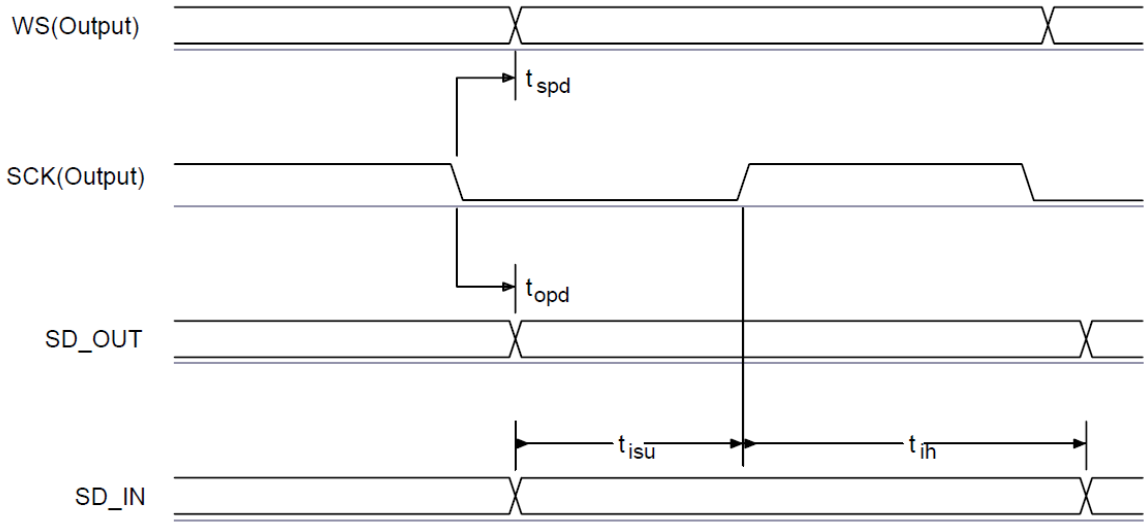


Figure 16: Digital Audio Interface Master Timing

4.5 RF Interface

The module integrates a balun filter. The user can connect a 50ohms antenna directly to the RF port.

4.6 General Purpose Digital IO

There are nine general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED displays or interrupt signals to host controller, etc. Do not connect them if not use.

4.7 Host Interfaces

4.7.1 UART Interface

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices.

Parameter		Possible Values
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4M baud (≤1%Error)
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Byte		8

Table 10: Possible UART Settings

4.7.2 USB Interface

BTM801 has a full-speed (12Mbps) USB interface for communication with other compatible digital devices. The USB interface on BTM801 acts as a USB peripheral, responding to requests from a master host controller.

BTM801 supports the *Universal Serial Bus Specification, Revision v2.0 and USB Battery Charging Specification,* available from http://www.usb.org.

4.7.3 SPI

The synchronous serial port interface (SPI) can be used for system debugging. SPI interface uses the SPI_MOSI, SPI_MISO, SPI_CSB and SPI_CLK pins.

The module operates as a slave and thus SPI_MISO is an output of the module. SPI_MISO is not in high-impedance state when SPI_CSB is pulled high. Instead, the module outputs 0 if the processor is running and 1 if it is stopped. Thus the module should NOT be connected in a multi-slave arrangement by simple parallel connection of slave SPI_MISO lines.

5. Electrical Characteristic

5.1 Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+120	°C
Operating Temperature	-40	+85	°C
PIO Voltage	-0.4	+3.6	V
VDD Voltage	-0.4	+3.6	V
VBUS Voltage	-0.4	+5.75	V
Other Terminal Voltages except RF	-0.4	+3.7	V

Table 11: Absolute Maximum Rating

5.2 Recommended Operating Conditions

Operating Condition	Min	Typical	Max	Unit
Storage Temperature	-40	--	+85	°C
Operating Temperature Range	-40	--	+85	°C
PIO Voltage	+2.7	+3.3	+3.6	V
VDD Voltage	+2.3	+3.3	+3.6	V
VBUS Voltage	+4.2	+3.3	+5.75	V

Table 12: Recommended Operating Conditions

5.3 Input/output Terminal Characteristics

5.3.1 Digital Terminals

Supply Voltage Levels	Min	Typical	Max	Unit
Input Voltage Levels				
VIL input logic level low	-0.4	-	+0.4	V
VIH input logic level high	0.7VDD	-	VDD+0.4	V
T_r/T_f			25	ns
Output Voltage Levels				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.4	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75VDD	-	-	V
T_r/T_f			5	ns
Input and Tri-state Current				
With strong pull-up	-150	-40	-10	µA

With strong pull-down	10	40	150	µA
With weak pull-up	-5	-1.0	-0.33	µA
With weak pull-down	0.33	1.0	5.0	µA
I/O pad leakage current	-1	0	+1	µA
CI Input Capacitance	1.0	-	5.0	pF

Table 13: Digital Terminal

6. Reference Design

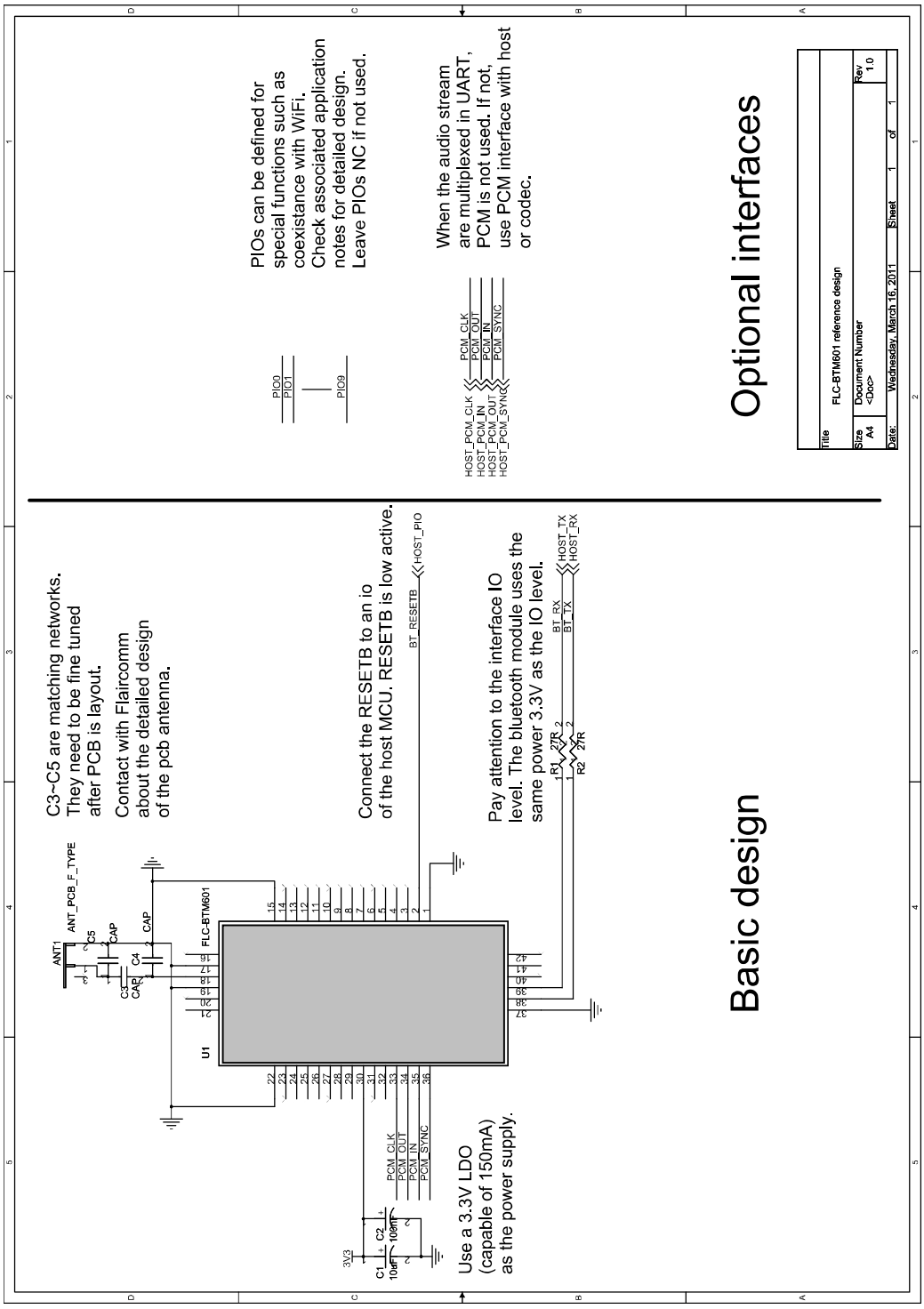
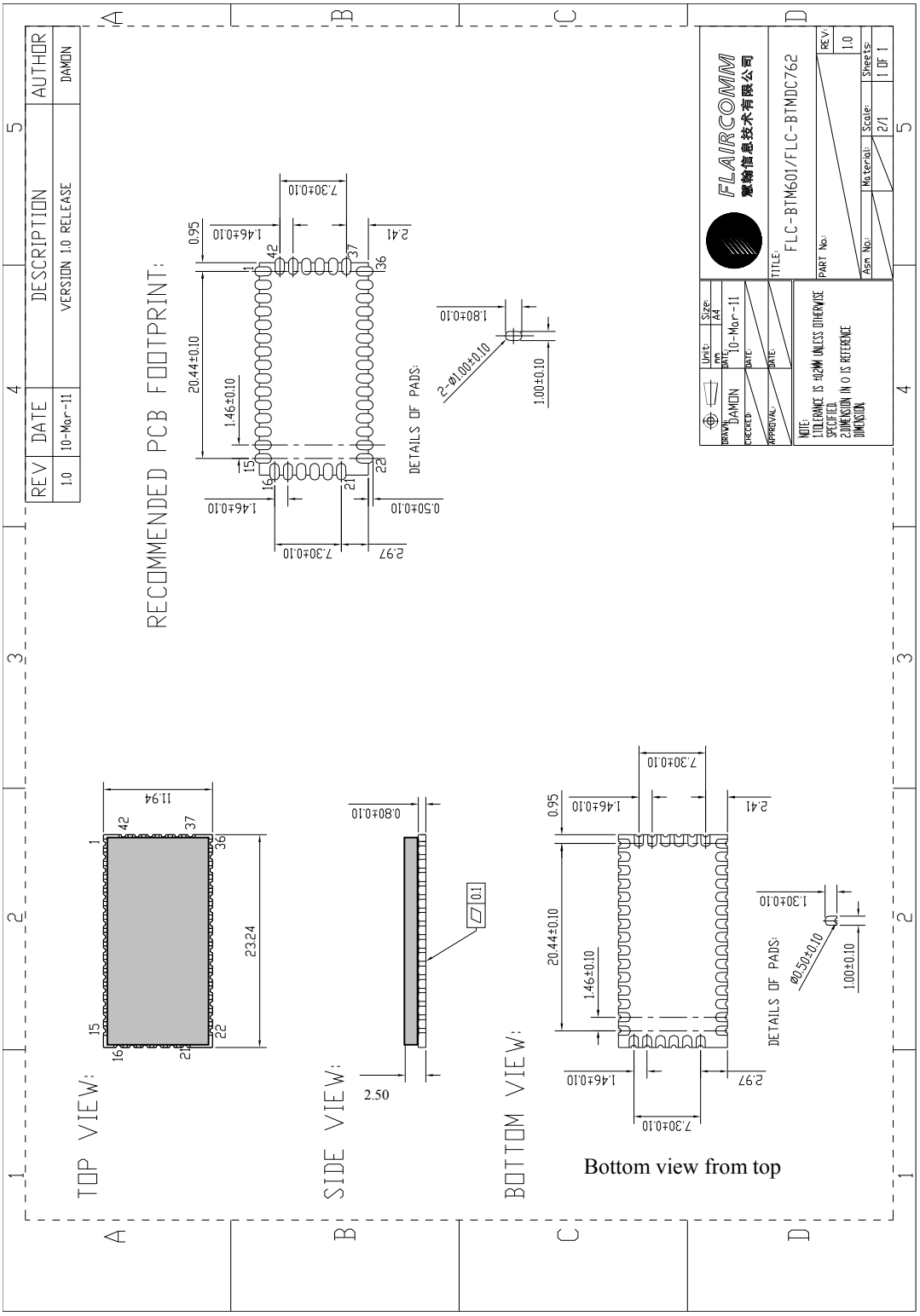


Figure 17: Reference Design

7. Mechanical Characteristic



Bottom view from top

Figure 18: Mechanical Characteristic

8. Recommended PCB Layout and Mounting Pattern

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in **Figure 19**. below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

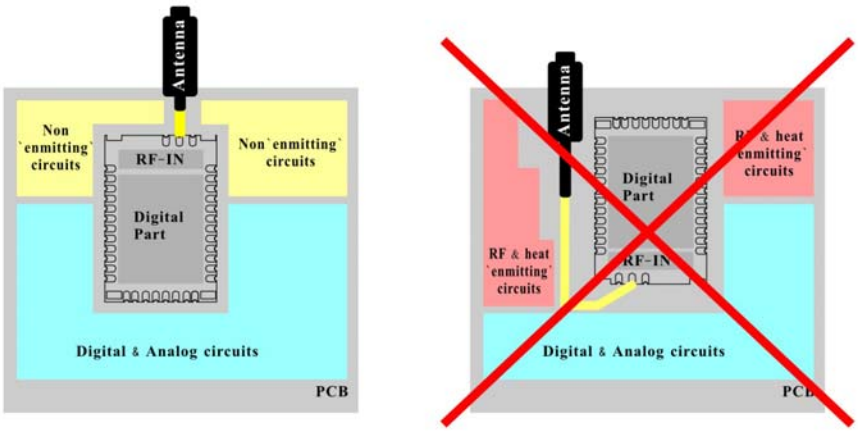


Figure 19: Placement the Module on a System Board

8.1 Antenna Connection and Grounding Plane Design

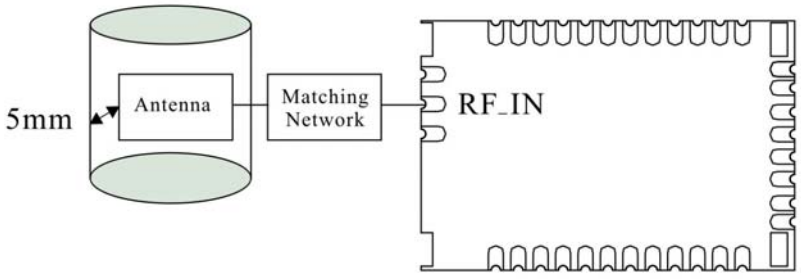


Figure 20: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.

- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

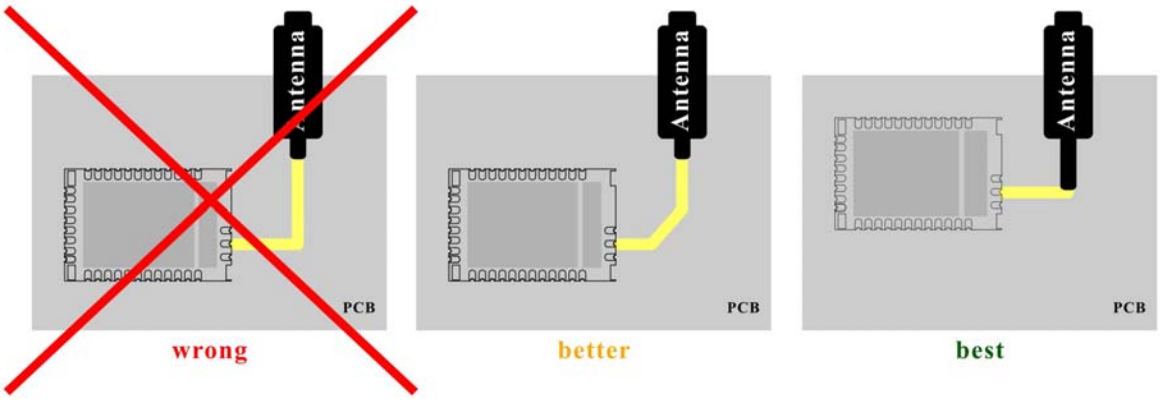


Figure 21: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

9. Recommended Reflow Profile

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

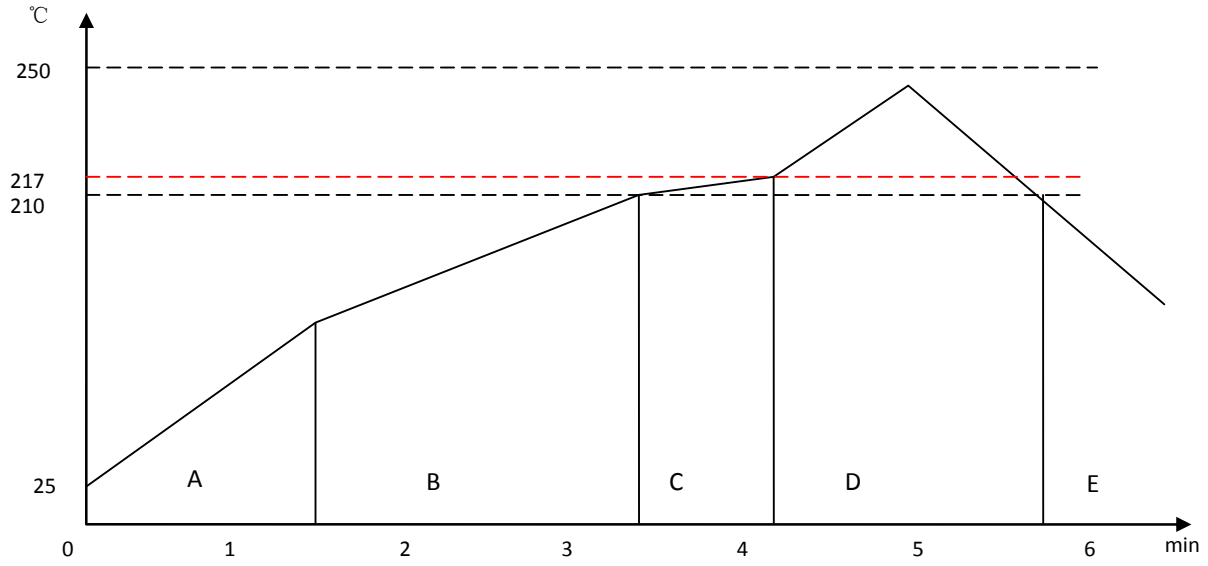


Figure 22: Recommended Reflow Profile

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone**.

Equilibrium Zone 2 (c) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longerlasting joint. **Typical cooling rate should be 4 °C**.

10. Ordering Information

10.1 Product Packaging Information

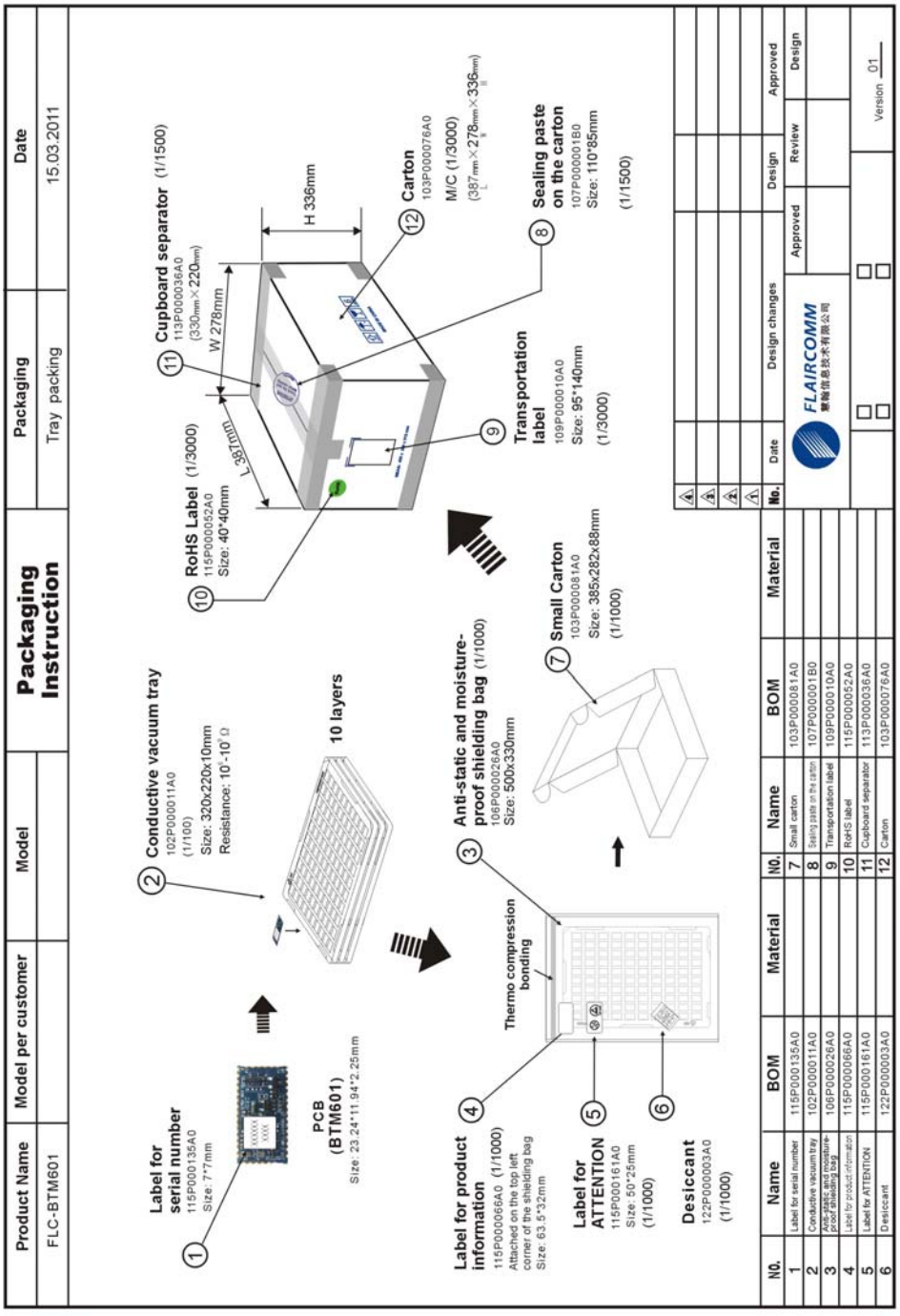


Figure 23: Product Packaging Information

10.2 Ordering information

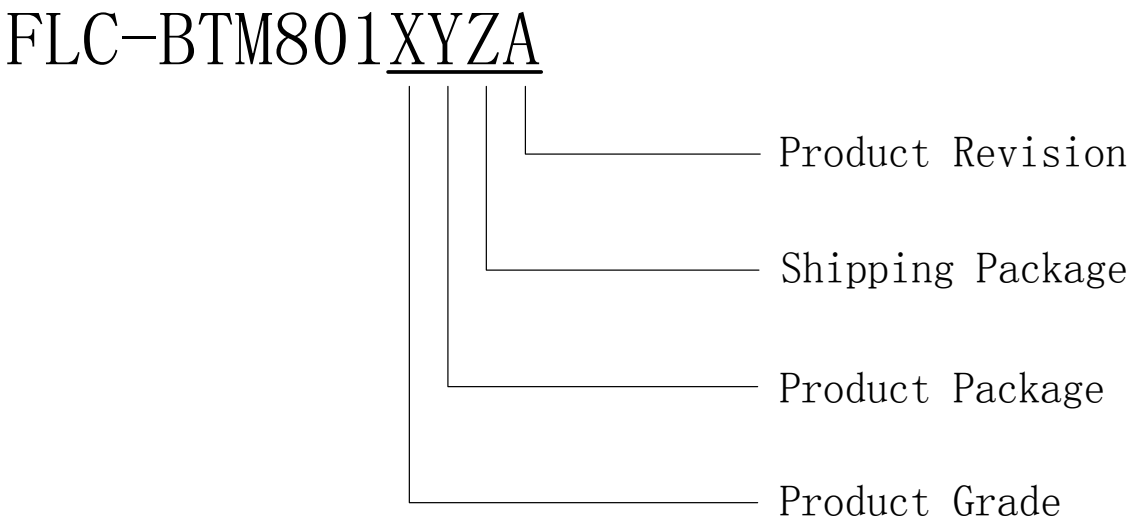


Figure 24: Ordering Information

10.2.1 Product Revision

Product Revision	Description	Availability
A	Release A	Yes

Table 14: Product Revision

10.2.2 Shipping Package

Shipping Package	Description	Quantity	Availability
0	Foam Tray	—	No
1	Plastic Tray	100x10x3 = 3000	Yes
2	Tape	—	Yes

Table 15: Shipping Package

10.2.3 Product Package

Product Package	Description	Availability
Q	QFN	Yes
L	LGA	No
B	BGA	No
C	Connector	No

Table 16: Product Package

10.2.4 Product Grade

Product Grade	Description	Availability
C	Consumer	Yes

I	Industrial	Yes
V	Automobile After-Market	Yes
A	Automobile Before-Market	Yes

Table 17: Product Grade