FLAIRCOMM

Flaircomm Technologies Inc.

FLC-BTM501/FLC-BTMDC751
Datasheet

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Release Record

Version	Release Date	Comments
1.0	March 18, 2011	Release
1.1	July 15,2011	Modified Table 1 and Table 16.
1.2	May 16,2012	Modified Table 2.

CONTENT

TABLE AND FIGURE

1. Introduction

FLC-BTM501 is a small form factor, low power and highly economic Bluetooth radio module that allows OEM to add wireless capability to their products. The module supports multiple interfaces that make it simple to design into fully certified embedded Bluetooth solutions.

With FLC's AT+™ programming interfaces, designers can easily customize their applications to support different Bluetooth profiles, such HS/HF, A2DP, AVRCP, OPP, DUN, SPP, and etc. The module supports Bluetooth® Enhanced Data Rate (EDR) and delivers up to 3 Mbps data rate for distances to 10M.

The module is an appropriate product for designers who want to add wireless capability to their products.

1.1 Naming Declaration

New Naming	Old Naming	Description
FLC-BTM501XXXA	FLC-BTMDC751	Built-in 16M flash memory.
FLC-BTM501XXXB	FLC-BTMDC751S	Built-in 8M flash memory.
FLC-BTM501XXXD	FLC-BTMDC751MV	Built-in 16M flash memory. HTG.
	FLC-BTMDC8501BM	
FLC-BTM501XXXE	FLC-BTMDC8501AS	Built-in 8M flash memory. Halogen-Free.

Table 1: Naming Declaration

1.2 Block Diagram

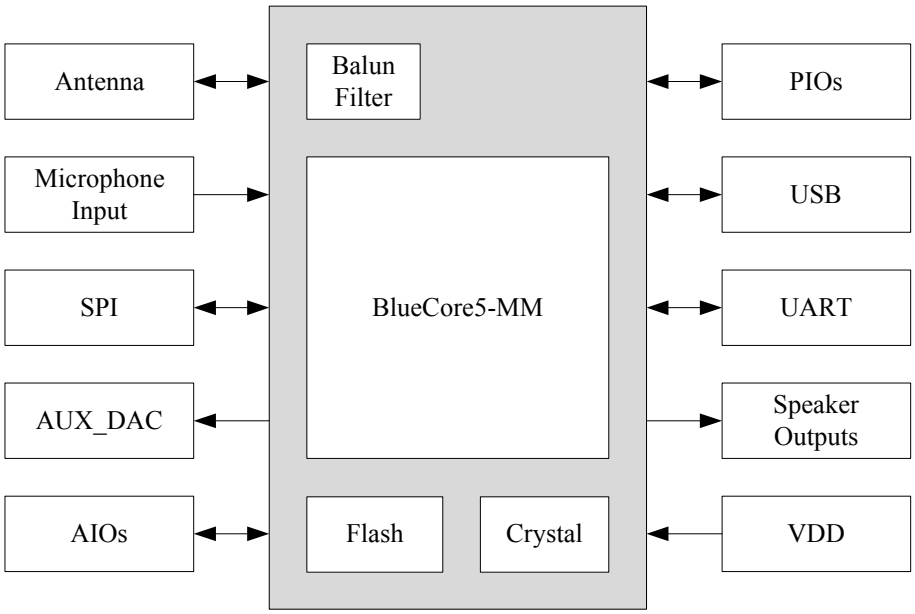

Figure 1: Block Diagram

1.3 Features

- Bluetooth v2.1+EDR, Class 2
- Profiles including HS/HF, A2DP, AVRCP, OPP, DUN, SPP, and etc.
- UART and USB programming and data interfaces
- Small form factor
- SMT pads for easy and reliable PCB mounting
- BQB/FCC/CE Certified
- RoHS compliant

1.4 Applications

- Automobile hands-free applications
- Stereo headset applications
- Cable replacements
- Bar code and RFID scanners
- Measurement and monitoring systems

- Industrial sensors and controls
- Medical devices
- Industrial PCs and laptops

2. General Specification

Bluetooth Specification	
Standard	Bluetooth2.1+EDR, Class II
Profiles	HS/HF, A2DP, AVRCP, OPP, DUN, SPP, etc. detailed profiles depends on the firmware
Frequency Band	2.402GHz ~ 2.480GHz
Maximum Data Rate	3Mbps
RF Input Impedance	50 ohms
Baseband Crystal OSC	16MHz
Interface	UART, PIO, AIO, USB, SPI, Speaker, Microphone, etc.
Sensitivity	-86dBm@0.1%BER
RF TX Power	4dBm
Power	
Supply Voltage	2.7V ~ 3.6V DC
Working Current	Depends on profiles, 30mA typical.
Standby Current	<1mA
Operating Environment	
Temperature	-40ºC to +85ºC for A and I grade -20ºC to +70ºC for V and C grade
Humidity	10%~90% Non-Condensing
Certifications	BQB/FCC/CE
Environmental	RoHS Compliant
Dimension and Weight	
Dimension	23.24mm x 11.94mm x 2.00mm (2.2mm for FLC-BTM501D)
Weight	1g

Table 2: General Specification

3. Pin Definition

3.1 Pin Configuration

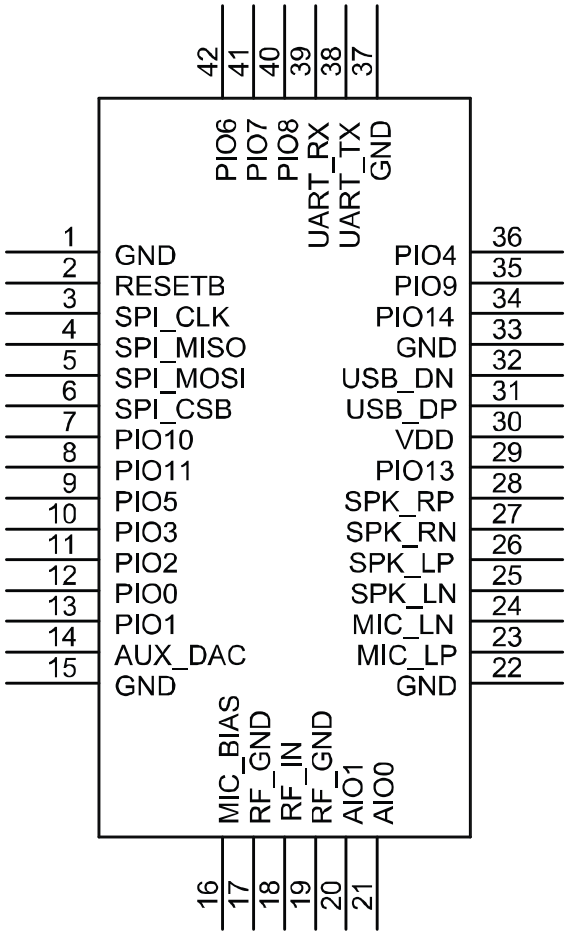

Figure 2: Pin Configuration

3.2 Pin Definition

Pin	Symbol	I/O Type	Description
1	GND	Ground	Ground
2	RESETB	CMOS input with weak internal pull-up	Active LOW reset
3	SPI_CLK	input with weak internal pull-down	Serial Peripheral interface clock for programming only
4	SPI_MISO	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface output for programming only
5	SPI_MOSI	CMOS input, with weak internal pull-down	Serial Peripheral Interface input for programming only

6	SPI_CSB	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface for programming only, active low
7	PIO10	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
8	PIO11	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
9	PIO5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
10	PIO3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
11	PIO2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
12	PIO0	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
13	PIO1	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
14	AUX_DAC	Analogue	Voltage DAC output
15	GND	Ground	Ground
16	MIC_BIAS	Analogue	Microphone Bias
17	RF_GND	RF Ground	RF ground
18	RF_IN	Analogue	Transceiver input/output line
19	RF_GND	RF Ground	RF ground
20	AIO1	Bi-directional	Analogue Programmable input/output line
21	AIO0	Bi-directional	Analogue Programmable input/output line
22	GND	Ground	Ground
23	MIC_LP	Analogue	Microphone input positive
24	MIC_LN	Analogue	Microphone input negative
25	SPK_LN	Analogue	Speaker output negative (left side)
26	SPK_LP	Analogue	Speaker output positive (left side)
27	SPK_RN	Analogue	Speaker output negative (right side)
28	SPK_RP	Analogue	Speaker output positive (right side)
29	PIO13	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
30	VDD	3.3v power input	3.3v power input
31	USB_DP	Bi-directional	USB data plus, pull up 1.5K when active
32	USB_DN	Bi-directional	USB data minus
33	GND	Ground	Ground
34	PIO14	Bi-directional with programmable	Programmable input/output line

		strength internal pull-up/down	
35	PIO9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
36	PIO4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
37	GND	Ground	Ground
38	UART_TX	Bi-directional CMOS output, tri-state, with weak internal pull-up	UART data output
39	UART_RX	CMOS input with weak internal pull-down	UART data input
40	PIO8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
41	PIO7	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
42	PIO6	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line

Table 3: Pin Definition

4. Physical Interfaces

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20µs or less. It is essential that the power rail recovers quickly.

4.2 Reset

The module may be reset from several sources: RESETB pin, power-on reset, a UART break character or via a software configured watchdog timer.

The RESETB pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active. It is recommended that RESETB be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-ups.

Pin Name / Group	Pin Status on Reset
USB_DP	Input with PD
USB_DN	Input with PD
UART_RX	Input with PD
UART_TX	Tri-state output with PU
SPI_MOSI	Input with PD
SPI_CLK	Input with PD
SPI_CSB	Input with PU
SPI_MISO	Tri-state output with PD
RESETB	Input with PU
PIOs	Bi-directional with PU
AIOs	Output, drive low
RF-IN	High impedance

Table 4: Pin Status on Reset

Note: Pull-up (PU) and pull-down (PD) default to weak values unless specified otherwise.

4.3 Audio Interfaces

Audio interface provides following features:

- Mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band

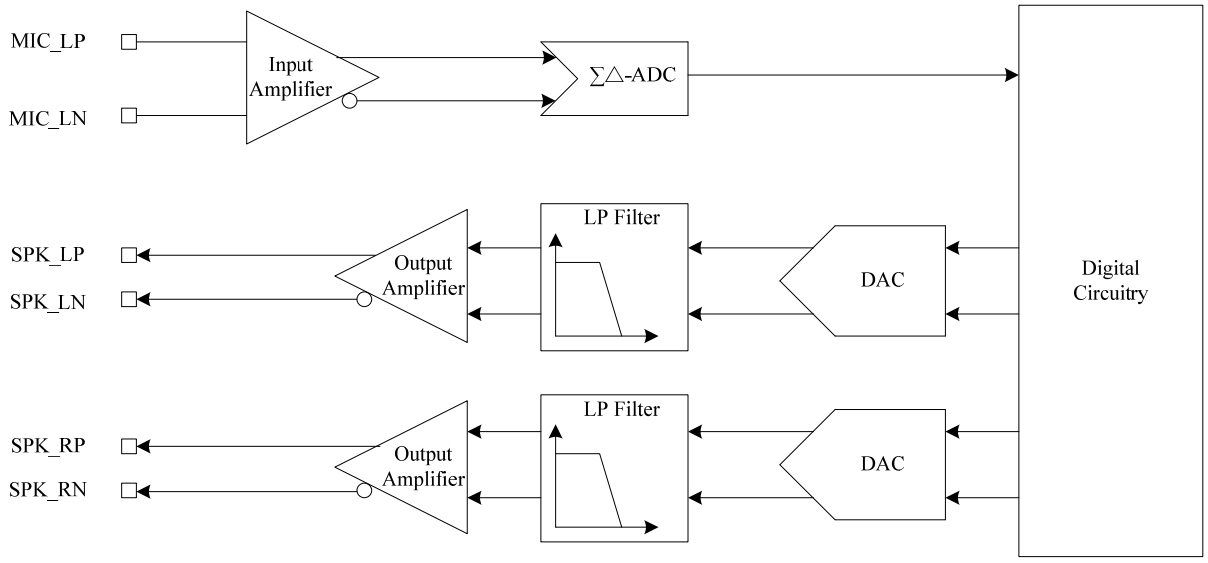

Figure 3: Audio Input and Output

The stereo audio CODEC uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a single power-supply of 1.5V and uses a minimum of external components. The module features a differential stereo audio output interfaces.

4.3.1 ADC

The ADC consists of a second order Digma Delta converter as show in **Figure 3**.

4.3.2 ADC Sample Rate Selection and Warping

ADC supports the following sample rates: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz.

One of the main concerns for stereo wireless music applications is the ability to keep sampl rates for the CODECs at both ends of the wireless link in synchronization. A VM function adjusts the sample rate using a 'warping' function to tune the sample rate to the required value. The ADC warp function allows the sample rate to be changed by +/-3%, in steps of $1/2^{17}$, or 7.6ppm. The warp function preserves the signal quality – the distortion introduced when warping the sample rate is negligible.

4.3.3 ADC Gain

The ADC contains two gain stages for each channel, an analogue and a digital gain stage.

4.3.4 DAC

The DAC contains two second order Sigma Delta converters allowing two separate channels that are identical in functionality as show in **Figure 3**.

4.3.5 DAC Sample Rate Selection and Warping

Each DAC supports the following sample rates: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz.

One of the main concerns for the DAC used in stereo wireless music applications is the ability to keep sample rates for the CODECs at both ends of the wireless link in synchronization. A VM function adjusts the sample rate using a 'warping' function to tune the sample rate to the required value. The ADC warp function allows the sample rate to be changed by +/-3%, in steps of $1/2^{17}$, or 7.6ppm. The warp function preserves the signal quality – the distortion introduced when warping the sample rate is negligible.

4.3.6 DAC Gain

The DAC contains two gain stages for each channel, a digital and an analogue gain stage.

4.3.7 Mono Operation

Mono operation is single channel operation of the stereo CODEC. The left channel represents the single mono channel for audio in and audio out. In mono operation the right channel is auxiliary mono channel that may be used in dual mono channel operation.

4.3.8 Audio Input Stage

The audio input stage of the module consists of a low noise input amplifier, which receives its analogue input signal from pins MIC_LP and MIC_LN to a second–order ∑-Δ ADC that outputs a 4Mbit/sec single-bit stream into the digital circuitry. The input can be configured to be either single ended or fully differential. It can be programmed for either microphone or line input and has a 3-bit digital gain setting of the input-amplifier in 3dB steps to optimize it for the use of different microphones.

4.3.9 Microphone Input

Check the reference design in **Figure 10** for the microphone input design.

4.3.10 Audio Output Stage

The output digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to a 2Mbits/sec multi-bit stream, which is fed into the analogue output circuitry.

The output circuit comprises a digital to analogue converter with gain setting and output amplifier. Its class-AB output-stage is capable of driving a signal on both channels of up to 2V pk-pk-differential into a load of 16Ω. The output is available as a differential signal between SPK_LP and SPK_LN for the left channel; and between SPK_RP and SPK_RN for the right channel. The output is capable of driving a speaker directly if its impedance is at least 8Ω if only one channel is connected or an external regulator is used.

The gain of the output stage is controlled by a 3-bit programmable resistive divider, which sets the gain in steps of approximately 3dB.

The multi-bit stream from the digital circuitry is low pass filtered by a second order bi-quad filter with a pole at 20kHz. The signal is then amplified in the fully differential output stage, which has a gain bandwidth of typically 1MHz.

4.4 RF Interface

The module integrates a balun filter. The user can connect a 50ohms antenna directly to the RF port.

4.5 General Purpose Analog IO

The general purpose analog IOs can be configured as ADC inputs by software. Do not connect them if not use.

4.6 General Purpose Digital IO

There are nine general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED displays or interrupt signals to host controller, etc. Do not connect them if not use.

4.6.1 Audio Signal Control

PIOs can be used to switch on/off external audio amplifier and microphone-bias generation. Please contact with Flaircomm for the special firmware.

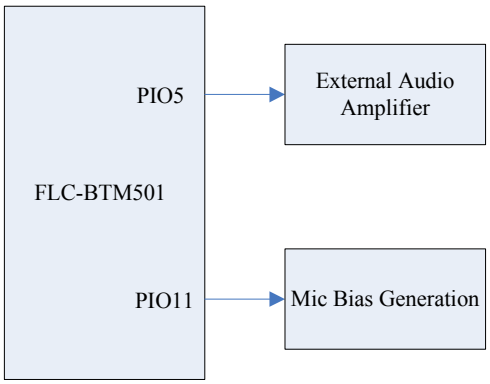

Figure 4: An Example of the Audio Signal Control by PIOs

4.7 Serial Interfaces

4.7.1 UART

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. PIO10 and PIO11 can be configured as UART_DTR and UART_RTS.

Parameter		Possible Values
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4M baud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Byte		8

Table 5: Possible UART Settings

When connecting the module to a host, please make sure to follow **Figure 5**.

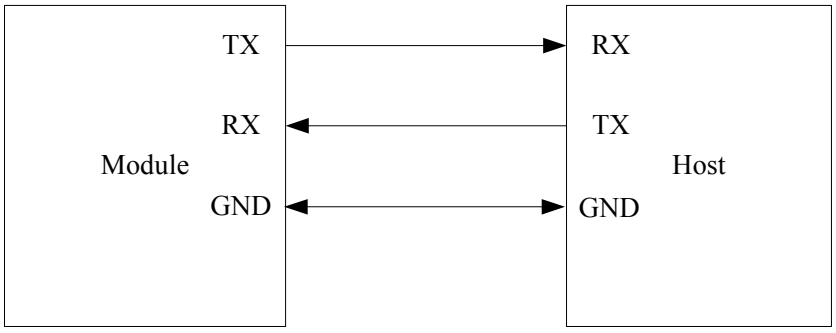

Figure 5: UART Connection

4.7.2 USB

There is a full speed (12M bits/s) USB interface for communicating with other compatible digital devices. The module acts as a USB peripheral, responding to request from a master host controller, such as a PC.

The module features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when module is ready to enumerate. It signals to the USB master that it is a full speed (12Mbit/s) USB device. The USB internal pull-up is implemented as a current source, and is compliant with section

7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ ±5% pull-down resistor (in the hub/host) when VDD =3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and DP on the USB cable.

4.7.2.1 Self-Powered Mode

In self-powered mode, the module is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to module via a resistor network (Rvb1 and Rvb2), so the module can detect when VBUS is powered up. The module will not pull USB_DP high when VBUS is off.

Self-powered USB designs (powered from a battery or LDO) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5KΩ 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self-powered mode. The internal pull-up in the module is only suitable for bus-powered USB devices, e.g., dongles.

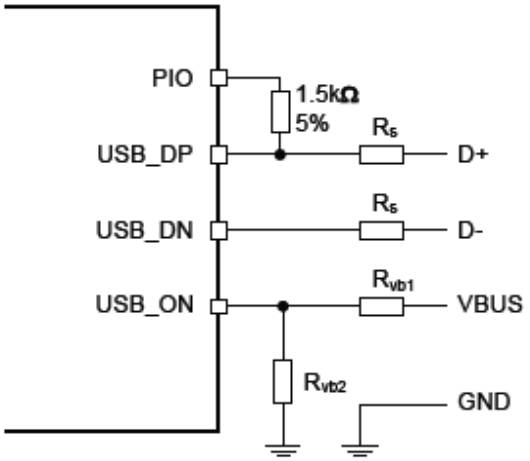

Figure 6: USB Connections for Self-Powered Mode

Note:

USB_ON is shared with the module PIO terminals.

Identifier	Value	Function
R_s	27Ω Nominal	Impedance matching to USB cable
Rvb1	22kΩ 5%	VBUS ON sense divider
Rvb2	47kΩ 5%	VBUS ON sense divider

Table 6: USB Interface Component Values

4.7.2.2 Bus-Powered Mode

In bus-powered mode, the application circuit draws its current from the 5V VBUS supply on the USB cable. The module negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume. For Class 2 Bluetooth applications, FLC recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus-powered mode, the module requests 100mA during enumeration. For Class 1 Bluetooth applications, the USB power descriptor should be altered to reflect the amount of power required. This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA. When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification. See USB Specification v1.1, section 7.2.4.1. Some applications may require soft start circuitry to limit inrush current if more than 10µF is present between VBUS and GND.

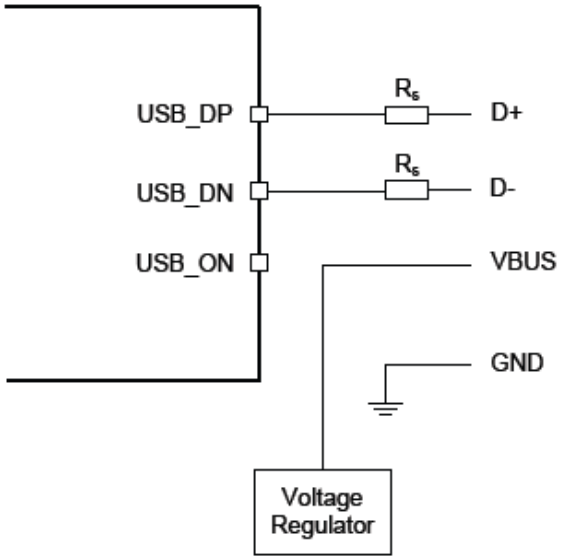

Figure 7: USB Connections for Bus-Powered Mode

4.7.3 I^2C

PIO8, PIO7 and PIO6 can be used to form a master I2C interface. The interface is formed using software to drive these lines. It is suited only to relatively slow functions such as driving a LCD, Keyboard, scanner or EEPROM. In the case, PIO lines need to be pulled up through 2.2Kohm resistors.

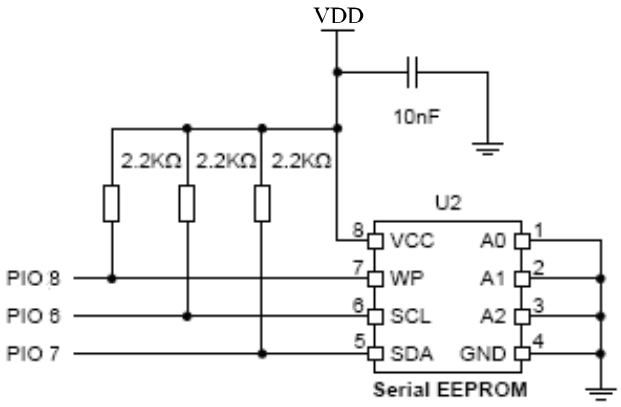

Figure 8: Example EEPROM Connection with I2C Interface

4.7.4 SPI

The synchronous serial port interface (SPI) can be used for system debugging. It can also be used for in-system programming for the flash memory within the module. SPI interface uses the SPI_MOSI, SPI_MISO, SPI_CSB and SPI_CLK pins. Testing points for the SPI interface are reserved on board in case that the firmware shall be updated during manufacture.

The module operates as a slave and thus SPI_MISO is an output of the module. SPI_MISO is not in high-impedance state when SPI_CSB is pulled high. Instead, the module outputs 0 if the processor is running and 1 if it is stopped. Thus the module should NOT be connected in a multi-slave arrangement by simple parallel connection of slave SPI_MISO lines.

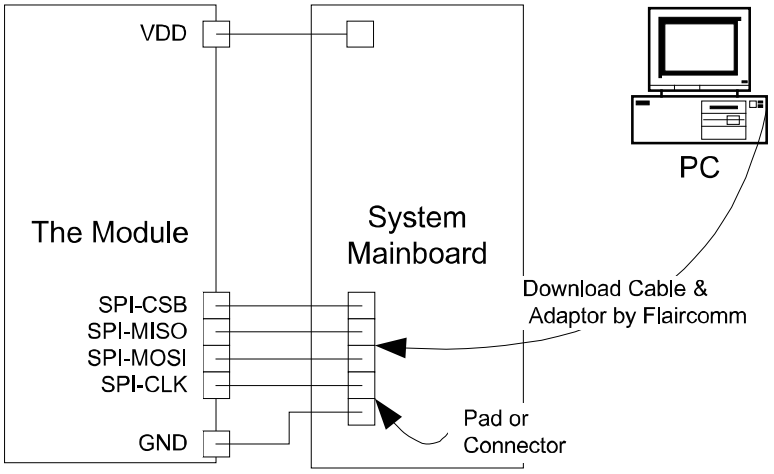

Figure 9: Design SPI for In-System Programming and Debug

5. Electrical Characteristic

5.1 Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+120	°C
Operating Temperature	-40	+85	°C
PIO/AIO Voltage	-0.4	+3.6	V
VDD_3V3 Voltage	-0.4	+3.6	V
USB_DP/USB_DN Voltage	-0.4	+3.6	V
Other Terminal Voltages except RF	-0.4	VDD+0.4	V

Table 7: Absolute Maximum Rating

5.2 Recommended Operating Conditions

Operating Condition	Min	Typical	Max	Unit
Storage Temperature	-40	--	+85	°C
Operating Temperature Range (for A and I grade)	-40	--	+85	°C
Operating Temperature Range (for V and C grade)	-20	--	+70	°C
VDD_3V3 Voltage	+2.7	+3.3	+3.6	V

Table 8: Recommended Operating Conditions

5.3 Input/output Terminal Characteristics

5.3.1 Digital Terminals

Supply Voltage Levels	Min	Typical	Max	Unit
Input Voltage Levels				
VIL input logic level low	-0.3	-	+0.25xVDD	V
VIH input logic level high	0.625VDD	-	VDD+0.3	V
Output Voltage Levels				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.125	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75xVDD	-	0.625xVDD	V
Input and Tri-state Current				
Ii input leakage current at Vin=VDD or 0V	-100	0	100	nA
Ioz tri-state output leakage current at Vo=VDD or 0V	-100	0	100	nA
With strong pull-up	-100	-40	-10	µA

With strong pull-down	10	40	100	µA
With weak pull-up	-5	-1.0	-0.2	µA
With weak pull-down	-0.2	+1.0	5.0	µA
I/O pad leakage current	-1	0	+1	µA
CI Input Capacitance	1.0	-	5.0	pF
Resistive Strength				
Rpuw weak pull-up strength at VDD-0.2V	500k	-	2M	Ω
Rpdw weak pull-up strength at 0.2V	500k	-	2M	Ω
Rpus strong pull-up strength at VDD-0.2V	10k	-	50k	Ω
Rpds strong pull-up strength at 0.2V	10k	-	50k	Ω

Table 9: Digital Terminal

5.3.2 USB

USB Terminals	Min	Typical	Max	Unit
Input Threshold				
V_{IL} input logic level low	-	-	0.3VDD	V
V_{IH} input logic level high	0.7VDD	-	-	V
Input Leakage Current				
GND < VIN < VDD[(a)]	-1	1	5	µA
CI Input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V_{IL} output logic level low	0.0	-	0.2	V
V_{IH} output logic level high	2.8	-	VDD	V

Table 10: USB Terminal

(a) Internal USB pull-up disabled

5.3.3 Internal CODEC - Analogue to Digital Converter

Parameter	Min	Typical	Max	Unit
Resolution	-	-	16	Bits
Input Sample Rate	8	-	44.1	kHz
Signal / Noise, f_{in}=1kHz, BW=20Hz->20kHz A-Weighted THD+N<1% 150mV Vpk-pk				
F_{sample} = 8kHz	-	82	-	dB
F_{sample} = 11.025kHz	-	81	-	dB
F_{sample} = 16kHz	-	80	-	dB
F_{sample} = 22.05kHz	-	79	-	dB
F_{sample} = 32kHz	-	79	-	dB
F_{sample} = 44.1kHz	-	78	-	dB

Digital Gain		-24	-	21.5	dB

Table 11: Analogue to Digital Converter

5.3.4 Internal CODEC - Digital to Analogue Converter

Parameter	Min	Typical	Max	Unit
Resolution	-	-	16	Bits
Output Sample Rate, Fsample	8	-	48	kHz
Signal / Noise, f_{in}=1kHz, BW=20Hz->20kHz A-Weighted THD+N<0.01% 0dBFS signal Load-100kΩ				
F_{sample} = 8kHz	-	95	-	dB
F_{sample} = 11.025kHz	-	95	-	dB
F_{sample} = 16kHz	-	95	-	dB
F_{sample} = 22.05kHz	-	95	-	dB
F_{sample} = 32kHz	-	95	-	dB
F_{sample} = 44kHz	-	95	-	dB
F_{sample} = 48kHz	-	95	-	dB
Digital Gain	-24	-	21.5	dB
Gain Resolution		1/32		dB

Table 12: Digital to Analogue Converter

5.3.5 Microphone Input

Microphone Input	Min	Typical	Max	Unit
Input full scale at maximum gain	-	4	-	mV rms
Input full scale at minimum gian(differential)		800	-	mV rms
Gain	-3	-	42	dB
Gain resolution	-	3	-	dB
Distortion at 1kHz	-	-	-74	dB
3dB Bandwidth	-	20		kHz
Input impedance	-	6		kΩ
THD+N(microphone input)@30mV rms input	-	0.04	-	%

Table 13: Microphone Input

5.3.6 Speaker Output

Speaker Driver	Min	Typical	Max	Unit
Output voltage full scale swing (differential)	-	750	-	mV rms

THD+N 100kΩ load		-	-	0.01%	%
THD+N 16Ω load		-	-	0.1%	%
SNR(Load=16Ω, 0dBFS input relative to digital silence)		-	95	-	dB
Allowed Load	Resistive	16(8)	-	O.C.	Ω
	Capacitive	-	-	500	pF

Table 14: Microphone Output

5.4 Power consumptions

Operating Condition	Min	Typical	Max	Unit
Connected Idle (Sniff 1.28 secs)		0.19		mA
Connected with audio streaming	40	45	50	mA
Deep Sleep Idle mode		60		uA

Table 15: Power consumptions

6. Reference Design

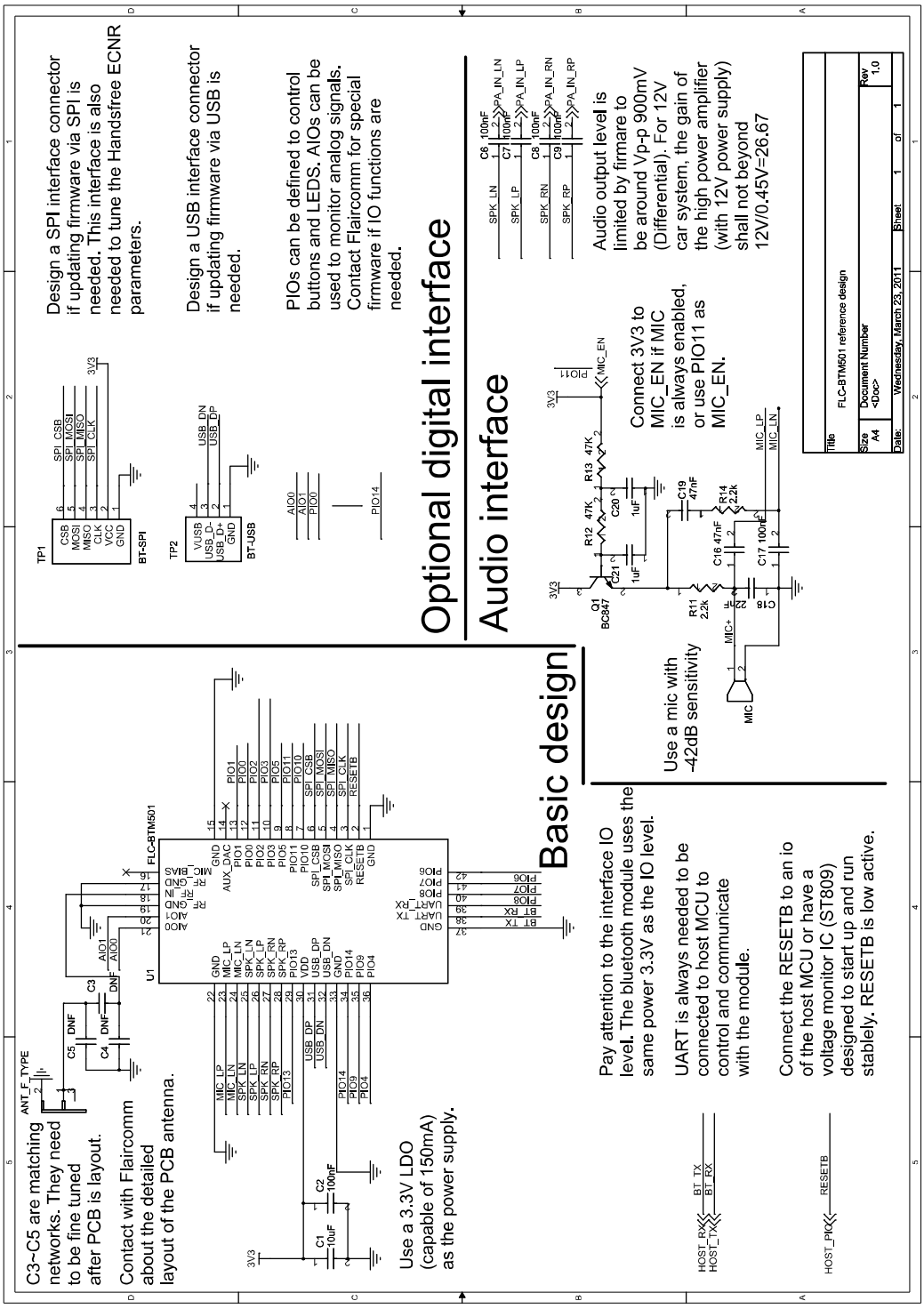

Figure 10: Reference Design

7. Mechanical Characteristic

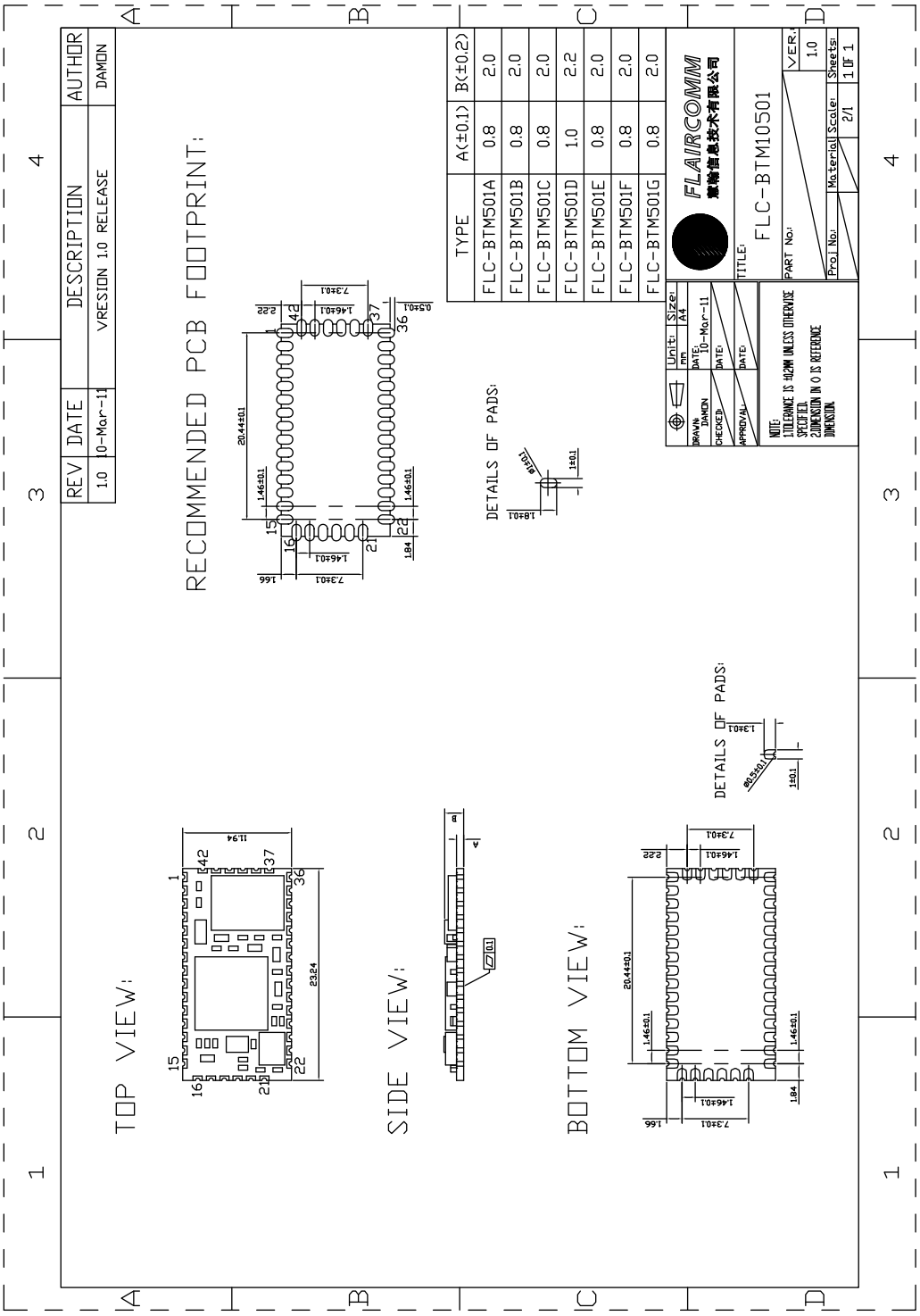

Figure 11: Mechanical Characteristic

8. Recommended PCB Layout and Mounting Pattern

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50Ω and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in **Figure 12** below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

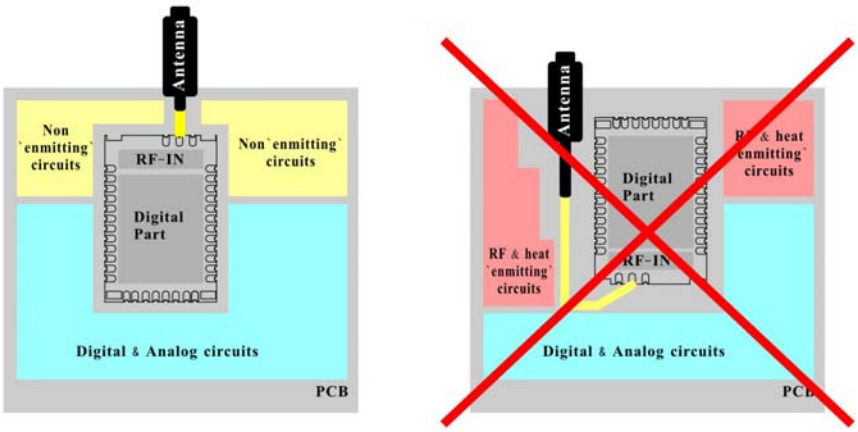

Figure 12: Placement the Module on a System Board

8.1 Antenna Connection and Grounding Plane Design

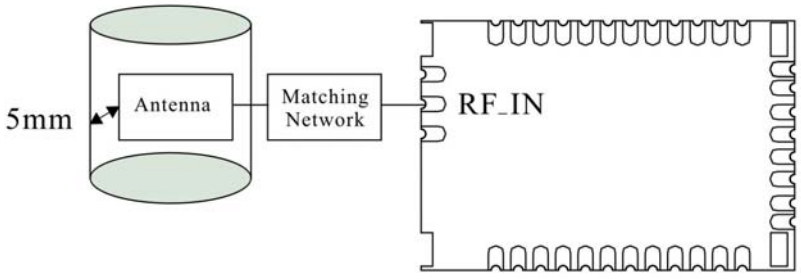

Figure 13: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

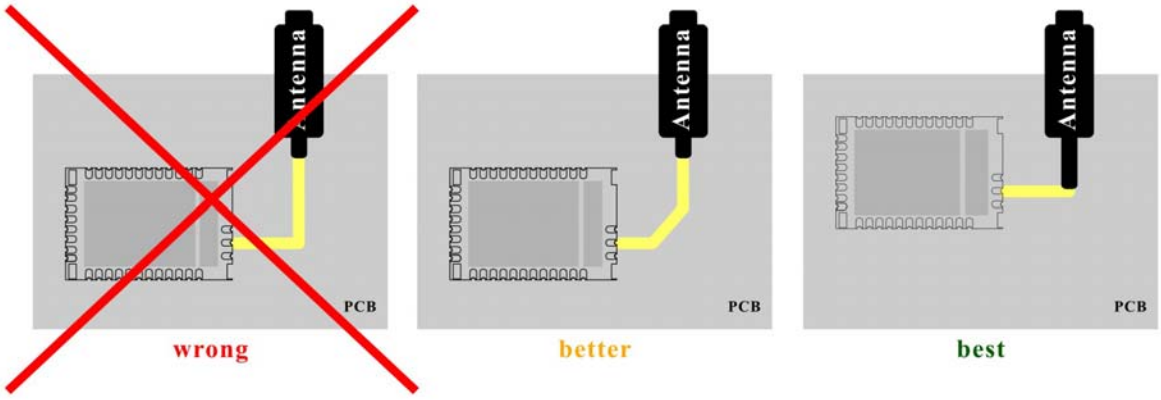

Figure 14: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

9. Recommended Reflow Profile

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

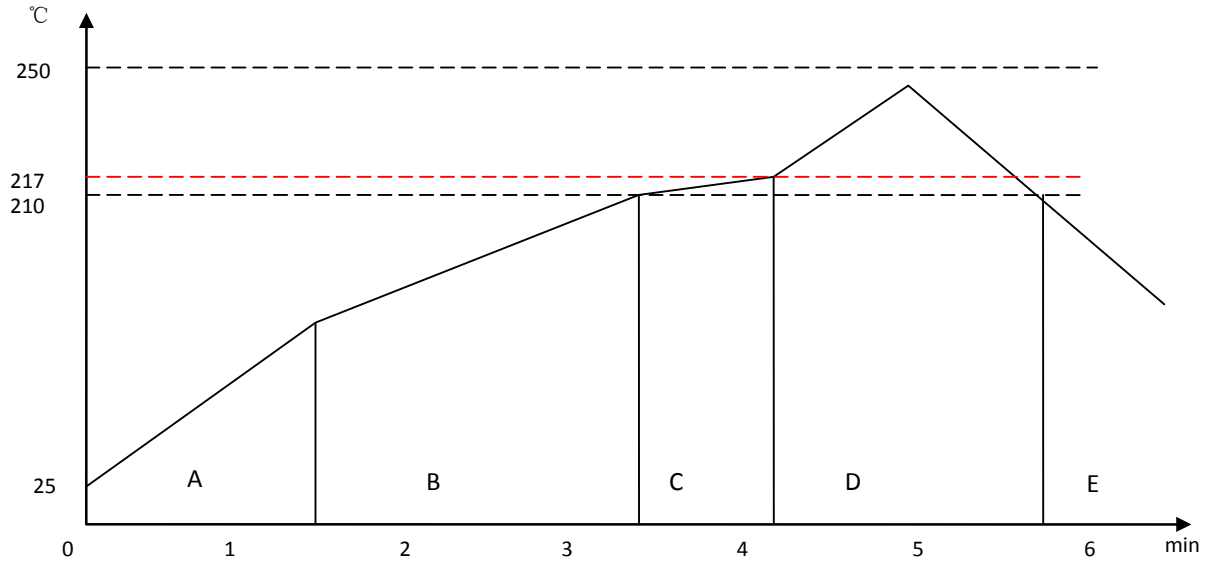

Figure 15: Recommended Reflow Profile

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone**.

Equilibrium Zone 2 (c) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longerlasting joint. **Typical cooling rate should be 4 °C**.

10. Ordering Information

10.1 Product Packaging Information

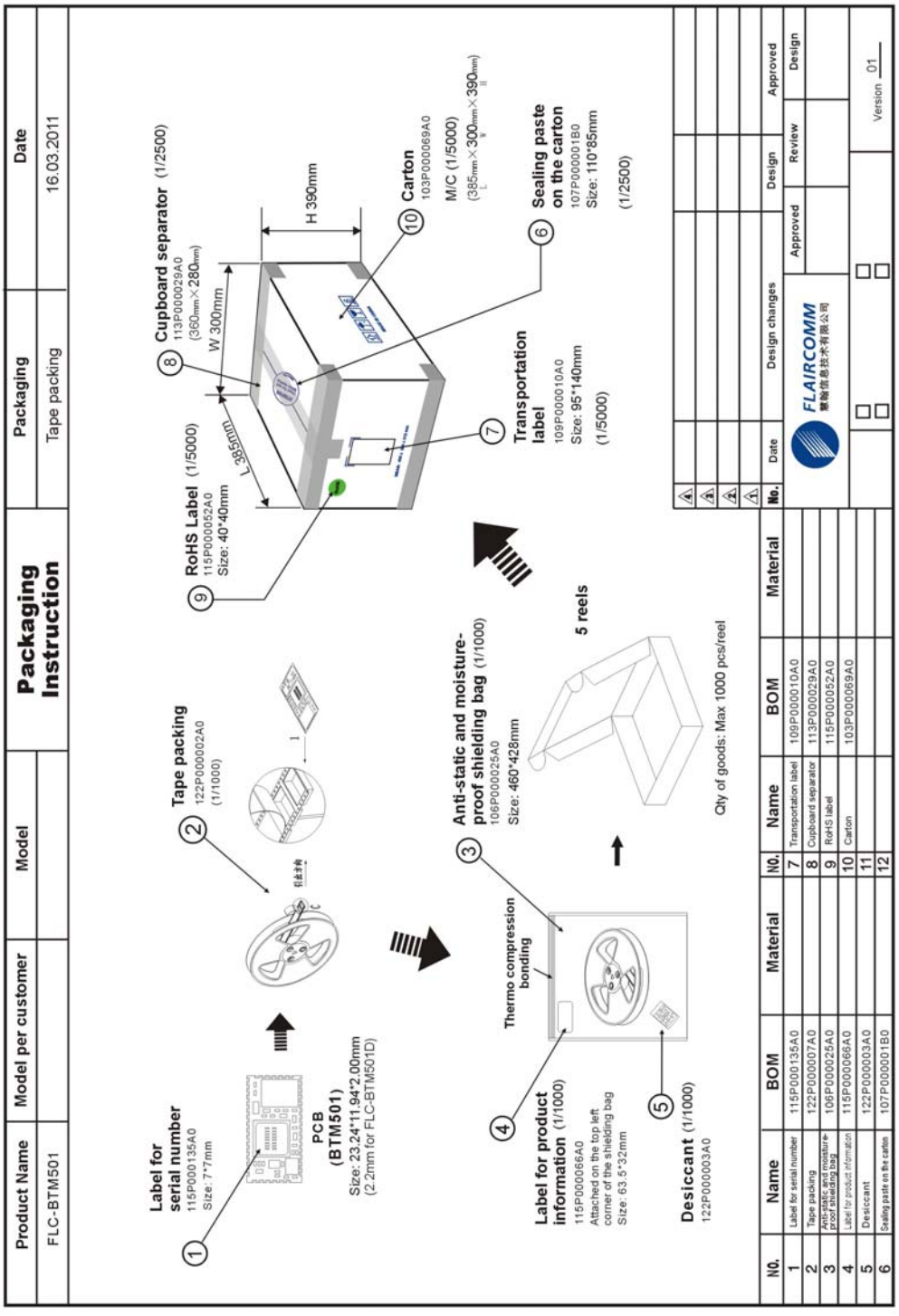

Figure 16: Product Packaging Information (Tape)

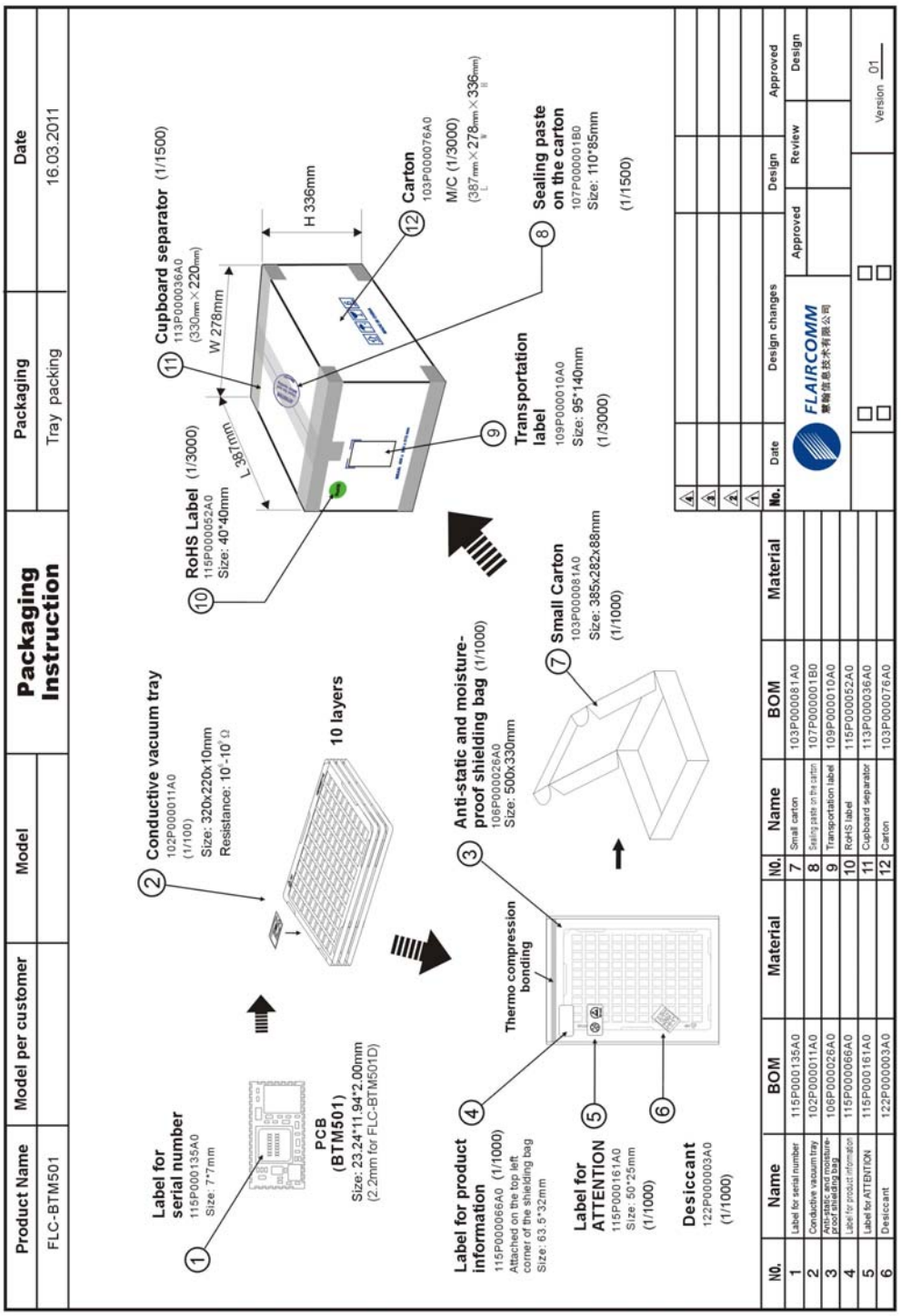

Figure 17: Product Packaging Information (Tray)

10.2 Ordering information

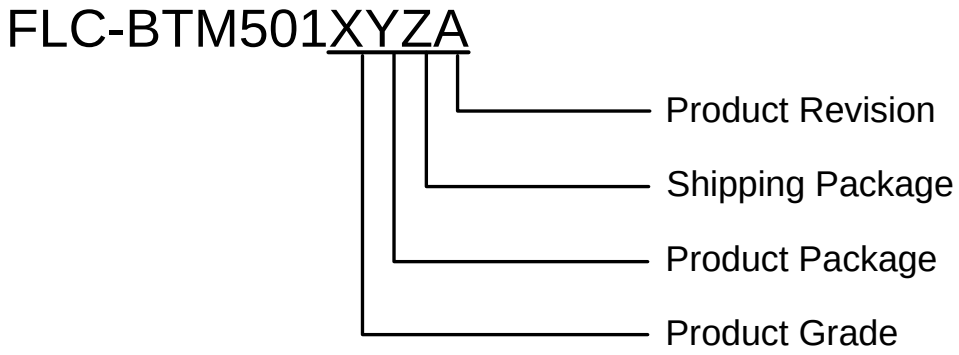

Figure 18: Ordering Information

10.2.1 Product Revision

Product Revision	Product Grade	Availability
A	C/V	Yes
B	C/V	Yes
D	A/I	Yes
E	A/I	Yes

Table 16: Product Revision

10.2.2 Shipping Package

Shipping Package	Description	Quantity	Availability
0	Foam Tray	—	No
1	Plastic Tray	100x10x3 = 3000	Yes
2	Tape	1000x5 = 5000	Yes

Table 17: Shipping Package

10.2.3 Product Package

Product Package	Description	Availability
Q	QFN	Yes
L	LGA	No
B	BGA	No
C	Connector	No

Table 18: Product Package

10.2.4 Product Grade

Product Grade	Description	Availability
C	Consumer	Refer to Table 16
I	Industrial	Refer to Table 16
V	Automobile After-Market	Refer to Table 16
A	Automobile Before-Market	Refer to Table 16

Table 19: Product Grade